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Optimized System Level Hardware Realization of Built-in-Self-Test Approach for Sigma-Delta Analog-to-Digital Converter

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ABSTRACT- System-level modeling is generally needed due to simultaneous increase in design complexity with multi-million gate designs in today's system-on-chips (SoCs). SystemC is generally applied to system-level modeling of Sigma-Delta ADC. CORDIC technique and test generation for the testing of mixed signal circuit components such as analog-to-digital converter is mostly implemented in system level modeling. This work focuses on developing fast and yet accurate model of BIST approach for Sigma-Delta ADC. The Sigma-Delta modulator's ADC static parameters as well as dynamic parameters are degraded. One of the dynamic parameters, signal-to-noise ratio (SNR) is directly obtained by the SIMSIDES (MATLAB SIMULINK tool). Then, the obtained parameters are tested by using Built-in-self-test that is desirable for the VLSI system in order to reduce the non-recurring cost (NRE) per chip by the manufacturer. This paper demonstrates a possibility to realize a simulation of testing strategy of high-resolution Sigma-Delta modulator using MATLAB SIMULINK and Xilinx EDA tool environment. This work also contributes towards the Output Response Analyzer (ORA) being used for testing parameters which help in reducing the difficulties in design of the complete ORA circuit. Moreover, the reusable features of hardware in the computation of different parameters are also improved in the ORA design.

Keywords- SNR; ADC; BIST; Output Response Analyzer; ORA; INL; TSG.

1. INTRODUCTION

With the increase in functionality of integrated on a single chip is basically a digital-driven trend. In order, to communicate with the outside or say analog world, analog-to-digital (A/D) and digital-to-analog (D/A) converter plays an important role towards the interfacing between analog and digital domains [3]-[5]. Analog-to-digital Converter (ADC) is widely used as a mixed signal device in many of the system-on-chip designs. Now a day, a trend toward integrating the complete mixed signal system onto a single chip is in heights. So with reduced size, cost and power consumption, the promotion towards the development of new generation of electronics systemic accomplishing all major features for the interaction of real time world to the digital processing circuitry is in its great demand.

The task of testing a VLSI chip to guarantee its functionality is exceptionally complex and often very time taking. In addition to the difficulty of testing the chips (IC) themselves, the incorporation of the chips into systems has caused test generation's cost to grow highly. The methodology to deal with the testing problem at the chip level is to incorporate built-in self-test (BIST) capability inside a chip. This increases the controllability and the observability of the chip [5]-[7], in conventional testing, test patterns are produced externally through the help of computer aided design tools (CAD). The test patterns and the expected responses of the Design under test to these test patterns are used by automatic test equipment (ATE) to determine if the actual responses same as the expected ones[29]. On the other hand, in built-in self-test, the test pattern generation and the output response estimation are done on chip; thus, the use of high-end automatic test equipment (ATE) machines to test chips can be avoided [10]-[12].

High-resolution ADCs with high sampling rates are required in a broad area of high-performance applications, such as high-grade imaging systems, wireless communications, and radar [14]-[18]. To deliver ADCs satisfying the requirements of the applications, it is obligatory that they are tested as less time as possible, but without negotiating the quality of the test. The analog to digital converter is the standard of the mixed circuit and this circuit is the most exclusive to test due both to the ADCs standard tests being quite long and to the high price of mixed signal testers and other test instruments [19]-[22]. The use of BIST techniques relieves the dependency on costly test equipment and allows delivering low-cost devices [23]-[26].

2. SIGMA-DELTA CONVERTERS

Sigma delta converters work at oversampling. That means the sampling frequency is much greater than message signal (Fm). Compared with Nyquist rate ADCs, oversampling ADCs gets high resolution in spite of analog components it uses digital signal processing for converting analog-to-digital conversion[27] and due to the oversampling sigma-delta ADCs; they do not required steep roll-off anti-alias filtering, [30]-[32]which is the prime requirement of Nyquist rate ADCs. Thus, higher order with better and higher linearity are no used and generally avoided to clarify why the study was undertaken and what hypotheses were tested[33]-[35]. In earlier research the hardware design of Analog to digital world standardized commonly by languages such as VHDL and Verilog. Lately, there has been a growing interest in alternative languages for coding at a much higher level of abstraction. System C, and System-Verilog represent the most widespread language Figure 1. Shown below. These languages equipped with well-known syntax with powerful constructs, enabling the realization and simulation of huge complex systems; in specially System C has grown up and become popular [28].

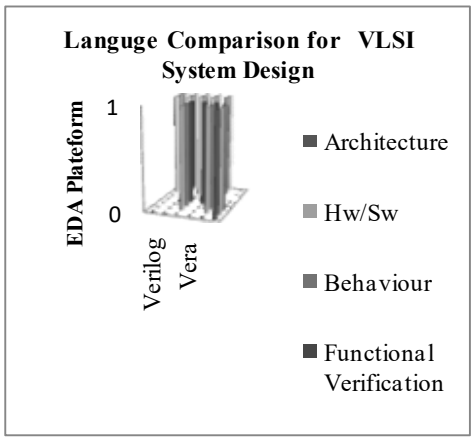

Figure 1. Language Comparison for Hardware Realization

3.METHOD

The method used in this work mainly uses following steps:

3.1 Test pattern Generation: We convert the BIST structure as digitized waveforms in to analog signals. The test signal is generated, the stored digitized waveform is periodically applied to the modulator under test.

The subsystem of Built-in Self-Test generates test stimulus signal which is a sinusoidal signal. The generated signal is highly trustful and highly configurable and also easily adjustable frequencies.

The resonators are formed by cascading two discrete-time integrators with the sign of one integrator being positive, negative. This arrangement is shown in Figure 2.

A digital resonator based on a Lossless Discrete Integrator (LDI) biquad circuit is used as test stimulus generator here. The resonator can be formed by cascading two discrete-time integrators.

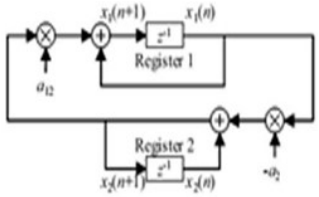

Figure 2. Proposed Test -Stimulus Generator for MATLAB

$$w_0 = f_{os}\cos^{-1}\left(1-\frac{a_{12}a_{21}}{2}\right) \quad for \quad 0 < a_{12}a_{21} \leq 4 \tag{1}$$

The second fact is that the amplitude (A) and phase (Ø) of the oscillating tone depend on the initial conditions imposed on registers $x_1$and x_2.

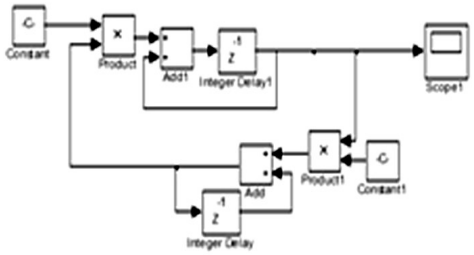

Figure 3. Simulink Realization of Test Vector Generator

3.2. On-Chip Signal Generator on VHDL and Verilog Platform

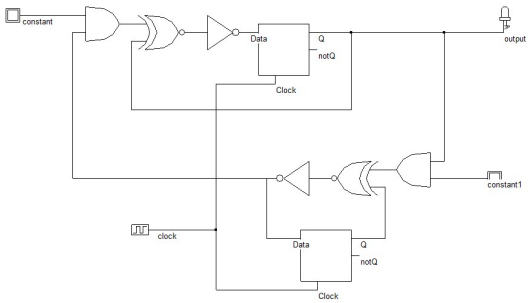

Figure 4. Hardware Gate Level Model Of Test Vector Generator.

3.3. System Level Hardware Retaliation of BIST Approach

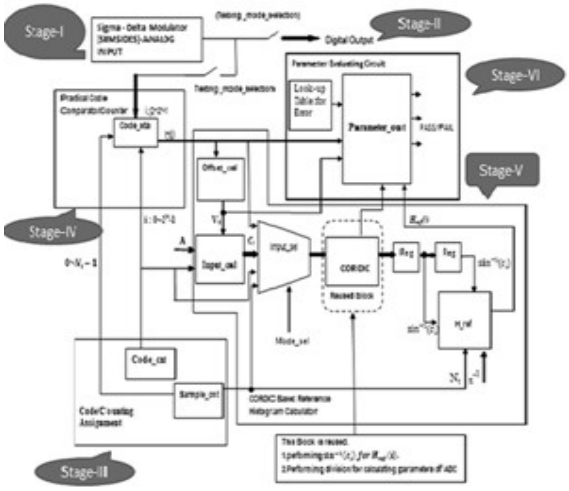

Figure 5. Proposed CORDIC enable ORA for BIST

3.4 Stage Description:

Stage-I: This stage include of the On-chip signal generator as well as the design of Sigma-Delta ADC using SIMSIDES.

Stage-II: This stage describe the digital output obtained from Stage-I.

Stage-III: in this stage Code_cnt and Sample_cnt Code/Counting Assignment counters is used.

Stage-IV: Comapres Code_sta the output from stage-I to the output from stage-II and according to that the counter will incremented its value.

Stage-V: This block makes all the necessary calculations such as INL, DNL, SNR using CORDIC-based Reference Histogram Calculator in response analyzer.

Stage-VI: Overall output of the Response Analyzer in the form of Pass/Fail is figure out by Parameter evaluating circuit

3.5 ADC under Test (Stage-I)

The Design under test (DUT) is a second order sigma delta modulator designed by using SIMSIDES.

SIMSIDES stand for (SIMULINK-based Sigma-Delta Simulator) is a MATLAB SIMULINK tool having S-function blocks and Z function block.

- *For giving the input:* Sine wave generator as proposed in fig.3 as the input.
- *For generating the SIMSIDES output*: After sending input to the sigma delta modulator its output is given for testing of pramertic faults.

3.6 Output of Second-Order Sigma-Delta Modulator (Stage – II)

The output of the Second-Order Sigma-Delta Modulator will be obtained using SIMSIDES whose, PSD (Power Spectral Density) is shown in figure 6. This graph shows the characteristic of the Modulator for the computation of different parameters such as static parameters and dynamic parameters. Table I. Shows all the input parameters required so as to obtain the characteristics of Sigma-Delta Modulator of figure 6.

Table I : Input paramètres required for the PSD

S. No	INPUT PARAMETER	VALUE
1	Signal to process	y
2	Sampling Frequency	fs
3	Window	Kaiser
4	No. of Points	N
5	Beta	30

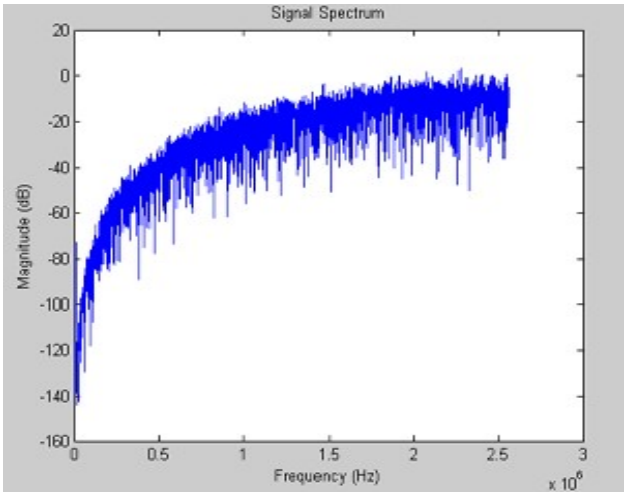

Figure 6: PSD of Second order Sigma-Delta Modulator

3.7 Output response analyzer (Stage-III)

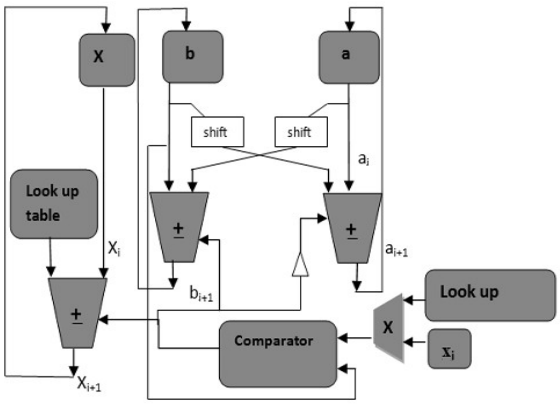

Figure7. Block diagram for CORDIC Computation technique

4. RESULT AND DISCUSSION

This section presented the experimental setup and the results of the simulated model .This section commences with a discussion of the components required in the experimental setup. The section then presents the result obtained. Finally, concludes by a discussion and analysis of the result obtained by considering required performance indicators like DNL, INL and SNR.

4.1 Calculassions of INL and DNL

Based on the theoretical calculation of INL and DNL shown in s the équations (1)-(3) the output from the CORDIC Technique can be calculated, but the practical calculation will be made directly from the SIMSIDES. The practical calculation is shown in figure 8. Where, first graph give the characteristic of DNL while the second graph shows the characteristic of INL.

4.2. Estimation of SNR

Signal to noise ratio is basically a measurement where a comparison between the levels of desired signal to that of the level of background noise is done or in other terms it is simply a ratio of signal power to that of the noise power.

$$SNR = \frac{Psignal}{Pnoise} \quad (1)$$

But to evaluate the theoretical value of ratio between signal and noise for our work when the static parameter i.e. Differential Non-Linearity will be taken into consideration we may use the equation (2), which shows the relation between them:-

$$SNR_d = -10.\log\frac{\sum_{i=1}^{2^n-2}[1+|G^2(DNL(i)^2+2DNL(i))|]}{2^n-2} \quad (2)$$

4.3 Computation of INL and DNL

The ADC static parameters i.e. differential nonlinearity (DNL) and integral nonlinearity (INL) can be directly obtained by comparing the reference histogram with the practical histogram. INL is defined as maximum deviation between the actual output level (after removing the errors i.e. offset error and the gain error) and ideal output of the modulator. DNL is basically used for measuring the accuracy of the modulator by calculating the deviation between two analog values that are corresponding to adjacent input digital values.

Using the values of equation no (3) we can find the values of INL and DNL with the help of following equations.

$$DNL(i) = DNL_0(i) + \epsilon_i, i = 1,2,\ldots..2^N - 2 \quad (3)$$

$$\text{Error} = (2^N - 2)^{-1}\sum_{i=1}^{2^N-2}[1 + |G^2(DNL(i)^2 + 2DNL(i))|] \quad (4)$$

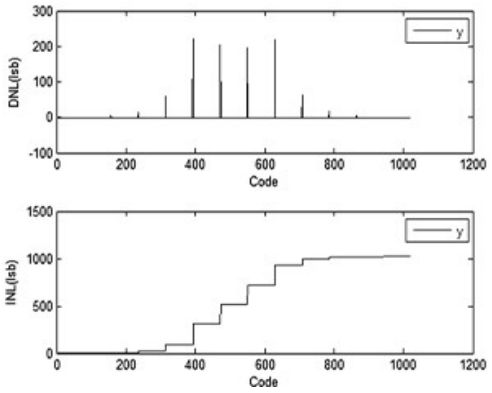

Figure 8. SIMSIDES Computation of INL and DNL

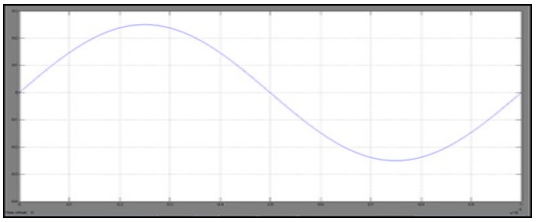

Figure 9. Scope Output of Stimules Vector Generator ($a_{21}=2^{-6}$, $a_{12}= 2.678\times10^{-4}$,$x_1(0) = 0$ and $x_2(0) = 0.0327250$, $f_{os}=$ 3.0725MHz.

4.4 For getting the BIST output:

The SIMSIDES output is given to the ORA of the BIST Circuit and the testing parameters are obtained .The op-amp based switched capacitor circuit for the second order Sigma-Delta Modulator is given as in figure 10.:

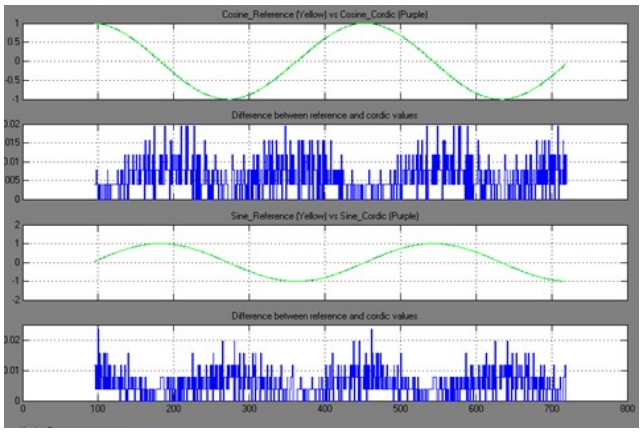

Figure 10. SIMSIDES ORA Response of calculated for Test Pass or Fail

Table II: Comparison Table of Result obtain

S. N.	Parameter	Ref.[3]	Ref.[9]	Ref.[27]	This Work
1	**Language [Accuracy]**	Low	Medium	Medium	**High**
2	**Simulation Speed**	Low	Medium	High	**Very High**
3	**Hardware Complexity**	Very High	Medium	Medium	**Low**
4	**DNL**	< + 0.01 LSB	< + 0.01 LSB	< + 0.01 LSB	**< + 0.01 LSB**
5	**INL**	< + 0.01 LSB	< + 0.01 LSB	< + 0.01 LSB	**< + 0.01 LSB**
6	**SNR**	-0.860	-0.87	-0.92	**-0.94**
7	**Data-bit width**	13 bit	13 bit	13 bit	**13 bit**

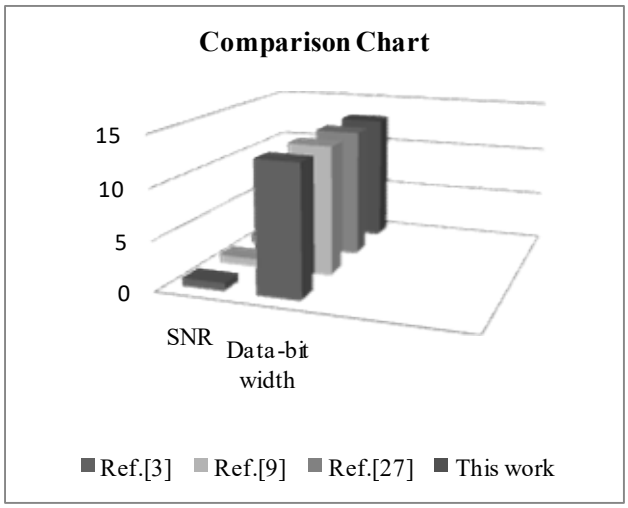

Figure 11. Shows Comparative result

5.CONCLUSION

This can be observed with the help of results and the discussions that the work is area efficient and better performance is resulted with improved the resolution and signal to noise ratio (SNR). Realization of system level Hardware model of BIST with 2nd order low-pass sigma-delta modulator design under test has been achieved. The special design could be applied to overcome the non-idealities. The modulator's static and dynamic parameters such as DNL, INL and SNR are obtained using CORDIC technique and are calculated using the proposed ORA circuit whose typical values are $\pm$ 0.2341, $\pm$ 0.2341 and 101.7833 respectively. A simple GUI interface has been designed for the calculation of dynamic specification (SNR=0.94 and data-bit width=13bits) of sigma delta analog to digital converter.

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