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Effect of changes in supply voltage on power consumption of digital CMOS delay lines

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ABSTRACT- In the beginning of the last decade, battery-powered hand-held devices such as mobile phones and laptop computers emerged. For that application we have to design a device which will consume minimum amount of energy. For that reason in this article we focused on power consumption and how to calculate the power. In this paper, an analysis of different delay lines based on CMOS architecture has been done. The effect of supply voltage on digital delay lines has been analysed as how supply voltage affected the value of power consumption of the digital delay line. After the analysis of those performance parameters, the trade-off has been made for better performance of delay lines.

Keywords- Power consumption, delay line, CMOS, supply voltage.

1. INTRODUCTION

There has been a tremendous growth in the computer, radar system and television market. As a outcome, the demand for elements which provide time control over pulse data has led to the development of a great form of delay lines; delay lines which find use in systems that relate electrical information to time. Computers, musical instruments, television studios, telemetering systems, guided missiles, radar systems and video tape recorders are typical systems that use delay lines.

As we know that every logic gate is a delay cell. So, we study different logic gates and developed delay lines with these logic gates. We used BSIM level 49 with .35 micron technology in simulation of these logic gates.

A. Delay line with chain of inverters

In this delay line, inverters are connected in series and making a delay line as show in figure 1. The delay of one inverter is about 24 picoseconds (psec). The delay of 10 state delay line is approximate 683psec.

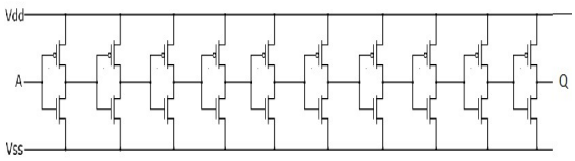

Fig 1. Chain of inverter based delay line

B. Delay line with NAND Gate

We used here 10 NAND gates in series. A single NAND gate work as a single delay cell. The delay of one delay cell is 36.41ps. The delay of 10^{th} stage is 987.99psec.

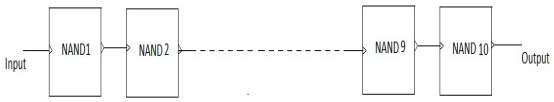

Fig. 2. 10 stage delay line with series of NAND

C. Delay line with NOR gate

We used 10 stages of nor gates. One nor gate work as single delay cell. After simulation we find a delay of one delay cell is 26.73ps. the 10 stage delay line with nor gate shown in figure 3.

Fig. 3. 10 stage delay line with series of NOR

There are 10 delay cells in the above delay line. It means we uses 10 nor gates in series. Hence, the delay of 10^{th} stage is 1.56×10^{-9} sec .

2. PARAMETERS CALCULATION OF THE DELAY LINE

A. Propagation Delay

As illustrated in Figure 4, the delay of a gate can be modulated by modifying the supply voltage. This ductility agrees the designer to trade-off energy dissipation for performance, as we will see in a next phase. However, increasing the supply voltage above a certain level yields only very minimal improvement and hence should be avoided. Also, Credibility about (hot-electron effects and oxide breakdown) enforce firm upper-bounds on the supply voltage in deep sub-micron processes.

We know that continuing technology scaling forces the supply voltages to reduce at rates similar to the device dimensions [1]. At the similar time, device threshold voltages are essentially collect constant. The reader perhaps amazement concern the impact of this trend on the integrity parameters of the CMOS circuits. Do circuits keep on working when the voltages are scaled and are there potential limits to the supply?

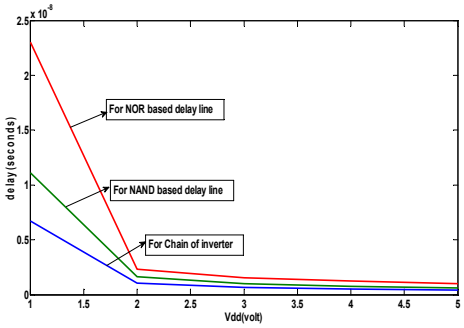

Fig. 4 Supply voltage v/s Delay for different delay line

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B. POWER CONSUMPTION

In order to computes the power consumptions, we has to take into the accounts how often the devices are switch. If the gate are switch on and off *f*(0-1) time per seconds, the power consumptions are given by

$$P_{dyn} = C_L V_{DD}{}^2 f \quad \text{.... (1)}$$

Where f represent the frequency of energy consuming transitions. Dynamic powers consist mostly of the switching powers, give in EQ (1). The supply voltages V_{DD} and frequency f is readily known by the designers. To estimates this power, one may considers each node of the circuits. The capacitances of the nodes are the sum of the gates, diffusions, and wire capacitance on the node.

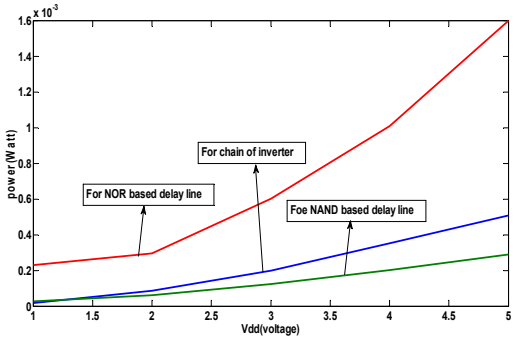

Fig. 5. Power v/s Supply voltage

Above figure 5 shows the graph between power dissipation and supply voltage. According to the figure it is clear that, by increasing the supply voltage power consumption increases. As V_{DD} are a quadratic term,its are good to select the minimum V_{DD} that may supports the require frequency of operations. Likewise, we chooses the lowest frequency of operations that achieve the desire end performances. Finally, the circuits can be optimize to reduce the overall load capacitances of each and every sections.

The calculation of dynamic power dissipation is given below,

1. For chain of Inverter

Delay of inverter chain without load = 692 psec

Then taking a load capacitance C_L of 20pf.

Delay of inverter chain with 20 pf load= $6.23*10^{-8}$

We know that the Elmore's delay equation $\tau = 0.69RC$

Where $\tau = 6.23*10^{-8}$

Put this value in above equation

$\tau = 0.69RC$

$6.23*10^{-8} = 0.69*R*20*10^{-12}$

$R = 4.5144K$.....(2)

$\tau = 0.69RC$

$692*10^{-12} = 4.514*10^{3}*C_L*.69$

$C_L = 222fF$.....(3)

Where

$Power = C_L V_{DD}^2 f$

$Power = 222*10^{-15}*9*0.1*10^{9}$

$Power = 199.3\mu W$

Equation (2) shows the extract value of load resistance and equation (3) shows the extract value of load capacitance for calculating the total power consumption through the device.

2. For NAND based delay line

Delay of NAND based delay line without load = $9.87*10^{-10}$ psec

Then taking a load capacitance C_L of 20pf.

Delay with 20 pf load= $1.45*10^{-7}$

We know that the Elmores delay equation $\tau = 0.69RC$

Where $\tau = 1.45*10^{-7}$

Put this value in above equation.

$$\tau = 0.69RC$$

$$1.45*10^{-7} = 0.69*R*20*10^{-12}$$

$$R = 10507.24.ohm.....(4)$$

$$\tau = 0.69RC$$

$$9.87*10^{-10} = 10507.24*C_L*.69$$

$$C_L = 1.36*10^{-13}F.....(5)$$

Where

$$Power = C_L V_{DD}^2 f$$

$$Power = 1.36*10^{-13}*9*0.1*10^9$$

$$Power = 1.225*10^{-4}W$$

Equation (4) shows the extract value of load resistance and equation (5) shows the extract value of load capacitance for calculating the total power consumption through the device.
Similarly for the other delay lines,
For NOR based delay line power consumption will be = $601.2\mu W$

3. CONCLUSIONS

Due to tremendous growth in computer and television market, development of great variety of delay lines occur. As per increasing the requirement, the complexity of delay lines also increased in terms of handling the performance parameters like power dissipation and propagation delay. So, designer have to control all these performance parameters and the tradeoff conditions occurring among these performance parameters.

If we further scaling the technology that we are used, then it is possible to get some much better results. This is the only way which can help us for further improving the performance of delay lines. By scaling the technology our area will going to decreased, and if our area will going to decrease, then our load capacitance will also decreases and this directly affected the value of delay. So, technology scaling played a major role in improving the performance of digital CMOS delay lines.

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