International Journal of Electrical & Electronics Research (IJEER)
FOREX Publication
Multi-disciplinary | Open Access | ISSN: 2347-470X

Date of Publication: 31 July 2019 | Volume 7, Issue 3 | Pages: *11-18*

Design of Low Leakage Arithmetic Logic circuit Using Efficient Power Gating Schemes

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ABSTRACT: As technology scales towards nanometer regime the leakage power consumption emerging as a major design constraint for the analysis and design of complex arithmetic logic circuits. In this paper, comparative analysis of standby leakage current and sleep to active mode transition leakage current has been done. An innovative power gating approaches is also analyzed which targets maximum reduction of major leakage current.

To analyze we introduce the stacking power gating scheme, we implemented this scheme on carry look ahead adder circuit and then simulation has been done using stacking power gating scheme with 45nm technology parameters. The simulation results by using this scheme in BPTM 45nm technology with supply voltage of 0.9V at room temperature shows that leakage reduction can be improved by 47.14% as on comparison with single transistor gating scheme on comparing with conventional scheme

Also, another novel approach has been analyzed with diode based stacking power gating scheme for further reduction in leakage power. The simulation results depicts that the analyzed design leads to efficient carry look ahead adder circuit in terms of leakage power, active power and delay.

Index Terms: High Performance Power Gating Schemes, Leakage power, sleep to active mode transition.

1. INTRODUCTION

In nanometer circuits, where design flexibility is much more stringent than in deep submicron era, drastic increase of leakage currents due to aggressive scaling of technologies make it very crucial to develop efficient technique to minimize leakage current. For portable electronic devices this equates to maximizing battery life. For example, mobile phones need to be powered for extended periods (known as standby mode), but are fully active for much shorter periods (known as talk or active mode, while making a call). When an electronic device such as a mobile phone is in standby mode, certain portions of the circuitry within the electronic device, which are active when the phone is in talk mode, are shut down. These circuits, however, still have leakage currents running through them, even though they have been de- activated. Even if the leakage current is much smaller than the normal operating current of the circuit. The leakage current depletes the battery charge over the relatively long standby time, whereas the operating current during talk time only depletes the battery charge over the relatively short talk time. As, a result, the leakage current has a disproportional effect on total battery life. Now a day's battery dependent portable application such as mobile phones, iPod and laptop computers operate in standby mode more than active mode. Reducing the ground bounce noise and stand by leakage power consumption of the portable devices during these long idle periods is highly desirable for a longer battery lifetime and device's long life for normal functionality. That is why building low power, low ground bounce noise and low leakage adder cells are of great interest.

Adders are the heart of computational circuits and many complex arithmetic circuits are based on addition [1], [2]. The adder circuits are commonly /aimed to reduce power consumption and increase speed. These studies have also investigated different approaches realizing adders using CMOS technology [3], [4]. For mobile applications, designers have to work within a very tight leakage power specification in order to meet product battery life and package cost objectives.

Finally, the paper is organized as follows: Section II motivates for the improved leakage reduction power gating schemes. Section III analyzed innovative diode based power gating schemes that have better performance in terms of leakage current and overall fluctuations in ground rails as compared to existing power gating schemes. The analyzed full adder schemes and diode based power gating schemes along with the strategies used to reduce leakage power are presented in section IV. Section V gives the comparative analysis of simulation results and finally the paper is concluded in section VI.

2. MOTIVATION FOR THE IMPROVED LEAKAGE CURRENT

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In recent times, leakage power reduction has received much attention in academia as well as industry. Several means of reducing leakage power have proposed. The most natural way of lowering the leakage power dissipation of a VLSI circuit in the STANDBY state is to turn off its supply voltage. This can be done by using one PMOS transistor and one NMOS transistor in series with the transistors of each logic block to create a virtual ground and a virtual power supply as depicted in Figure 2 [15]. But in practice only one transistor is necessary. Because of their lower on-resistance, NMOS transistors are usually used. In the ACTIVE state, the sleep transistor is on. Therefore, the circuit functions as usual. In the STANDBY state, the transistor is turned off, which disconnects the gate from the ground. Additional savings may be achieved if the width of the sleep transistor is smaller than the combined width of the transistors in the pull-down network. In practice, Dual V_{TH} CMOS or Multi-Threshold CMOS (MTCMOS) is used for power gating .In these technologies there are several types of transistors with different V_{TH} values. Transistors with a low V_{TH} are used to implement the logic, while high-V_{TH} devices are used as sleep transistors. To guarantee the proper functionality of the circuit, the sleep transistor has to be carefully sized to decrease its voltage drop while it is on. The voltage drop on the sleep transistor decreases the effective supply voltage of the logic gate. Also, it increases the threshold of the pull-down transistors due to the body effect. This increases the high-to-low transition delay of the circuit. This problem can be solved by using a large sleep transistor. On the other hand, using a large sleep transistor increases the area overhead and the dynamic power consumed for turning the transistor on and off.

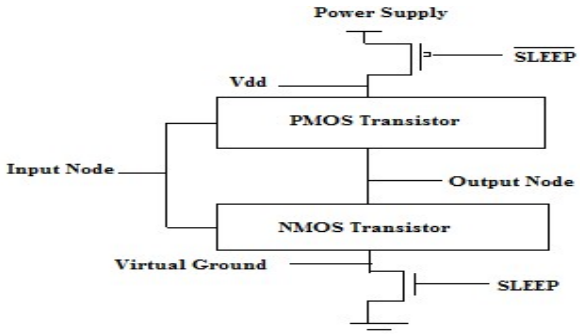

Figure 1: Power Gating Circuit

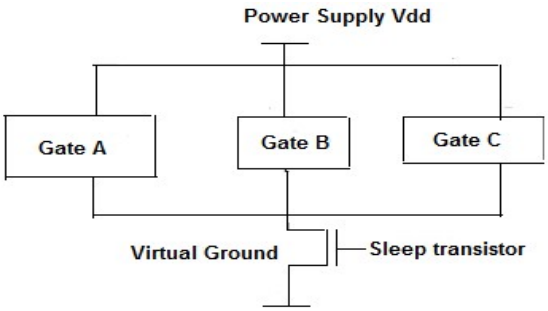

Figure 2: Using one sleep transistor for many gates [18]

3. HIGH PERFORMANCE INNOVATIVE POWER GATING SCHEMES

3.1 Stacking Power Gating Scheme

Stacking power gating scheme is one of the high performance innovative power gating scheme. Stacking sleep transistors are used to reduce the magnitude of peak current and voltage glitches in power rails i.e. ground bounce noise. Stacking power gating scheme works on reduction of leakage current by stacking effect and reduction of ground bounce noise by controlling the intermediate node voltage.

As the new trend towards low Vth transistors and as technology scaling down to nanometer channel length regime, there is need of modification of topology, which greatly suppress the leakage current in standby mode than existing conventional power gating structures. By taking the advantage of stacking scheme leakage current can be controlled in standby mode. This can be seen from figure 4. Here sleep transistors ST1 and ST2 are stacked. When in standby mode i.e. When ST1 and ST2 both are off. In this structure firstly, the leakage current is reduced by stacking effect, turning both ST1 and ST2 sleep transistors OFF. This raises the intermediate node voltage VGND to positive values to small drain current [14]. Stacking sleep transistors are used in stacking power gating scheme to reduce the magnitude of peak current and voltage glitches in power rails i.e. ground bounce noise [8]-[12]. Positive potential at the intermediate node has four effects:

1. Gate to source voltage of ST1 (Vgs1) becomes negative

2. Negative body- to- source potential (Vbs1) of ST1 causes more body effect.

3. Drain- to- source potential (Vds1) of ST1 decreases, resulting in less drain induced barrier lowering. Drain- to- source potential (Vds2) of ST2 is less compared to ST1, because most of the voltage drops across the ST1 in sleep mode. This significantly reduces the drain induced barrier lowering. The expression for the sub threshold leakage current is [14].

$$I_{sub}=Ae^{q/nkT\,(Vgs-Vtho+\gamma Vbs+\eta Vds)}(1-e^{-qVds/KT}) \quad (1)$$

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Where A= μCox (W/Leff) (KT/q)^2 e$^{1.8}$, Vgs, Vds and Vbs are the gate- to- source, the drain- to- source, and the bulk- to- source voltages, respectively. The bulk is connected to ground. Γ and η are body effect and DIBL coefficients respectively. Vtho is the zero-bias threshold voltage. Cox is gate- oxide capacitance, μ0 is the zero- bias mobility, and is the sub threshold swing coefficient. From equation (1) it is observed that an increase in the body effect (negative Vbs), and reduction in Vds (less DIBL) reduce the sub threshold current exponentially. So by using simple stacking effect we can able to reduce the leakage in standby mode. But we cannot able to reduce the ground bounce noise.

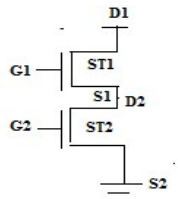

Fig.3 Stacking Structure

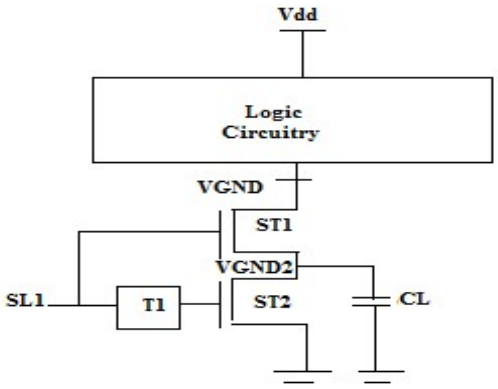

Fig.4. Stacking power gating scheme [3]

Further, by modifying this scheme ground bounce noise that occurs during mode transition can be reduced fig.5. The strategy is as follows:

1. Isolating the ground for small duration during mode transition
2. Turning On the ST2 transistor in linear region instead of saturation region to decrease the current surge.
3. During sleep to active mode transition, transistor ST1 is turned ON and transistor ST2 is turned ON after a small duration of time (T1). The logic circuit is isolated from the ground for a short duration as the transistor ST2 is turned OFF. During this duration, the ground bounce noise can be greatly reduced by controlling the intermediate node voltage VGND2 and operating the transistor ST2 in triode region. The intermediate node (VGND2) voltage can be controlled by inserting proper amount of delay that is less than the discharging time of the ST1 transistor and by proper selection of the capacitance CL.

Stacking power gating has three modes of operations

1. Active mode
2. Standby mode
3. Sleep to active mode transition

In active mode, the sleep signal of the transistor is held at logic '1' and both the sleep transistors ST1 and ST2 remain ON. The equivalent circuit of sleep transistors ST1 and ST2 is shown in fig.5. In this case both transistors offers very low resistance and virtual ground (VGND) node potential is pulled down to the ground potential, making the logic difference between the logic circuitry approximately equal to the supply voltage to work properly. $R1_{on}$ and $R2_{on}$ are equivalent resistances of ST1 and ST2 transistors, when the transistor ST1 and ST2 are turned ON. Hence, they offer very low resistances i.e. $R1_{on}$ and $R2_{on}$ are very low. C1 is the internal node capacitance of drain of transistor ST1. C2 is the external capacitance placed in between the transistors ST1 and ST2 to control intermediate node voltage. As compared to external capacitance, internal capacitance at drain of ST2 is neglected. In active mode,

Voltage across the capacitor C1 = V_{C1} (active *mode)* = V ($R1_{on}$) + V ($R2_{on}$) = 0V.

Voltage across the capacitor C2 = V_{C2} (active *mode)* = V ($R2_{on}$) = 0V.

To reduce the leakage current in standby mode, power supply rail and ground rail is isolated by turning OFF the sleep transistors. The sleep signal SL1 is held at logic '0' to switch OFF the sleep transistors ST1 and ST2 are shown in fig. 6. $R1_{OFF}$ and $R2_{OFF}$ are ST1 and ST2 OFF resistances, and offers very high resistances. So there is no discharging path for C1 and C2 transistors. The capacitor C1 will charge up to the V_{DD}. Capacitor C2 charges to small amount of voltage, because most of the charge is acquired by the capacitor C1, giving no path for capacitance C2 to charge. As high threshold voltage sleep transistor ST1 is OFF, so it potentially blocks the leakage current to charge up the capacitance C2. In standby mode capacitance C1 (virtual ground node) has been charged up to V1 and the capacitor C2 has been charged to V2.

So, V_{C1} (*standby mode*) = V1, V_{C2} (standby *mode*) = V2

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In sleep to active transition mode, initially the transistor ST1 is turned ON. After small duration of time (T1) transistor ST2 is tuned ON to reduce the ground bounce noise. The parameters T1 and the capacitance C2 are decided based on design objectives.

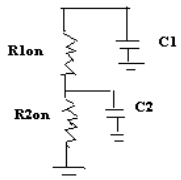

Fig.5. Equivalent circuit of sleep transistors ST1 and ST2 in active mode

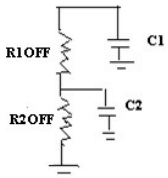

Fig.6. Equivalent circuit of sleep transistors ST1 and ST2 in standby mode.

3.2 Diode based Stacking Power Gating Scheme

If we incorporate the strategy which is operating the sleep transistor as a diode in stacking power gating leads diode based stacking power gating. We can get more ground bounce noise reduction by incorporated strategy. Stacking sleep transistors (T1, T2) are used in diode based stacking power gating scheme shown in fig.7 reduce the magnitude of peak current and voltage glitches in power rails i.e. ground bounce noise. The diode based stacking power gating scheme consists of 5 parts:

- Transistors T1, T2 are the sleep transistors which are high Vt transistors for less leakage current.
- Transistor S1 is a control transistor used to make the sleep transistor S1 working as a diode during mode transition.
- TG1 is the transmission gate.
- Tn time delay provided for T1 and T2.
- C2 is the capacitor inserted in the intermediate node VGND2.

In this scheme, 3 strategies have been used to reduce the peak of ground bounce noise and leakage current.

1. Making the sleep transistor working as a diode during mode transition for some period of time due to this limitation in large transient hence reduction in the peak of ground bounce noise.
2. Isolating the ground for small duration during mode transition this was achieved by delay circuitry.
3. Turning ON the T2 transistor in linear region instead of saturation region to decrease the current surge was achieved by a capacitor placed in intermediate node.

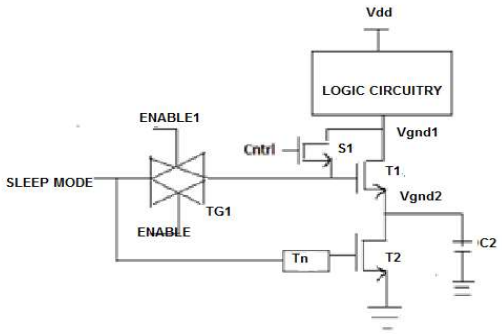

Fig.7. Diode based stacking power gating scheme

Ground bounce noise problem occurs when circuit is going from sleep to active and vice-versa. Diode based stacking power gating scheme combines the aforementioned three strategies to minimize the instantaneous current flow through the sleep transistors. There are several benefits of combining stacked sleep transistors with capacitors. First the magnitude of power supply fluctuations/ ground bounce noise during mode transitions will be reduced because these transitions are gradual. Second, while conventional power gating uses a high-threshold device as a sleep transistor to minimize leakage, a stacked sleep structures can achieve the same effect with a normal threshold device. Fig. 8 shows the applied signals to this scheme.

Diode based Stacking power gating scheme has three modes of operations: Active mode, Standby mode and Sleep to active mode transition.

In active mode, the sleep signal of the transistor is held at logic '1'and both the sleep transistors T1 and T2 remain ON and control transistor is OFF by giving logic 0. In this case both transistors offer very low resistance and virtual ground (VGND) node potential is pulled down to the ground potential, making the logic difference between the logic circuitry approximately equal to the supply voltage. While in standby mode leakage current is reduced by the stacking effect, turning both T1 and T2 sleep transistors OFF.

The analyzed design give major contribution in sleep to active mode in terms of peak of ground bounce noise compared to stacking power gating. Ground bounce noise occurs when circuit is going from sleep to active and vice versa. In first stage sleep transistor (T1) working as diode by turn on the

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control transistor S1 which is connected across the drain and gate of the sleep transistor (T1). Due to this drain to source current of the sleep transistor drops in a quadratic manner. This reduces the voltage fluctuation on the ground and power net and it also reduces the circuit wakeup time.

So in sleep to active transition mode, we are turning ON transistor T1 initially after small duration of time S2 will be turned ON to reduce the ground bounce noise. In second stage control transistor is off that sleep transistor works normally. During sleep to active mode transition, transistor S1 is turned ON and transistor T2 is turned ON after a small duration of time (T1).

The logic circuit is isolated from the ground for a short duration as the transistor T2 is turned OFF. During this duration, the ground bounce noise can be greatly reduced by controlling the intermediate node voltage VGND2 and operating the transistor T2 in triode region.

The intermediate node (VGND2) voltage can be

1. Controlled by inserting proper amount of delay, that is less than the discharging time of the T1 transistor.

2. Proper selection of the capacitance C2.

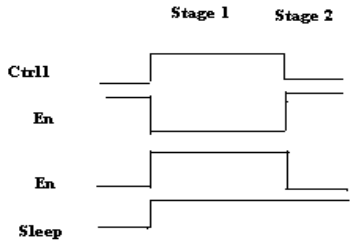

Fig.8. Applied signals to the diode based stacking power gating Scheme [26].

4. LEAKAGE REDUCTION APPROACH USING POWER GATING SCHEME AND VALIDATION THROUGH CARRY LOOK AHEAD ADDER CELL

A new transistor resizing approach method for leakage power reduction using power gating circuits is discussed in this section. We validate approach through 1 bit full adder cell. Fig.10 shows the conventional CMOS full adder using 28 transistors. This is considered as a Base case for comparison.

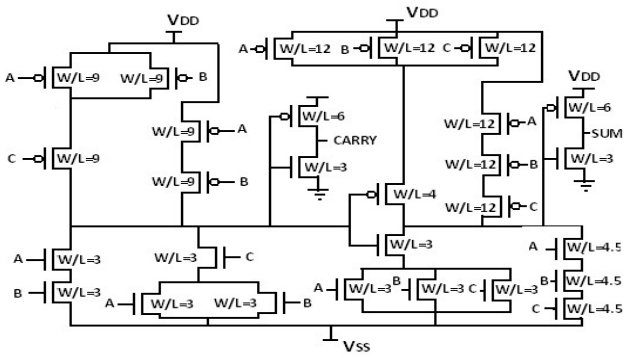

Fig.9. Conventional Full Adder

The CMOS structure combines PMOS pull up and NMOS pull down networks to produce considered outputs. The transistor sizes are specified as a ratio of Width/Length (W/L). The sizing of transistors plays a key role in static CMOS style. It is observed in the conventional adder circuit that the transistor ratio of PMOS to NMOS is 2 for an inverter and remaining blocks also followed the same ratios when we considered the remaining blocks as an equivalent inverters. This ratio doesn't give best results with respect to noise margin and standby leakage power when it is simulated in 90nm process. Modified adder circuits with sizing are presented in full adder1 and full adder2 targeting the standby leakage current, and ground bounce noise. Further, power gating scheme is used to reduce the leakage power, where a sleep transistor is connected between actual ground rail and circuit ground. Ground bounce noise is being estimated when the circuits are connected with a sleep transistor as shown in fig. 11. Full adder circuit 1 with sleep transistor and its equivalent circuit are shown in fig 12 and fig.13 respectively. The smallest transistor considered for 90nm technology has a width of 120nm and a length of 100nm and gives W/L ratio 1.2. The W/L ratio of NMOS is fixed at 1.2 and W/L of PMOS is 3.8 which is 3.16 times that of NMOS in full adder1. The sizing of each block is based on the following assumption.

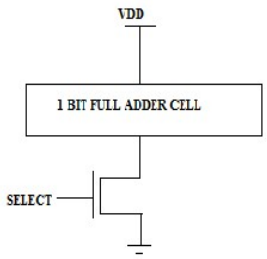

Fig.10. One bit full adder cell with sleep transistor

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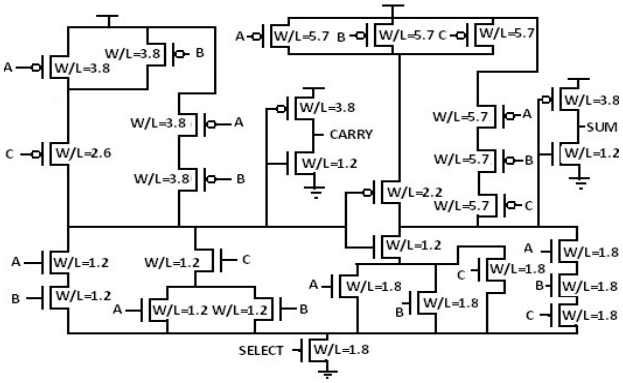

Fig.11. Carry Look Ahead Adder circuit with sleep transistor

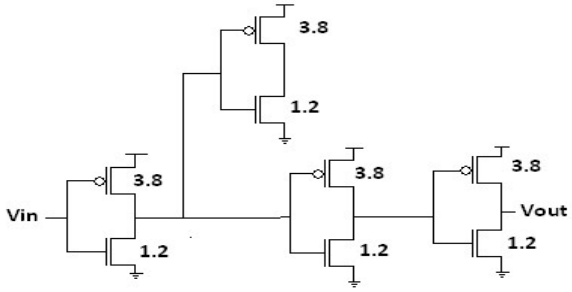

Fig.12. Equivalent circuit for CLA

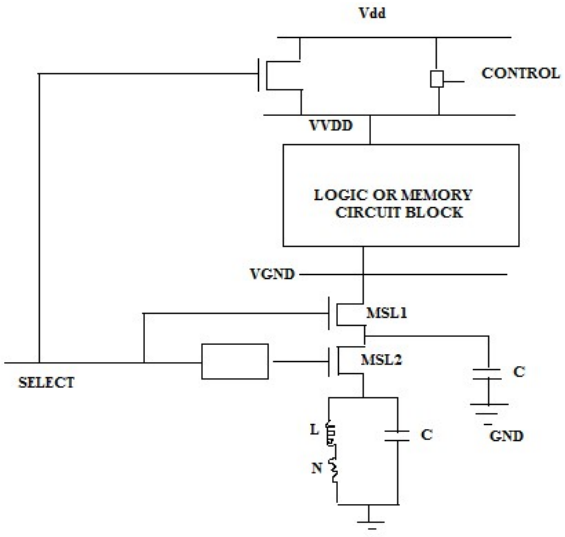

Fig.13. Proposed Scheme or Improved Power Gating Scheme

TABLE 1: Effect of temperature on standby Leakage Current of 74182 Benchmark circuit for various power gating techniques

Temperature (ºC)	27ºC	75ºC	100ºC
Base Case	203	518	922.2
Stacking power gating	20.05	250.95	555.7
Diode based stacking	18.9	200.91	430.92
Diode based staggered phase damping	6.95	198	333.3

Further a 4-bit adder circuit using cascaded stacking power gating scheme has been analyzed and the conditions for the important design objectives i.e. (i) Minimum ground bounce noise (ii) Minimum standby leakage power have been achieved by using the modified design where ground bounce noise has been controlled by using stacked sleep transistors with delta T delayed SELECT signal for MSL2. Further, this scheme increases the circuit performance in terms of leakage power.

In scheme we have implemented cascading of stacking power gating, which turns on by a single pulse applied at the first stacking power gating SELECT signal input. When the inputs A_0,B_0, are applied only first full adder get activated and when S_0 and C_1 are calculated next full adder got activated and the previous one got deactivated this process continues till final results S_0, S_1,S_2 and C_f get calculated, hence in this scheme only one full adder get Vdd to GND path for current to flow at the time of its operation.

5. PERFORMANCE ANALYSIS AND SIMULATION RESULTS

There are various performance issues which must be considered while designing the logic circuits. In this paper, we do the performance analysis of 1bit full adder cell and 4bit full adder cells using improved power gating schemes which includes standby leakage power and ground bounce noise. Then diode based power gating schemes named diode based staggered phase damping scheme and diode based stacking power gating scheme simulation results and discussion will be presented. The simulation was done with the help of Cadence Spectre 90nm standard CMOS technology at room temperature with supply voltage of 0.9V. The entire simulation setup is shown in Table 2.

Standby leakage power is measured when the circuit is in standby mode. Sleep transistor is connected to the pull down

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network of 1 bit full adder cell (fig.10). Sleep transistor is off by asserting an input 0V. For simplicity, size of a sleep transistor is equal to the size of largest transistor in the network (pull up and pull-down) connected to the sleep transistor. The sleep transistor size in Full adder1 and Full adder2 is reduced due to the resizing of the adder cells in proposed circuit. Standby leakage is greatly reduced in both full Adder1, Full Adder2 and 4bit full adder circuit with stacking power gating as shown in fig.18. Standby leakage is greatly reduced in both Full adder1, Full adder2 and 4bit full adder with stacking power gating as shown in fig.18. In case of Full adder1 reduction in standby power is about 82%, in Full Adder2 it is about 84% and in 4bit full adder with stacking power gating it is about 87% for all input combinations.

TABLE 2: Simulation Set Up

Parameter	Description
Technology	45nanometer BPTM
Logic Circuit Topology	Static CMOS
Minimum Channel Length	45 nanometer
Low $V_{t,p}$	$2.02e^{-01V}$
Low $V_{t,n}$	$1.8e^{-01V}$
High Vt,n for sleep transistor	$2.5\ e^{-01V}$
Input vector sequence "AB"	"11"
Sizes of M1,M2	W/L = 45nm/45nm
Sizes of M3,M4	W/L= 225nm/90nm
Sizes of MSL1,MSL2	W/L = 90nm/90nm
C2	2.3fF

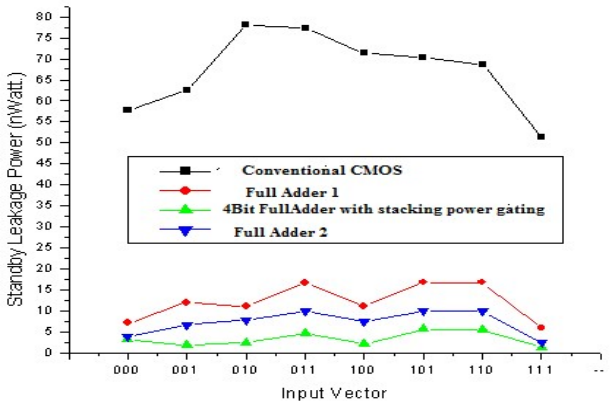

Fig.14. Comparison of standby leakage power with different input combinations of four designs

During the power mode transition, an instantaneous charge current passes through the sleep transistor, which is operating in its saturation region, and create current surges elsewhere, these surges result in voltage fluctuations in the power rails. If the magnitude of the voltage surge or circuit may erroneously latch to the wrong value or switch at the wrong time. Inductive noise, also known as simultaneous switching noise, is phenomena that have been traditionally associated with input/output buffers and internal circuitry. The noise immunity of a circuit decreases as its supply voltage is reduced such as power gating to address the problem of ground bounce in low-voltage CMOS circuits.

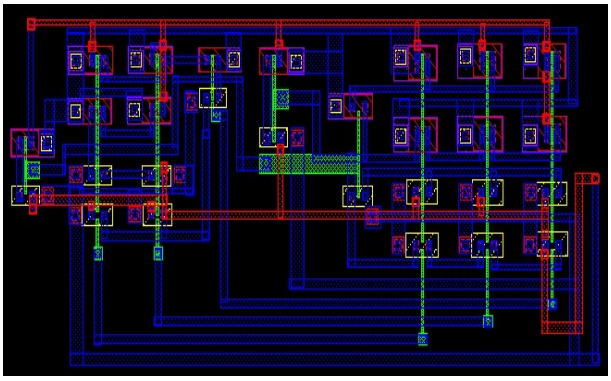

Fig.15. Layout of CLA with Stacking Power Gating Approach with 45nm technology

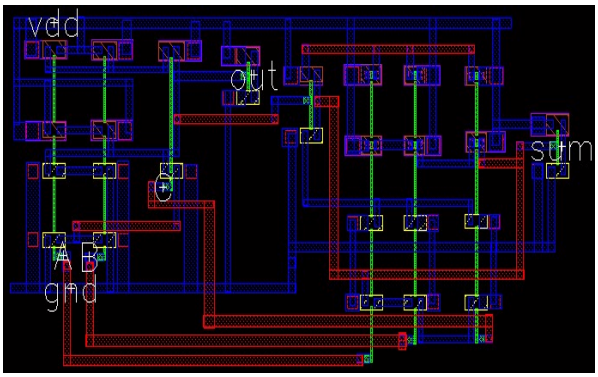

Fig.16. Layout of CLA with Diode based Stacking Power Gating Scheme with 45nm technology

5. CONCLUSION

Scaling down the CMOS technology feature size and threshold voltage for achieving high performance has resulted in increase of leakage power dissipation. This paper presented low leakage full adder cells with low ground bounce noise.

Experimental results show that in the proposed full adder cells, the leakage power is reduced by 82% (Full Adder1), 84% (Full Adder2) and 89% (4bit Full adder with stacked power gating scheme) in comparison to the conventional 1bit full adder. Ground bounce noise is reduced about 1.5 times in Full Adder1, 3 times in Full Adder2 and 12.3 times in 4bit Full

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Adder with stacking power gating respectively, compared to conventional full adder cell.

Since leakage and ground bounce are the two critical sources of noise in current nanoscale circuits and systems, reduction of leakages and ground bounce would definitely increase the reliability. However, it is important to note that the reduction of voltage level across the logic circuit during data retention mode will drastically reduce the noise tolerance of the circuits during that mode.

As most of the work analyzed here is for small circuits which are being utilized at various intermediate stages in large circuits, the problem of ground bounce noise is more important concern in the case of large electronic circuit because as technology is moving towards small sized portable embedded systems where the power is much important factor for its portability.

These portable systems are battery dependent and use power gating schemes to reduce standby leakage power so there is need to work for reduction of ground bounce noise with system prospective as the technology is moving to the era of system on chip so designer's main concern should be towards system level more than the single entity.

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