International Journal of Electrical & Electronics Research (IJEER)
Volume 2, Issue 2, Pages 5-11, June 2014, ISSN: 2347-470X

Leakage current analysis for stack based Nano CMOS Digital Circuits

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***Abstract*— Due to the growing impact of subthreshold and gate leakage, static leakage is contributing more and more towards the power dissipation in deep submicron Nano CMOS technology. There have been many works on subthreshold leakage and techniques to reduce it, such as controlling the input vector to the circuit in standby mode, forcing stack and body bias control. In this tutorial paper we have reviewed the leakage current with change in drain source, gate and bulk voltages for 4 different submicron technologies using the latest PTM models. Simulation result shows the effect of gate leakage and subthreshold leakage in total leakage current for different input vectors for a stack of 3 Nano technology NMOS transistors, further analyzes also the subthreshold and total leakage variation with input vector in a stack of 4 Nano technology NMOS transistors.**

Keywords - Leakage Current, Subthreshold Leakage Current, Gate Tunneling Leakage Current, Minimum leakage vector, Low power design, Digital CMOS Circuit.

1. Introduction

With the continuous scaling of CMOS devices, leakage current is becoming a major contribution to the total power consumption. In current deep-sub micrometer devices with threshold voltages, subthreshold and gate leakage have become dominant sources of leakage [6][9]. One of the most challenging aspects of today's CMOS VLSI circuits is standby power dissipation. Feature size reduction has made the effects of leakage currents more pronounced. This becomes more complicated in sub 100nm technologies with not only subthreshold leakage but also with the gate oxide [5]-[11].

Device dimensions are scaled down with each technology generation to increase the density and performance. With scaling of device dimensions, the supply voltage must be scaled down to keep power consumption low [12]. The speed of the circuit decreases if the ratio V_{dd}/V_{th} is less than five because the current driving capability decreases. Hence the transistor threshold voltage (V_{th}) has to be commensurately scaled to maintain a high drive current and achieve performance improvement. The scaling of threshold voltages results in an exponential increase in subthreshold current. However, threshold voltage scaling results in a significant amount of leakage power dissipation due to an exponential increase in the subthreshold leakage current conduction [9]. Borkar in [10] predicts a 7.5-fold increase in the leakage current and a five-fold increase in total energy dissipation for every new microprocessor chip generation. In order to maintain reasonable short channel effects (SCE), the gate oxide thickness (T_{ox}) has to be scaled. However the gate tunneling current increases with scaling of T_{ox} [10], [12].

This paper shows the minimum input vector for Subthreshold leakage, Gate leakage and total leakage current and the effect of adding stack transistor to a NMOS transistor for the reduction of gate leakage to total leakage ratio in nano-scale C-MOS circuit. We use an approach which takes an advantage of the natural leakage behavior in stacks of MOS transistors [16], [17] to reduce sleep mode leakage while avoiding active mode performance loss. We first identify a circuit input vector that will put most of the circuit into a low leakage state [3],[4]. In general, the low leakage state occurs when most of the MOS transistors are turned off in each leakage path which depends on the input vector [18] [2].

The remainder of this paper is organized as follows. Section 2 illustrates the analysis of Leakage current. Section 3 describes the Stack effect and input vector for minimum leakage current. Section 4 estimate and analyze the contribution of gate leakage and sub threshold leakage in total leakage for a stack of 3 NMOS transistors and subthreshold and total leakage variation with input vector in a stack of 4 NMOS transistors. Section 5 shows the simulation result, which analyze the various leakage currents in stack of NMOS transistor and describes the effect of adding stack transistor to a NMOS transistor for the reduction of gate leakage to the total leakage ratio in nano-scale CMOS circuit. Conclusion is given in Section 6.

2. Leakage Current Analysis

A. Gate Leakage Current

The gate direct tunneling leakage flows from the gate through the "leaky" oxide insulation to the substrate. The equation governing the current density of the direct tunneling is given by [7]

$$J_{DT} = AE_{OX}^{2} \exp\left\{ -\frac{B\left[1-\left(1-\frac{V_{ox}}{¤_{ox}}\right)^{\frac{3}{2}}\right]}{E_{ox}} \right\} \quad (1)$$

where

$$A = q^3 / 16\,\pi^2 \hbar\, \Phi_{ox}$$

$$B = 4\sqrt{2m^*}\;\; ¤^{3/2} \Big/ 3\hbar q \quad (2)$$

The direct tunneling occurs at $V_{ox} < \Phi_{ox}$

$$V_{gs} = V_{fb} + V_{ox} + \Phi_s + V_{poly}$$

Where V_{gs} is the applied gate bias, Φ_s is the surface potential and V_{poly} is the potential drop across the polysilicon depletion layer which depends on doping concentration of polysilicon.

Its magnitude increases exponentially with the gate oxide thickness Tox and supply voltage V_{dd}. According to the 2001International Technology Roadmap for Semiconductors, high-K gate dielectric reduced direct tunneling current is required to control this component of the leakage current for low standby power devices.

B. Sub-threshold Leakage Current

The subthreshold current is the drain-source current of an OFF transistor. This is due to the diffusion current of the minority carriers in the channel for a MOS device operating in the weak inversion mode (i.e., the subthreshold region.) For instance, in the case of an inverter with a low input voltage, the NMOS is turned OFF and the output voltage is high. Even when V_{GS} is 0V, there is still a current flowing in the channel of the OFF NMOS transistor due to the V_{DD} potential of the VDS. The magnitude of the subthreshold current is a function of the temperature, supply voltage, device size, and the process parameters, out of which, the threshold voltage Vth plays a dominant role.

In current CMOS technologies, the subthreshold leakage current is much larger than the other leakage current components. This current can be estimated by using the following equation [6], [3].

$$I_{DS} = K\left(1 - e^{-V_{DS}/V_T}\right) e^{(V_{GS}-V_T+\eta V_{DS}/\eta V_T)} \quad (3)$$

Where K is functions of the technology, and η is the drain-induced barrier lowering coefficient. Decreasing the threshold voltage increases the leakage current exponentially. The equation for subthreshold current indicates that it depends exponentially on Vth, V_{DS} and V_{GS}. Therefore it is a function of the terminal voltages, V_D, V_B, V_S and V_G. This means that to know subthreshold leakage of a device the biasing condition should be known or by controlling the terminal voltages the subthreshold leakage can be controlled. In fact decreasing the threshold voltage by 100mv increases the leakage current by a factor of 10. Decreasing the length of transistors increases the leakage current as well. Therefore, in a chip, transistors that have smaller threshold voltage and/or length due to process variation, contribute more to the overall leakage. Although previously the leakage current was important only in systems with long inactive periods (e.g., pagers and networks of sensors), it has become a critical design concern in any system in today's designs.

From (1) for tunneling current it can be observed that tunneling current increases exponentially with a decrease in oxide thickness as well as V_{ox}. The latter depends on the biasing condition which is related to gate topology and input signal. Therefore input pattern of each gate affects the subthreshold as well as gate leakage current. The leakage of transistors in a stack is a function of no. of transistors and input pattern.

3. Stack Effect

Subthreshold current depends exponentially on V_T, V_{DS} and V_{GS} [2]. Therefore it is a function of the terminal voltages, V_D,V_B,V_S and V_G. This means that to know subthreshold leakage of a device the biasing condition should be known or by controlling the terminal voltages the subthreshold leakage can be controlled.

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Source biasing is the general term for several techniques that change the voltage at the source of a

transistor. The goal is to reduce V_{GS}, which has the effect of exponentially reducing the subthreshold current. Another result of raising the source is that it also reduces V_{BS}, resulting in a slightly higher threshold voltage due to the body effect. Circuits that directly manipulate the source voltage are rare, and those that exist usually use switched source impedance or a self-reversed biasing technique

Probably the simplest example of source biasing occurs when "off" transistors are stacked in series. Conceptually, the source voltage of the upper transistor will be a little higher than the source voltage of the lower transistors in the stack. Hence V_{GS} of upper transistor is negative, V_{BS} is negative resulting in increase in threshold voltage and V_{DS} is also lower. Due to this, the leakage of upper transistor reduces [4], [18]. This reduction is called stack effect. But this reduction in leakage comes at an increase in delay performance. The reduction in leakage due to stack effect can lead to increase in delay and hence can be used in situations where this delay can be tolerated or by using gates with natural stack [13].

The leakage in gates is state dependent as subthreshold leakage and gate leakage of a MOS device is dependent on the terminal voltages.

A. Simulation setup

To reduce leakage in a circuit with the use of the source biasing we observe the behavior of gate and subthreshold leakage in a stack over different technologies and biasing conditions, we perform certain simulations using the latest predictive technology models of 130nm,90nm ,65nm and 45nm technology. The models for sub-threshold leakage and gate tunneling leakage are used to understand the dependence of these leakage currents on the different parameters and to understand the mechanism.

Here we use Aim-spice simulator for the BSIM4 models to obtain leakage currents for the transistors with different input signals. The results are stored in several tables containing the leakage of each gate for a given input pattern.

B. Predictive technology models (PTM)

Berkeley Predictive Technology Model (BPTM) [19] are developed based on BSIM4 [14]. BPTM includes more physical parameters into the prediction. Their values were empirically fitted from published data of early stage experiments. BPTM models are empirical in nature and model file for each technology node is empirically fitted. The overall trend of scaling is not smooth by BPTM and increasingly significant intrinsic correlations among physical parameters are not sufficiently considered.

Further new generation of PTM is developed that overcomes these limitations. First, new physical models are employed in the prediction to correctly capture first-order correlations among model parameters. These additional models include Vth_0 dependence on N_{ch}, low field mobility degradation, and velocity overshoot. Based on comprehensive studies of published data over various technology generations, the scaling trend of key physical parameters are concluded, such that both nominal and variation transistor performance are predicted with a guaranteed confidence. Through this new approach, smooth and accurate predictions are obtained from 130nm to 45nm nodes. The PTM models can be customized using ten parameters. These first order parameters are critical to determine the behavior of MOS devices during technology scaling.

4. Estimation and Analysis of Leakage Current in a Stack

To estimate the total gate current in the stack we observe the gate current flowing from the primary inputs to the gates of transistors in the circuit.

The total gate leakage in a stack is expressed as

$$I_{gate} = \sum |I_{gk}| \quad (3)$$

The total leakage in the stack is given as

$$I_{leak} = I_{sn} + \sum (1 - V_{gk}) |I_{gk}|$$

$$= I_{VDD} + \sum (1 - V_{gk}) |I_{gk}| \quad (4)$$

Subthreshold current is expressed as

$$I_{sub} = I_{leak} - I_{gate} \quad (5)$$

Power dissipation is given as

$$P = V_{DD} . I_{leak} \quad (6)$$

A. Leakage behavior in a stack of 3 NMOS transistors

The stack behavior is observed with the four predictive technologies using models such as 130nm, 90nm, 65nm and 45nm for a stack of 3 transistors as shown in Fig. 1

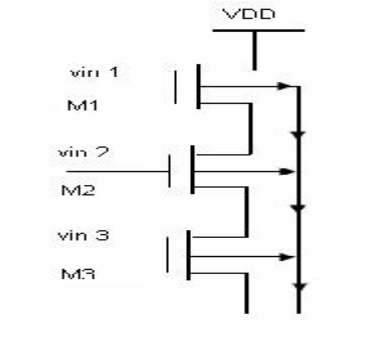

Fig.1 Stack of 3 NMOS transistors M1, M2 and M3.

Input vector vs. leakage currents in 130nm, 90nm, 65nm, 45nm technologies using a stack of 3 NMOS transistors (models used: PTM v1.0) (Toxe(130)=2.2.5nm; Toxe(90)=2.05nm ;Toxe(65)=1.85nm ;Toxe (45) =1.75nm) are shown in figure 2, 3 and 4.

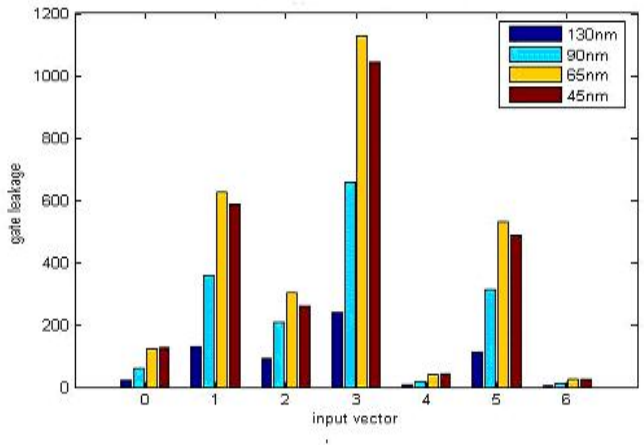

Fig.2 Comparison of Sub threshold leakage current of Nano technology NMOS stack for different input vectors.

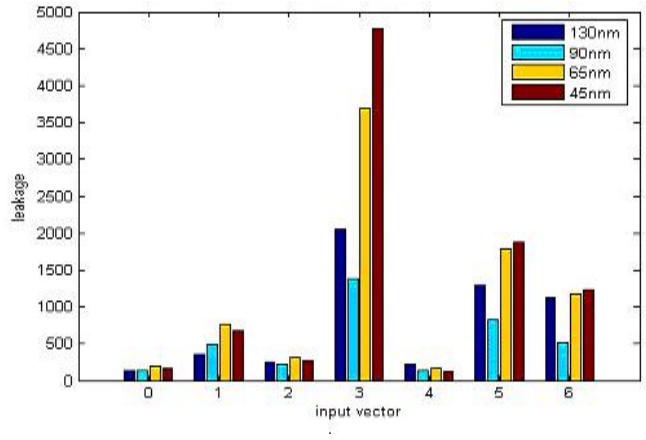

Fig.3 Comparison of Gate leakage current of Nano technology NMOS stack for different input vectors.

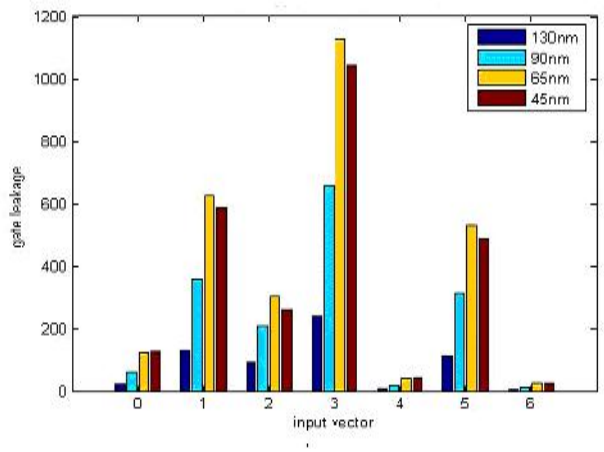

Fig.4 Comparison of Total leakage current of Nano technology NMOS stack for different input vectors.

Table I shows the Input vector required for minimum leakage currents.

Table I: Minimum input vector of 4 Nano NMOS stack for sub threshold leakage, gate leakage and total leakage current.

Leakage current	**Technology used**			
	130 nm	90 nm	65 nm	45 nm
I_{sub}	“000”	“010”	“010”	“010”
I_{gate}	“110”	“110”	“110”	“110”
I_{total}	“000”	“000” “100”	“100”	“100”

Total Sub threshold and gate leakage v/s input vector in a stack of 4-NMOS transistor are shown in fig.5.

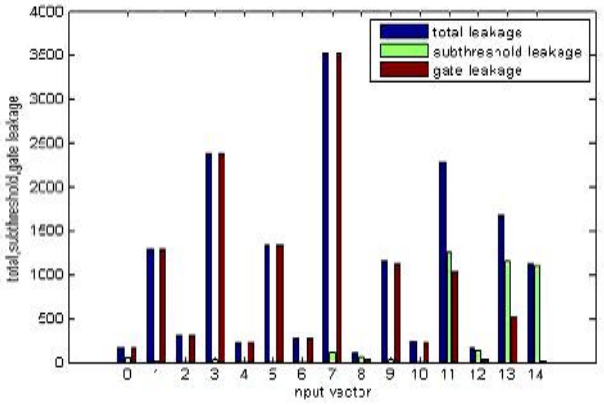

Fig.5 Sub threshold and total leakage variation with input vector in a stack of 4 NMOS transistors (65 nm.)

5. Simulation Results

Following table shows the subthreshold, gate and total leakage current variation for different minimum input vectors applied to Stack of four NMOS transistors.

Table II: subthreshold leakage, gate leakage and total leakage variation with input vector in a stack of 4 NMOS transistor (Technology node: 65 nm).

Leakage Current	**Minimum Leakage Vector**
Isub	*0010, 0100, 0101, 0110, 1010*
Igate	*1110*
Itotal	*1000*

Gate, drain or source voltage (either 1 or 0) is used to denote region of operation or state of each transistor in the stack as shown in fig. 1. Different states of transistors are shown in fig. 6

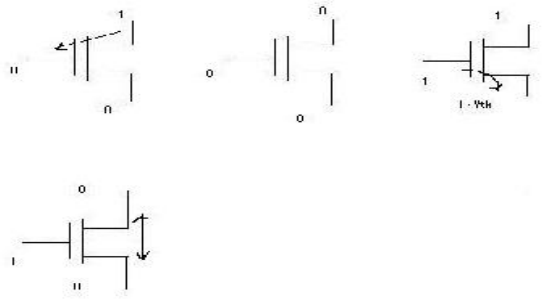

Fig.6 Four different states (in terms of gate, drain and source voltages) for a transistor in a stack.

Table III (A): Leakage analysis of a 3 NMOS Nano transistor stack

Transistor In Stack	**Input Vector**			
	000	001	010	011
M1	*State 010 Igdo Leakage*	*State 010 Igdo Leakage*	*State 010, Igdo Leakage*	*State 000, Gate Leakage is negligible*
M2	*State 000 Gate Leakage is negligible*	*State 000, Gate Leakage is negligible*	*State 100 Contribute to gate Leakage*	*State 100, Contribute to gate Leakage*
M3	*State 000 Gate Leakage is negligible*	*State 100, Contribute to gate Leakage*	*State 000, Gate Leakage is negligible*	*State100, Contribute to gate Leakage*

Table III (B): Leakage analysis of a 3 NMOS Nano transistor stack.

Transistor In Stack	**Input Vector**		
	100	101	110
M1	*State 11'1', very small gate Leakage*	*State 11'1', very small gate Leakage*	*State 11'1', very small gate Leakage*
M2	*State 010, Gate Leakage is low*	*State 000, Gate Leakage is negligible*	*State 11'1', very small gate Leakage*
M3	*State 000, Gate Leakage is negligible*	*State 11'1', very small gate Leakage*	*State 010, Gate Leakage is low*

Reverse tunneling gate leakage is comparatively smaller than forward tunneling leakage because it includes only gate to source (Igso) and gate to drain overlap (Igdo) current. Using 3 NMOS transistor stack structure in Fig.1,

A. "000" INPUT:

Intermediate nodes have a small voltage. Subthreshold leakage is not high as Vgs is negative for all the transistors.

B. "001" INPUT:

Subthreshold increases slightly due to one 'on' transistor.

C. "010" INPUT:

Gate leakage of M2 charges the intermediate nodes. This reduces gate and subthreshold leakage. But as subthreshold leakage is exponentially dependent on Vgs it reduces more significantly due to the negative Vgs of M2.

D. "011" INPUT:

Subthreshold leakage is high due to the two transistors being 'on' and also having a direct path to ground. Gate leakage is high due to M2 and M3.

E. "100" INPUT:

Subthreshold leakage is almost same as that with input "001". Gate leakage contribution is low.

F. "101" INPUT:

Subthreshold leakage is high due to the two 'on' transistors but less than the subthreshold current with input vector "110" as only M1 has a path to ground.

G."110" INPUT:

Subthreshold leakage is high due to 'on' transistors but as there is no path to ground from leaky transistors, M1 and M2, it is less than the current due to input vector "011".

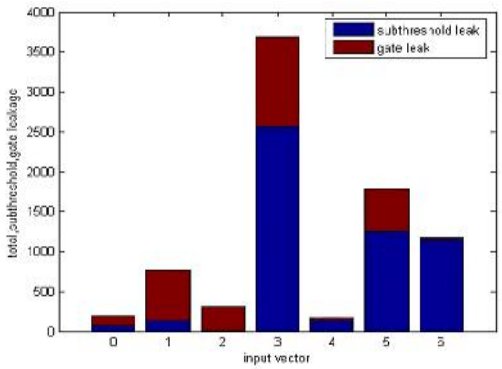

Fig.7 Contribution of gate leakage and sub threshold leakage in total leakage for a stack of 3 NMOS Nano transistors (Technology node: 65 nm).

The Fig.7 shows the contribution of gate leakage and subthreshold leakage in total leakage current for different input vectors

The behavior of subthreshold leakage and Gate leakage for different input vectors in different condition are discussed as follows:

CASE I: Subthreshold leakage is dominant than gate leakage (130nm)

a) Subthreshold is observed to be the lowest in the case when maximum no. of transistors are off. As shown in Fig. 2, for a stack of 3 transistors: Minimum input vector is "000".

b) Gate leakage is observed to be the lowest when all transistors in the stack except the one connected to ground are ON. As shown in Fig. 3, for a stack of 3 transistors: Minimum input vector is "110" but subthreshold leakage increases substantially.

c) The total leakage (subthreshold leakage + gate leakage) is reduced when the maximum no. of transistors are off as the dominating leakage component i.e. subthreshold leakage is dependent on it and hence for a stack of 4 transistors, the minimum leakage vector is "0000".

CASE II: Gate leakage is dominant than subthreshold leakage (90nm, 65nm, 45nm)

a) Subthreshold is observed to be the lowest when one or more of the intermediate transistors (i.e. with drain and source both connected to the intermediate nodes of the stack) which are not connected to ground through another conducting transistor are ON. This is due to the fact that gate leakage current charges the intermediate node voltage and hence leads to reduction in subthreshold leakage current and gate leakage current. As shown in Fig 1, for a stack of 3 transistors, the minimum input vector is "010".

b) Gate leakage is observed to be the lowest when all transistors except the one connected to ground are on. As shown in Fig. 2, considering the gate leakage minimum input vector is "110" but subthreshold increases substantially as it is dependent on the no of 'ON' transistors in the stack

c) The total leakage (subthreshold leakage + gate leakage) is reduced when the input vector is "100".Gate leakage is minimum with the input vector "110" but the reduction is only slightly less than that obtained by "100".On the other hand the subthreshold which depends on the number of 'ON' transistors increases substantially with "110" and offsets the reduction in gate leakage. Hence considering this, input vector "100" which reduces gate leakage without significantly increasing the subthreshold current is found to be the best solution for reduction in total leakage. As shown in Fig. 4 and Fig. 5, applying input vector "1000" or "100" for a four transistor and three transistors stack reduces leakage as this combination reduces gate leakage and subthreshold leakage, whereas in case of a 2 transistor stack the minimum leakage vector will be "00".

6. Conclusion

This paper analyzes the growing impact of leakage power in submicron technologies. It focuses on two important leakage mechanisms in scaled technologies. There have been many works on subthreshold leakage and techniques to reduce it. But as Tox is scaled down below 2nm in the new generation technologies, both the leakages, gate leakage and subthreshold leakage have to be addressed together. The leakage currents are therefore analyzed considering their effects on the two leakage mechanisms.

Circuit level techniques incorporated requiring support from technology and process level techniques can be more effective in reducing leakage. There cannot be a single technique that will guarantee the best leakage power reduction. There are delay and area overheads and also the cost of minimum leakage vector application depends on the previous state of the circuit and time for which it will remain in standby mode. Hence the future work can be collaborating the circuit level techniques with technology dependent circuit level techniques and process level techniques.

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