

Leakage Current Analysis of FinFET Based 7T SRAM at 32nm Technology

Dr. Chhavi Saxena,

Associate Professor, Department of ECE, Maharana Pratap College of Technology, Gwalior, Madhya Pradesh
vlsi.chhavi@gmail.com

Abstract— FinFETs can be a replacement for bulk-CMOS transistors in many different designs. Its low leakage/standby power property makes FinFETs a desirable option for memory sub-systems. Memory modules are widely used in most digital and computer systems. Leakage power is very important in memory cells since most memory applications access only one or very few memory rows at a given time. As technology scales down, the importance of leakage current and power analysis for memory design is increasing. In this paper, we discover an option for low power interconnect synthesis at the 32nm node and beyond, using Fin-type Field-Effect Transistors (FinFETs) which are a promising substitute for bulk CMOS at the considered gate lengths. We consider a mechanism for improving FinFETs efficiency, called variable-supply voltage schemes. In this paper, we've illustrated the design and implementation of FinFET based 4x4 SRAM cell array by means of one bit 7T SRAM. FinFET based 7T SRAM has been designed and analysis have been carried out for leakage current, dynamic power and delay. For the validation of our design approach, output of FinFET SRAM array have been compared with standard CMOS SRAM and significant improvements are obtained in proposed model.

Keywords— FinFET; 7T SRAM Cell; leakage current; Delay.

I. INTRODUCTION

As nanometer process technologies have advanced chip density and operating frequency have increased, making power consumption in battery-operated portable devices a major concern. Even for non-portable devices, power consumption is important because of the increased packaging and cooling costs as well as potential reliability problems. Thus, the main design goal for VLSI (Very-large scale integration) designers is to meet performance requirements within a power budget.

Recently, new multi-gate or tri-gate architectures, also known as FinFET technology, deliver superior levels of scalability; design engineers face significant challenges in creating designs that optimize the promise of this exciting new technology. Design metrics including performance, power, area, cost and time to market have not changed since the inception of the integrated circuit (IC) industry.

In fact, Moore's law is all about optimizing those parameters by driving to the smallest possible transistor size with each new technology generation. However, as process technologies continued to shrink towards 20-nanometers (nm), it became impossible to achieve a similar scaling of certain device parameters, particularly the power supply voltage, which is the dominant factor in determining dynamic power. Additionally, optimizing for one variable such as performance automatically translated to unwanted compromises in other areas like power. Given the new emerging metric of performance per unit power (Koomey's law), one major design optimization alternative designers have in FinFETs, as compared to planar technology, is much better performance at the same power budget, or equal performance at a much lower power budget.

Today's chips consist of billions of transistors and design teams strive for "better, sooner, cheaper" products with every new process node. However, as feature sizes have become finer, the perils of high leakage current due to short-channel effects and varying dopant levels have threatened to derail the industry's progress to smaller geometries. The FinFET transistor structure promises to rejuvenate the chip industry by rescuing it from the short-channel effects that limit device scalability faced by current planar transistor structures. Leading foundries estimate the additional processing cost of 3D devices to be 2% to 5% higher than that of the corresponding Planar wafer fabrication. FinFETs are estimated to be up to 37% faster while using less than half the dynamic power or cut static leakage current by as much as 90%.

FinFETs also promise to alleviate problematic performance versus power tradeoffs. Designers can run the transistor faster and use the same amount of power, compared to the planar equivalent, or run them at the same performance using less power. This enables design teams to balance throughput, performance and power to match the needs of each application. Therefore multi gate FETs are expected to advantageous in terms of gate length scaling and leakage. FinFET seems to be promising candidate to be applied in the next generation SRAM technology due to its superior scalability for a given gate insulator thickness, higher channel mobility, absence of random dopant fluctuation effects without compromising its performance.

A FinFET uses an intrinsic body. It greatly suppresses the device-performance variability caused by the fluctuation in the number of dopant ions, while planar- bulk MOSFET requires a heavily doped channel which causes serious process variability. It is preferable to extend standard cell SRAM ability by effectively taking advantage of the FinFET-based technology together with the novel circuit technique. FinFET is suitable for future nanoscale memory circuit design due to its reduced Short Channel Effects (SCE) and leakage current. FinFET SRAM cells can reduce area and leakage power. Data stability can be enhanced by dynamically adjusting the threshold voltage of access transistors. Furthermore its ability to operate at much lower supply voltage extended voltage scaling which was levelling off and allowed further badly needed static and dynamic power savings.

Voltage supply is connected to the SRAM cell. This technique maintains the lower supply and threshold voltages although reducing leakage and leakage power dissipation. Stacking effect is produced by additional transistor in combination with the SRAM cell transistors when the gated-transistor is turned off. These techniques have been used to reduce leakage in FinFET-based 7T SRAM cell using cadence virtuoso tool in 32nm technology.

The simulated result is compared with the CMOS technology using SRAM cell. An overview of this paper is organized as follows: Section II shows a detailed structure of a proposed FinFET 7T SRAM cell. Section III describes the leakage reduction techniques and its effects on leakage current. We analyze the comparative CMOS and FinFET simulation results in Section V. The final section draws the conclusions of this work.

II. 7T SRAM CELL DESIGN USING FINFET STRUCTURE

A SRAM cell is proficient of holding a data bit so long as the power is applied to the circuit. A double-gate FinFET SRAM cell design is a better choice due to self-alignment. As technology scales down, while dealing with short- channel effects (SCEs), not only very ultrathin to keep the current drive is required but also very low is required to maintain the device speed and variations under control [1] as this effect can degrade the devices subthreshold slope and cause changes in the threshold voltage.

The subthreshold current generally occurs when the gate-to-source voltage of transistors is less than the threshold voltage. When the current flows from the gate through the oxide layer to substrate, this current is called gate leakage current. As we go down below 65 nm technology, there seems to be no viable options

of continuing forth with the conventional MOSFET. Therefore, multigate FETs such as planar double-gate FETs and FinFETs have been proposed for low-power digital CMOS technologies to reduce leakage reduction.

In this paper, 7T SRAM cell using FinFET technology is proposed also some circuit level techniques has been imposed to reduce leakage current. There are different types of leakage reduction techniques. One is the multi-threshold leakage reduction technique [2] which uses high threshold PMOS and NMOS acting as a switch to disconnect power supply during standby mode thereby reducing leakage. This technique provides increased operating speed by low-threshold MOSFET and reduced leakage by high-threshold voltage. Another technique is gated [3] in which an NMOS transistor with gated alignment of opposite sides of gates and the fabrication compatibility with the existing standard CMOS technology [7], [8]. The FinFET SRAM cell structure is a better choice due to self-alignment of opposite sides of gates and the fabrication compatibility with the existing standard CMOS fabrication technology. Memories having shorter access time and low power dissipation are generally required so that FinFET based SRAM cells become popular due to the low power dissipation.

The 7T SRAM cell that stores one bit of information is shown in figure1. The cell consists of two FinFET [4] inverters where the output of each is fed as input to other; this loop stabilized the inverters to their respective state. The access transistor and the word line (WL) and bit line (BL) are used to write and read, to and from the cell. In the standby mode the access transistors turn to off by making the word line low [5]. The inverter will be complementary in this state. The PMOS of the left inverter is turned on, the output potential is high and the PMOS of the second inverter is switched off. The gates of the transistor that connect the bit line and the lines of the inverter are driven by the word line. If the word line is kept low the cell is disconnected from the bit lines. It has one additional transistor compared with the standard 6T SRAM cell but operates and consumes much less leakage power.

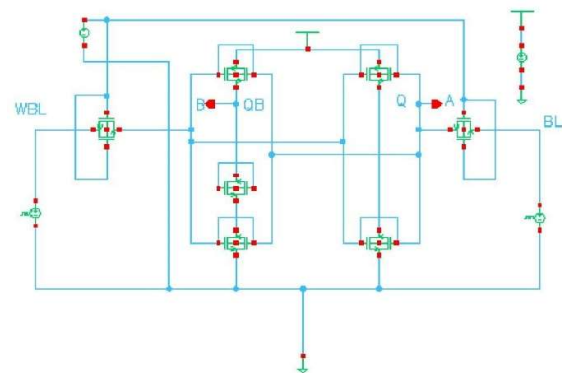


Figure 1. 7T FinFET based SRAM Cell Design

III. EFFECT ON LEAKAGE CURRENT AND ITS REDUCTION TECHNIQUES

Leakage current becomes a great issue in deep submicron CMOS technology consisting of three major components. They are junction-tunneling leakage, subthreshold leakage and gate leakage.

The Subthreshold leakage is the drain-source of a transistor operating in the weak inversion region. Contrasting the strong inversion region in which the drift current dominates, the sub-threshold conduction is due to the diffusion current of the minority carriers in the channel for a MOS device. The magnitude of the sub-threshold current is a function of the temperature, supply voltage, device size and the process parameters out of which the threshold voltage (V_T) plays a dominant role [6]. I_{SUB} can be calculated by using the formula:

$$I_{DS} = K \{1 - e^{-(V_{DS}/V_T)}\} e^{(V_{GS} - V_T + \eta V_{DS})/\eta V_T}$$

Where K and n are functions of the technology, and η is the drain-induced barrier lowering coefficient. Figure 2 shows the comparative study of leakage currents at variable supply voltage. It clearly shows that FinFET SRAM has small leakage current.

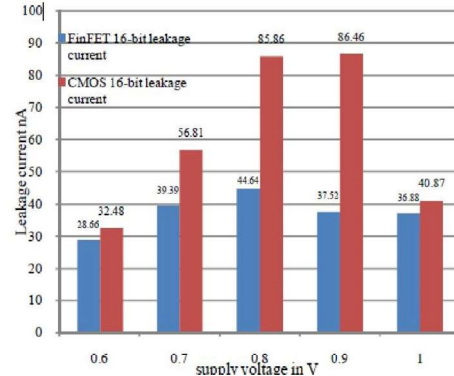


Figure 2. Comparison of Leakage current between the CMOS and FinFET SRAM cells

3.1 Leakage Reduction Techniques

(A) Multi-Threshold Voltage Leakage Reduction Technique

In this scheme, a high threshold sleep control is connected in series with low circuit. This can be understood from fig.3. In active mode, sleep transistors must be on to provide the standard circuit functionality of SRAM cell, whereas, in standby mode, sleep transistors must be off in order to improve the leakage current.

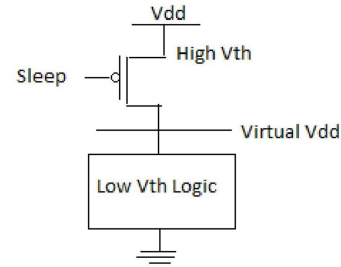


Figure 3. Multi-threshold voltage technique

Sleep transistor of high threshold must be used; otherwise leakage current will increase making this technique less effective so that low-threshold FinFET transistors are used in the SRAM cell logic and high-threshold transistor as sleepy transistor. High-transistors are used for low subthreshold current and low- transistors are used to improve the performance of the cell.

B) Gated Technique

Leakage associated with SRAM cell creates a major problem in chip designing because of large area. The leakage in cell can be reduced using gated- technique by contributing an extra transistor producing stacking effect [9]. This extra NMOS transistor produces greater impact on leakage current in conjunction with SRAM cell transistors. It happens because gated transistor becomes on in used portions and becomes off during unused portions in SRAM cell. Here, NMOS transistor is connected between ground and source region of NMOS transistors of the cell. Similarly, PMOS transistor can also be connected between the and source region of PMOS transistors in SRAM cell. Gated- transistor becomes on during active mode and switches to off state during standby mode. Leakage current due to this technique can be reduced by stacking effect produced which arises because of the three transistors present between the ground terminal and the bit lines (BL and BLB).

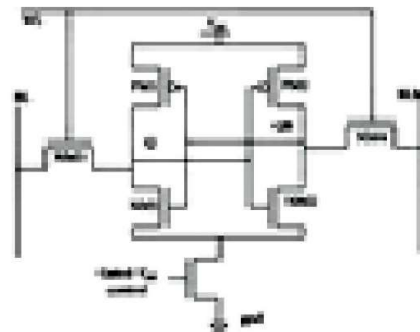


Figure 4. Gated technique

Transistor of adequate width must be used to provide isolation from leakage current during read cycle. During PMOS gated, insignificant area overhead and transistor width reduce because of no concern during read operation. So NMOS gated provides better control over the leakage than PMOS gated-. The gated technique is shown in Figure 4.

IV. SIMULATION RESULTS AND DISCUSSION

Table1 shows the comparative analysis of simulation results of leakage current of 7T FinFET SRAM cell using FinFET and CMOS technology using 32nm Cadence virtuoso tool.

TABLE I: Leakage Current Comparison of 7T SRAM Using CMOS & FinFET Technology

Leakage Current (nA)	7T SRAM Using CMOS Technology	7T SRAM Using FinFET Technology
0.6	32	25.6
0.7	55.9	36.8
0.8	82.6	40.67
0.9	85.3	30.8
1	88.9	76.6

From table 1, it is concluded that leakage current reduces remarkably in FinFET technology as compared to CMOS. It has been also observed that as supply voltage increases, leakage current also increases. So, for minimum leakage current, 0.6V power supply can be used.

V. CONCLUSION

In this paper, FinFET based 7T SRAM has been designed and analysis for leakage current has been carried out imposing leakage reduction technique. For the validation of our design approach of 7T SRAM, output of FinFET 7T SRAM has been compared with standard CMOS 7T SRAM for 32nm technology and significant improvements are achieved in proposed model.

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