International Journal of Electrical & Electronics Research. (IJEER)
Volume 3, Issue 3, Pages 66-69, September 2015, ISSN: 2347-470X

Comparative Analysis of Low Power and Low Leakage Reduction for Logic Circuits

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ABSTRACT

As technology scales in nanometer regime leakage current are becoming important metric of comparable importance to leakage current for the analysis and design of complex logic circuits. In this paper, we did the comparative analysis of leakage current for carry look ahead logic circuits. The simulation results depicts that the proposed design leads to efficient in terms of standby leakage power. We have performed simulations using Cadence Spectre 90nm standard CMOS technology at room temperature with supply voltage of 1V.

Keywords - Low Power, Low Leakage, Leakage Power, Power Gating.

1. INTRODUCTION

It's no secret that power is emerging as the most critical issue in system- on-chip (SoC) design today. Power management is becoming an increasingly urgent problem for almost every category of design, as power density-measured in watts per square millimeter rises at an alarming rate. The power density trend versus power design requirements for modern SoCs is mapped in figure 2. The widening gap represents the most critical challenge that designers of wireless, consumer, portable, and other electronic products face today.
The traditional approach of scaling supply voltage for low-power applications becomes less energy efficient as technology continues to scale down. This is because leakage power is becoming more prominent and in low-power applications with a high standby-to-active ratio, it may become the dominant part of the total power consumption. Several methods have been developed to reduce the active energy of logic circuits. [1][2][15].

Multi-threshold CMOS (MTCMOS) is widely used to significantly suppress leakage currents in standby mode [4], [5]. In this technique, a sleep transistor is added between the actual ground rail and circuit ground (called virtual ground). This device is turned off in the sleep mode to cutoff the leakage path through the stack effect [6].In this paper, power gating technique for low leakage and low power techniques has been compared. Section II explains the power gating approach and its consequences on leakage reduction. Section III discusses the comparative results and finally the paper is concluded in section IV.

2. POWER GATING TECHNIQUES

Power gating approach is very effective in leakage power reduction. Up to yet various techniques have been introduced and implemented for reducing leakage but no great success has been get. And still the leakage is a big deal for technology below 45nm.

Power gating is a technique where in circuit blocks that are not in used are temporarily blocked. Power gating technique is widely used to significantly suppress the leakage currents in standby mode. In this technique, a sleep transistors of high threshold (VTH) voltage are added between the actual ground rail and circuit ground (virtual ground). This device is turned off in the sleep mode to cutoff the leakage path from ground. This scheme is effective because gating the power supply causes virtual ground rail to charge up close to supply voltage VDD, which suppresses the leakage current. However, when the virtual ground rail is restored to its nominal value, there is a potentially significant "wake-up" penalty associated with discharging the virtual ground rail capacitance back to ground. In the conventional power gating as shown in figure.3, the transition of sleep mode to active mode makes the sleep transistor turn ON in saturation. Instantaneous discharge through the sleep transistor operating in saturation region creates current surge at sleep/ active mode change and causes high ground bounce noise [3] – [10].

MOSFETS in this scheme during the standby mode the sleep transistors are turned off, and the diodes clamp the supply voltage to a reduced value of (Vdd-2 Vth diode). As

opposed to power gating scheme, VRC can maintain state retention in the storage elements and can eliminate the state restoration procedures that cause performance degradation. A better solution is proposed in [10] by adding only a single built in pMOSFETs to a conventional power gating scheme. It has been claimed that this scheme supports an additional intermediate power savings mode as well as power cut off mode. In the intermediate mode, leakage reduction and data retention are realized and the magnitude of power supply voltage fluctuations during power- mode transitions is reduced. The analyzed circuit generates multiple sleep modes by controlling the steady state virtual ground rail potential. The analyzed circuit generates multiple sleep modes by controlling the steady state virtual ground rail potential. The virtual ground potential, in turn, is controlled by the gate voltage of the sleep transistor during sleep mode. However, this mechanism will require additional control circuitry, which will incur much higher area and performance penalties on the overall system as compared to other power gating and related schemes.

2.1 Stacking Power Gating Approach

In this technique, the leakage current is reduced by the stacking effect, turning both MSL1 and MSL2 sleep transistors off. Here, we apply the SELECT input in a manner by which the ground bounce noise is minimum. This is achieved by adjusting the value of ΔT (this is the delay introduced to the SL signal using delayed buffer) which gives the summation of ground bounce noises of these two transistors minimum. When the value of ΔT is half of the oscillation period of the ground bounce noise then the positive peak of the ground bounce noise superimposes with the negative peak thereby bringing it closer to zero. This approach works on strategies (a) Reduction of leakage current by stacking effect [15].

In this, the leakage current is reduced by turning OFF both sleep transistors M1 and M2. This raises the intermediate node voltageVGND2 to positive values due to small drain current. An additional delay is inserted, between sleep and active mode to further reduce the ground bounce noise. During sleep to active mode transition, transistor M1 is turned ON and transistor M2 is turned ON after a small duration of time T1. The logic circuit is isolated from the ground for a short duration as the transistor M2 is turned OFF. This reduces the leakage current significantly by controlling the intermediate node voltage VGND2 and operating the transistor M2 in triode region.

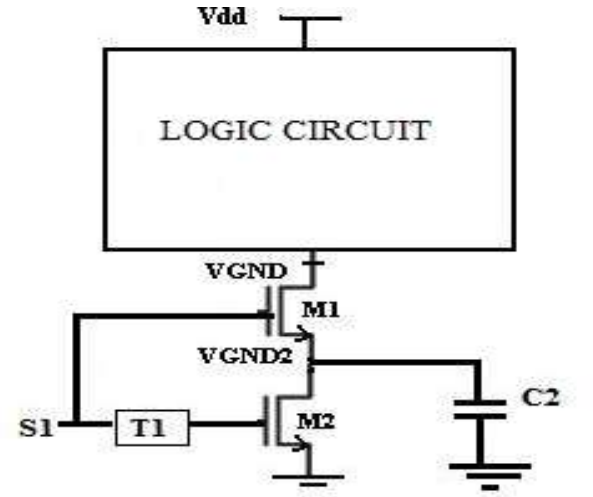

Figure 1 Stacking Power gating Approach

2.2 Diode based stacking power gating approach

If we incorporate the strategy which is operating the sleep transistor as a diode in stacking power gating approach leads diode based stacking power gating [15]. Stacking sleep transistors (T1, T2) are used in diode based stacking power gating scheme shown in fig.2 reduce the magnitude of peak current and voltage glitches in power rails i.e. ground bounce noise. The diode based stacking power gating scheme consists of 5 parts:

Transistors T1, T2 are the sleep transistors which are high Vt transistors for less leakage current, transistor S1 is a control transistor used to make the sleep transistor S1 working as a diode during mode transition, TG1 is the transmission gate, Tn time delay provided for T1 and T2 and C2 is the capacitor inserted in the intermediate node VGND2.

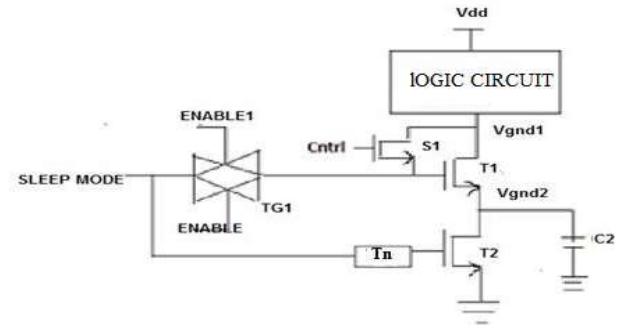

Figure 2: Diode based Stacking Power Gating Approach

3. COMPARATIVE RESULTS

In this paper we did the comparative analysis of power gating approach for 4-bit carry look ahead adder circuit. The simulation was done with the help of cadence spectre 45nm at room temperature with supply voltage 0.7V. The detailed simulation setup used was:

1) Tool – Cadence
2) Module – Virtuoso Analog Design Environment
3) Simulator – Spectra
4) Technology – 45nm
5) Technology File – gpdk045
6) Power supply – 0.7V.

3.1 Standby Leakage Power

In this section, we evaluated the standby leakage current of carry look ahead adder circuit. All the results for leakage current calculation have been simulated under the condition that the all logical inputs of circuit are held at logic '0' and carry signal Cin, propagate carry P and generate carry G are held at logic '1'. Table1 shows standby leakage current comparison of different power gating approaches. Effect of voltage scaling is analyzed. The result shows that diode based stacking power gating approach reduces the most standby leakage current. Dependence of standby leakage current on temperature has also been evaluated and is shown in table 2. As temperature increases from 27 ºC to 100 ºC standby leakage current also increases. Table 2 clearly shows that diode based stacking power gating reduces the most standby leakage current.

Table 1: Effect of supply voltage scaling on leakage current for 4-bit CLA Adder

Supply V. (V)	0.7	0.6	0.5	0.4	0.3	0.2	0.1
Stacking Power Gating	20.5	19.89	17.65	17.01	14.32	13.29	11.99
Diode Based Stacking	18.9	14.97	14.29	12.96	11.99	10.09	8.35

So from the analysis results studied from table 1 and 2 we analyzed that diode based technique is best as the leakage reduction is most as compared to other.

Table 2: Effect of temperature on standby leakage power

Temp.	27°c	75°C	100°C
Stacking Power Gating	20.5	250.95	555.7
Diode Based Stacking	18.9	200.91	430.92

4. CONCLUSIONS

Standby leakage current for stacking power gating, diode based stacking power gating approaches is evaluated in this paper. Use of transistor stacking, diode based stacking, cluster sizing reduces standby leakage current with considerable amount. Effect of temperature on standby leakage current for different power gating approaches for high speed 4- bit carry look ahead adder circuit have been also analyzed in this paper.
A stacking power gating approach has been presented which reduces standby leakage current. It has been evaluated that this approach reduces standby leakage current by 89.8%. In diode based stacking power gating technique effect of stacking, diode connected to stacking on standby leakage current, has been evaluated. Diode based stacking power gating technique reduces standby leakage current up to 90.7% as on compared with conventional mode.

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