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Investigation analysis of open circuit and short circuit fault on cascaded H-bridged multilevel inverter using artificial neural network approach

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ABSTRACT- Cascaded H-bridge multilevel inverters are becoming increasingly used in applications such as distribution systems, electrical traction systems, high voltage direct conversion systems, and many others. Despite the fact that multilevel inverters contain a large number of control switches, detecting a malfunction takes a significant amount of time. In the fault switch configurations diode included for freewheeling operation during open-fault condition. During short circuit fault conditions are carried out by the fuse, which can reveal the freewheeling current direction. The fault category can be identified independently and also failure of power switches harmed by the functioning and reliability of cascaded H-bridge multilevel inverters. This paper investigates the effects and performance of open and short switching faults of multilevel inverters. Output voltage characteristics of five level MLI are frequently determined from distinctive switch faults with modulation index value of 0.85 is used during simulation analysis. In the simulation study, with the modulation index value of 0.85, one second open and short circuit faults are generated for the location of the defective switch. Fault is identified automatically by means of artificial neural network technique using sinusoidal pulse width modulation based on distorted total harmonic distortion and managed by its own. The proposed topology is to be design and evaluate using MATLAB/Simulink platform.

Keywords: Artificial Neural Network, Fast Fourier Transform, Multilevel inverter, Sinusoidal Pulse Width Modulation, Total Harmonic Distortion

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1. INTRODUCTION

Multilevel inverters have aroused huge attention in the examination of established manufacturing electric drive organizations in recent days, with the intention of reaching their power quality as well as demands. The elimination of harmonic distortion ripples in the output voltage pattern by increasing level capacity, as well as the portability of battery packs or fuel including in intervals, are two of the most important advantages of multilevel inverters. Despite the fact that MLIs are an established technology that may be used in engineering applications, the failure of power electronic switches and fault analysis is a new research issue for researchers. It's used in engineering to check the condition of power switches in inverters. The number of levels in the inverter changes, as does the number of additional switching devices, raising the possibility of each of the power switches collapsing. As a result, therefore any issue should be handled right away so that the drive and motor operations are not accepted under abnormal scenarios. To improve system reliability, an effective problem diagnosis system must be implemented.

Jahan HK et al. [1] had investigated in both moderate and high-power applications of multilevel converters which play a significant role. Multi-level inverters come in three typical configurations: diode clamped, flying capacitor, and cascaded H-bridged. The modular design of cascaded-H bridged multilevel inverter characteristics and performance are used to achieve medium voltage and high-performance characteristics. Short and open circuit faults are two types of failures which can occur in power switching devices in CHB-MLI. Short circuit problems mostly damage, so protection from short circuit is required. ANN approaches for short circuit protection by using high potency fuses and de-saturation method. Haji-Esmaeili MM et al. [2] had analyzed open-circuit faults in power switches the device shutting down, and they can go undetected for a long time. This could cause secondary defects in the inverter or other drive components, culminating in the entire system being shut down and expensive repairs.

Jalhotra M et al. [3] had investigated short-circuit faults in power electronic switches, on the other hand, are extremely

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damaging and necessitate special precautions to automatically shut down the entire drive. These types of failures must be identified and repaired in a microsecond in order to safeguard analogous semiconductor devices from damage in the converter leg. On the other perspective, extended open circuit fault behavior of the power converters might cause the entire system. Expertise in fault behaviors, fault prediction, and fault diagnostics will be necessary to keep the multilevel inverter system functioning smoothly. The position of faults is identified by an algorithm which was developed by Amini J et al. [4]. Babaei E et al and Ezhilvannan P et al [5-6], the open circuit (OC) fault can be caused by a number of factors, including a damaged inner wire, a transient short-circuits, or a gate driver failure. Over-voltage, over-current, safety component failure, and improper gating signal are some of the causes of short circuit (SC) failure. Suresh K et al. [7] investigated a number of recent articles on problems such as the creation of inverted pulse width modulation (PWM) method in CHB-MLI systems. Kiran Kumar G et al. [8, 9] has analyzed fault analysis in inverter and also faults an inverter device is used continuously under abnormal settings, further issues will arise, resulting in severe consequences. The device voltage and current of a multilayer inverter might vary based on the part and location of the faults. Some research concentrates on the device output current or voltage to assess fault form and position more quickly and easily, and then used the sample to expand a number of fault diagnosis techniques. Owing to the dangerous effects of short circuit faults on converter circuits, this type of fault must be detected as soon as possible. It is necessary to remember that certain circuit drivers are already in a position to detect defective switches. Hence considering the value of MV drives on the industry, robust detection mechanisms need to be discussed. Huang Z et al. [10] had investigated electrical drives and devices require complex electrical converters to conform to high power requirements. Multilevel inverter methods have also been tested as an approach to high and low voltage systems. Compared to traditional two-level inverters, multilevel inverters produce major output voltage and low harmonic output current distortion.

S. Khomfoi et al. [11] suggested an artificial-intelligence-based fault diagnostic and reconfiguration method for a cascaded H-bridge multilevel inverter drive (MLID). The MLID's output phase voltages are utilized as diagnostic signals for locate and detect faults. Since MLID platforms have several semiconductor switches and a nonlinear system complexity, diagnosing an MLID system using a mathematical model was difficult. As a result, the defect diagnosis of an MLID process was accomplished using a neural network (NN) categorization.

S. Srinivasan et al. [12, 13] had discussed Selective Harmonic Elimination (SHE) are the better way for achieving the desired fundamental component and for harmonic-free high - power applications.

The fundamental objectives of the proposed research effort are to develop a high-performance fault detection methodology for evaluating open and short circuit faults in MLI using enhanced signal processing and soft computing techniques. The fast Fourier transform (FFT) technique and ANN approach are used to evaluate the spectrum properties of output voltage wave forms produced using both modeling and experimental investigations at various fault situations. By using FFT technique, extract salient features such as total harmonic distortion (THD) and harmonic contents of output voltage signal at different fault cases. The performance characteristics of the FFT-ANN model-based fault detection approach for multilevel inverters can be compared to develop an effective fault diagnostic system. These concerns include the identification of switch faults and the monitoring of tolerances because parameters contribute to the reliability of the power converter systems. The validation of proposed model is implemented with the help of open and short circuit fault voltages and total harmonic distortion.

2. PROPOSED METHOD OF FAULT DIAGNOSIS SYSTEM IN MULTILEVEL INVERTER

Figure 1 illustrates literally the entire fault detection system set up for identifying defective power semiconductor switches in multilevel inverters, which includes both multilevel inverter and fault diagnosis system. The fast Fourier transform (FFT) approach was used to identify the properties of output voltage patterns. Frequency domain analyses of the terminal voltage patterns are required to construct a significant application assessment method. The FFT approach was used to retrieve distinct attributes from the output voltage signal. Despite the fact that a skilled feature extractor should supply critical data facts more about artificial neural network in the selected area, it was the highest degree of consistency reached within the adaptive intelligence network. Figure 2 depicts the signal separation of output voltage in terms of harmonics and RMS voltage output. The FFT provides a frequency response representation for any periodic or non-periodic signal. Figure 3 depicts one of the 11^{th} order sample harmonics, as well as THD and Vrms values, which are all utilized to extract characteristics from the output signal employing FFT analysis. The exact fault in open and short circuit faults is detected based on harmonics change in odd values, total harmonic distortion, and Vrms values. Figure 3 shows that a modulation index of 0.85 is better than 0.9 and for the value of THD and Vrms.

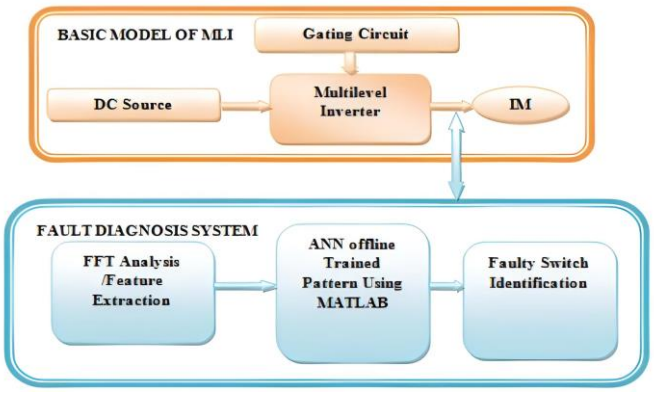

Figure 1: Proposed fault diagnosis system of multilevel inverter

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The FFT provides frequency domain representation of any periodic or non-periodic signal. In particular, the Fourier transform (FT) is an extension of the Fourier series. The FT utilizes exponents and trigonometric functions rather than sines and cosines, even in a Fourier series. The FT is specified as in expression for a signal or parameter f(t) in equation (1),

$$F(\omega) = \int_{-\infty}^{\infty} f(t) e^{-i\omega t} dt \quad (1)$$

The inverse Fourier Transform is defined as in equation (2),

$$f(t) = \frac{1}{2\pi} \int_{-\infty}^{\infty} F(\omega)\ e^{-i\omega t} d\omega \quad (2)$$

The expression below is used to calculate THD for an output voltage pattern in equation (3),

$$THD = \sqrt{\frac{V_2^2 + V_3^2 + V_4^2 + ... + V_n^2}{V_1}} \quad (3)$$

Where V_n is the root means square value (RMS) of the voltage of the nth harmonic, and n=1 is the frequency of the signal. It determines the degree of distortion in a voltage output.

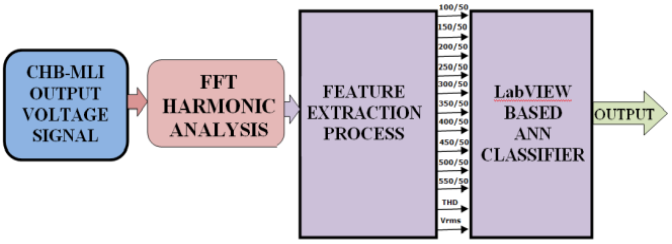
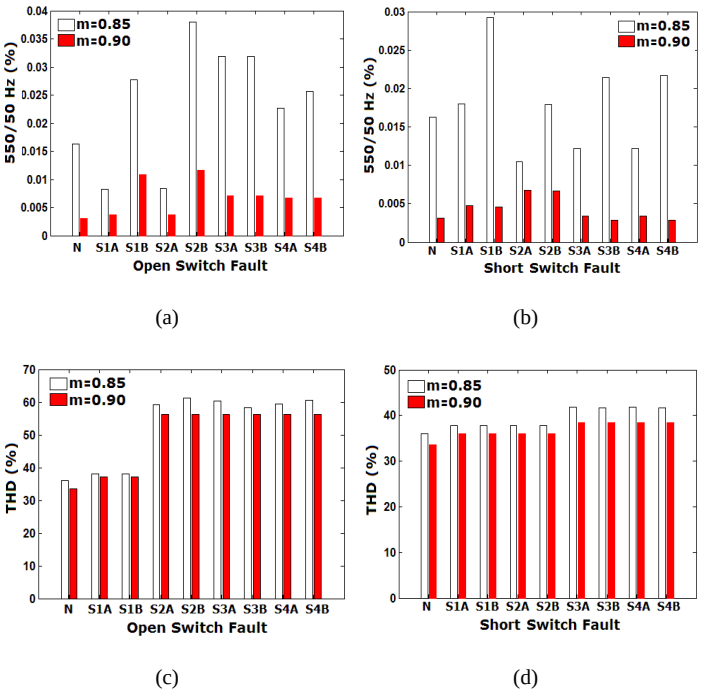


Figure 2: FFT Harmonic analysis of output voltage signal



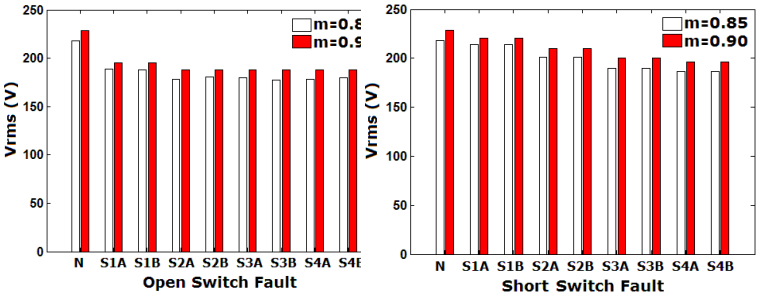


Figure 3: Representation of FFT investigation during (a) 11th harmonic with Open Circuit fault (b) 11th harmonic with Short Circuit fault (c) THD for Open Circuit fault (d) THD for Short Circuit fault (e) Vrms for Open Circuit fault (f) Vrms for Short Circuit fault

2.1 Fault Classification Using ANN Techniques

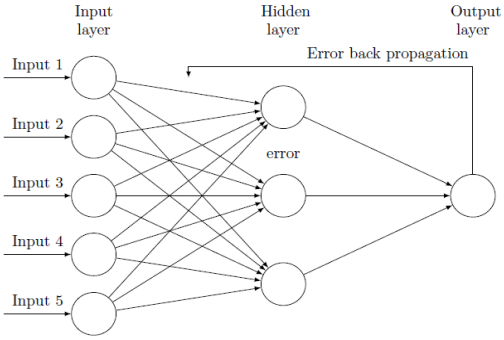


Figure 4: Back propagation of error in multilayer feed forward network

In a multilayer feed forward network, *Figure 4* depicts the error back propagation. The back propagation technique is used to compute the necessary modifications once the network's weights are picked at random. The back propagation (BP) algorithm may be separated into four stages in general. The back propagation algorithm has four steps: feed-forward processing, back propagation to the output layer, back propagation to the hidden layer, and weight modifications. When the error function's value falls below a certain threshold, the algorithm is disturbed, i.e., when the difference between the observed and projected performance is smaller than a certain threshold (convergence criteria). The deviation is back-propagated in this system, and the weight values are effectively adjusted using a technique to lower the mean square error (MSE), which is also the mean of all the errors for all combinations of inputs and outputs and is calculated using expression (4),

$$MSE = \frac{1}{n} \sum_{m}^{n} (P_m - Q_m) \quad (4)$$

The expected and observed outputs for the m^{th} input pattern are denoted by P_m and Q_m, respectively, where n denotes the total number of input sets. Effective failure detection for multilevel inverters was automated using an artificial neural network (ANN) in this investigation. The ANN was used to solve the difficulty of detecting the faulty switch in a cascaded

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multilevel inverter. Due to its simple methodology and excellent predictive potential, the multi-layer feed forward network with back propagation learning technique has been regarded one of the numerous ANN designs accessible in the literature.

Using the 9 output neurons, the fault is categorized as no fault, S1A to S4A fault, and S1B to S4B fault. The output layer neurons are set up to perform multiple binary training patterns in response to different degradation scenarios.

Network topology, size, and learning rate, number of training sets, convergence criterion, and number of iterations are all essential parameters that influence the neural network's convergence and learning time. The learning rate is known to damp out oscillations to some extent, during the training phase. Higher values of learning rate may result in fast convergence, but it may result in oscillation. The training time of the neural network will rise as the number of training sets and training cycle increases. For improved classification results, an appropriate neural network structure must be found. As a result, in order to arrive at an ideal topology, the effectiveness of the neural network for varying parameters of the learning rate, training sets, convergence criterion, iterations, and number of neurons in the hidden layer must be examined in depth and assessed.

The majority of processing facilities in the hidden layer and the number of observations is two significant parameters that influence the neural network's functionality. The neural network fails to meet the convergence requirements when the number of hidden layer neurons is fewer than 10. The neural network takes longer to train and meet the convergence requirements when the quantity of hidden layer neurons rises over 24.

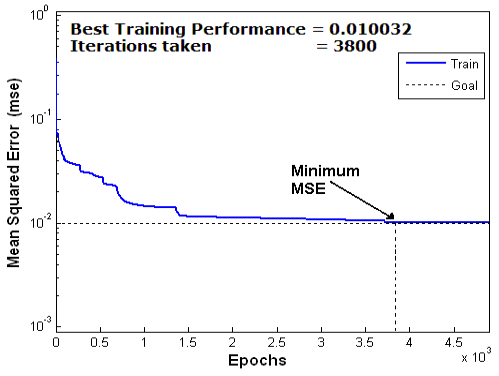

Figure 5: Identification of best training performance of MSE

The current network achieves convergence criterion at 3800 iterations throughout the training phase. It shows that 3800 iterations are enough for the optimal neural network to be successfully trained. Then 150 more data points were employed for identification testing with modulation indices ranging from 0.8 to 0.95 which is as shown in *figure 5*.

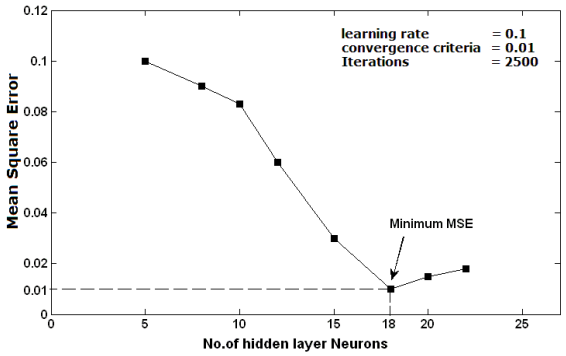

Figure 6: Investigation of the ANN-MSE at various statistics of hidden layer neurons for 18

The neural network takes longer to train and conform to the convergence requirements when the number of hidden layer neurons increases beyond 18. In order to arrive at an ideal number of epochs, the network's mean square error was calculated by keeping the step size at 0.1 with 18 hidden layer neurons. *Figure 6* displays the proposed fault diagnostic system's detection rates for various numbers of hidden layer neurons, with MSE values determined from varying amounts of hidden layer neurons. As compared to other instances, the device performs better with 18 secret layer neurons. In this context, the overall detection performance for all fault conditions is about 100%, and the device can correctly find the fault in nearly any situation.

2.2 Five level Cascaded H-Bridged MLI

Figure 7 shows the schematic single-stage, five-stage voltage output of the cascaded H-bridged multi-level inverter used in existing positions correlated with induction motor load. Induction motor characteristics such as unbalanced stator currents and voltages, torque oscillations, efficiency and torque decreases, overheating, and excessive vibration are all affected if the multilevel inverter power semiconductor switches fail. Furthermore, some harmonic components of currents and voltages can be amplified by these motor problems. To achieve good performance, the defective switch must be identified and replaced as quickly as possible. Each IGBT switch is categorized as S1A, S1B, etc. by its cell position. The simulation experiments have been performed using the MATLAB/SIMULINK tool and *table 1* summarizes the parameters used for the simulation analysis.

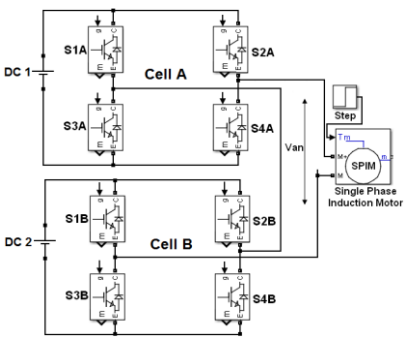

Figure 7: Single-phase cascaded H-Bridged 5-level multi-level inverter coupled to the drive system

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Table 1. Simulation parameters of five level MLI

Parameters	Values
DC Input Voltage	115V
Number of H-Bridges	2
No. of switches	8
Output levels	5
Modulation Index	0.85
Carrier Frequency	3 kHz
Load	Single Phase IM, 0.5HP, 50 Hz, 230V

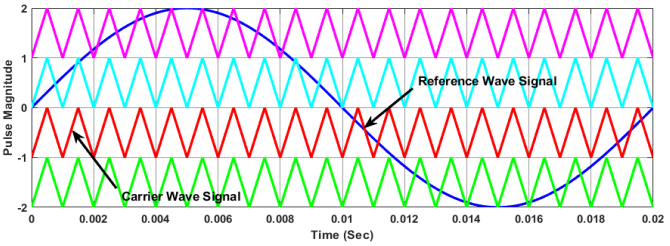

Figure 8: The sinusoidal reference signal and the triangular carrier signal in PWM are used for modulation index of 0.85 carrier frequency of 3 kHz values

The SPWM approach is frequently utilised to create the requisite IGBT transition switching patterns. The pulse of the triangular carrier is the same as the reference sinusoidal signal when SPWM is resent. As illustrated in *Figure 8*; the switching signals are processed using a sinusoidal and triangular signal with a modulation index of 0.85. The technique of sinusoidal pulse width modulation addresses sinusoidal waveform creation by contrasting reference to carrier waves or filtering the pulse output waveform by altering the widths of triangular waveforms.

Table 2. Switching table of five level cascaded MLI

Switching Sequences								Voltage levels
Bridge - A				Bridge - B				
S1	S4	S2	S3	S1	S4	S2	S3	
1	1	0	0	1	1	0	0	$+2V_{dc}$
1	1	0	0	0	0	0	0	$+V_{dc}$
0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	$-V_{dc}$
0	0	1	1	0	0	1	1	$-2V_{dc}$

Table 2 illustrates the switching patterns of five level cascaded multilevel inverter during healthy condition. SPWM based cell a switching pulses are generated by 3 kHz carrier frequency and 0.85 modulation index is shown in *Figure 7*.

3. RESULTS AND DISCUSSION

3.1 Open Circuit Fault Analysis and Discussion

The primary open circuit failure occurs around 1 sec with the bridged *cell A* switch in *S1A* to determine the voltage level output before and after the start of the open circuit failure of the multilevel inverter. *Figure 9* reflects the typical output voltage, amplified view and output current at both the failure of such a single stage cascaded H-Bridge inverter topology related to the inductive motor. Related voltages and pulses are sampled at 20 kHz, which is shown in *Figure 9*.

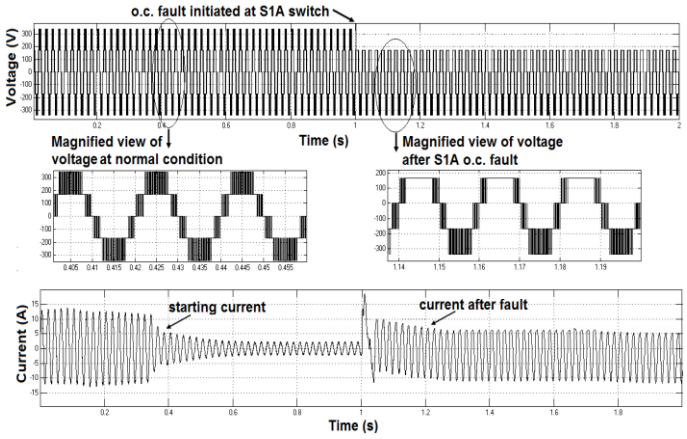

Figure 9: Voltage and load current pattern of cascaded H-bridged inverter topology with inductive motor before and after S1A switch open circuit fault initialization

In the case of open switch fault waveforms, there is a fifty percent clipping at the voltage magnitude level in the positive or negative half of the time as opposed to no fault condition. *Figure 10* shows the output voltage and load current waveforms with an induction motor load following an S2A open circuit fault. *Figure 11* depicts the typical output voltage waveforms of cells A and B at 0.85 modulation index values under normal, open-switch fault circumstances, respectively. When comparing open switch fault voltage waveforms to no fault conditions, there is a fifty percent clipping in the voltage magnitude level in the positive or negative half cycle. When comparing the output voltage waveforms under open-switch fault scenarios to the normal state, there is a significant variation in all output voltage patterns. These waveform images clearly depict the fluctuations at each problem instance, which can help to create a fault detection system that is more efficient.

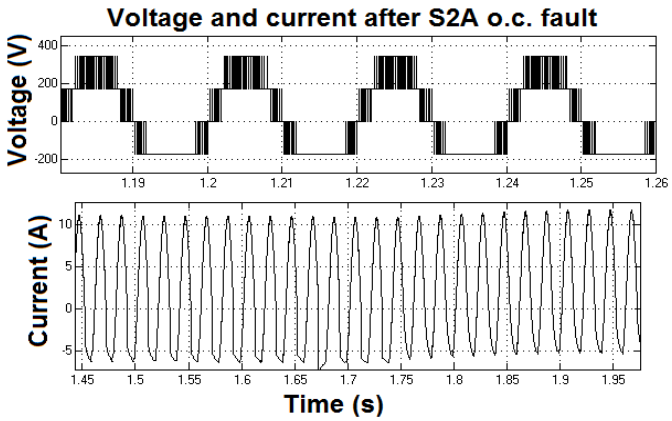

Figure 10: Fault analysis of S2A switch during open circuit fault

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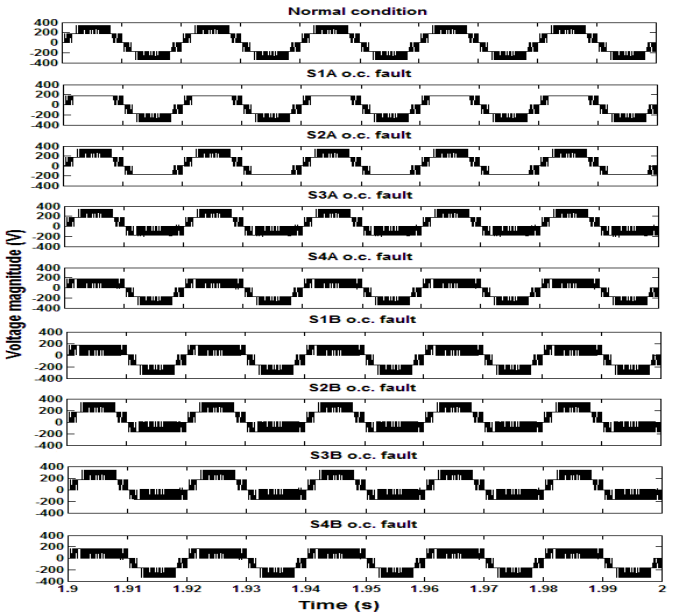

Figure 11: Output voltage waveforms at normal condition and after open switch fault of *Cell A* and *B*

3.2 Short Circuit Fault Analysis and Discussion

The initial short-circuit fault is triggered by one second (1sec) of the H-Bridge A S1A switch to consider the pre and post current and voltage series starting the short-circuit fault of the inverter topology. The output displays the normal output voltage and current waveform of the H-Bridged multilevel cascaded single-phase inverter. The short circuit fault of S1A is generated at one second (1 sec) and the *figure 11* shows the embellished current and voltage waveform and also shows the start of the fault. *Figure 12* illustrates a magnified view of the output voltage and load current waveforms with an induction motor load following an S1A short circuit failure. *Figure 13* displays the standard output waveforms obtained under the normal and distinct short switch fault conditions of cells A & B at the 0.85 modulation index value respectively. As a consequence, there is a small decrease in the output voltage and in the positive or negative half loop in the case of short switch fault waveform generation. As a result of a detailed inspection of the output voltage waveforms, it has been a significant change in all voltage output patterns in both the open-switch and short-switch voltage fluctuations as opposed to normal conditions. These waveform diagrams explicitly display the variations for each fault situation, which would help encourage the development of a successful fault detecting system.

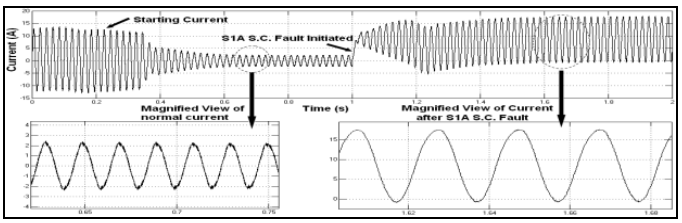

Figure 12: Magnified view of fault analysis before and after the initiation of S1A short circuit fault with induction motor load m=0.85. Fault initiated at 1 sec

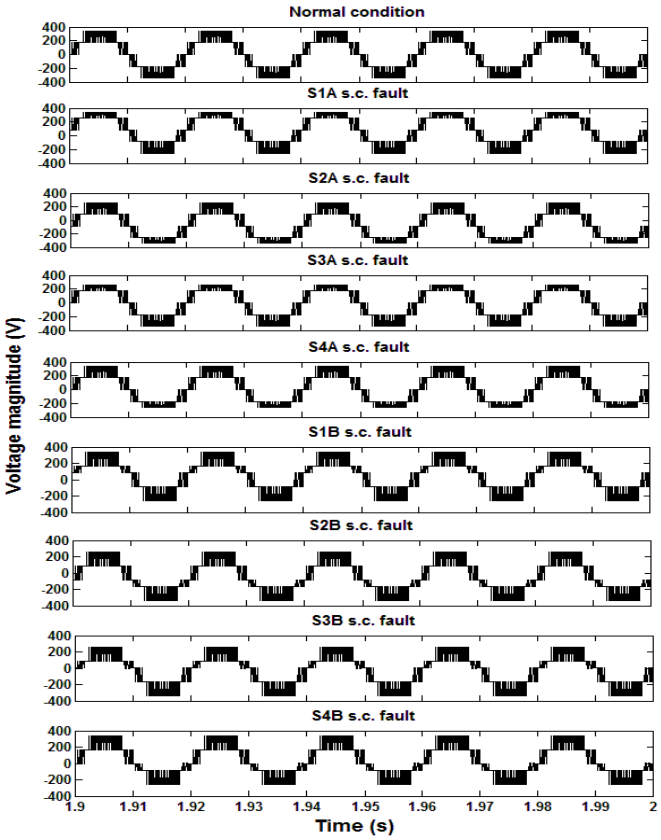

Figure 13: Voltage output patterns in normal state as well as short circuit fault states of *Cells A* and *B*

Figure 13 depicts the typical output voltage waveforms of cells A and B at 0.85 modulation index values under normal, short-switch fault circumstances, respectively. When comparing short switch fault voltage waveforms to no fault conditions, there is a fifty percent clipping in the voltage magnitude level in the positive or negative half cycle. When comparing the output voltage waveforms under short-switch fault scenarios to the normal state, there is a significant variation in all output voltage patterns. These waveform images clearly depict the fluctuations at each problem instance, which can help to create a fault detection system that is more efficient.

The key properties of the load voltage output waveform are explored utilizing simulation under various open-switch and short-switch faulty conditions. Furthermore, major elements such as THD analysis using the FFT technique, as well as an assessment of the MSE at various numbers of hidden layer neurons, are defined to be fed to that back propagation trained ANN. In a cascaded multilevel inverter, this suggested fault detection approach could identify each individual fault switch. When compared to the load current pattern, the output voltage waveform at different fault circumstances exhibits distinct patterns, making it easier to discern the nature of the defect via visual observation. THD and Harmonic/Fundamental ratios up to 11th order harmonics collected from the FFT analysis provide critical information about the multilevel inverter's failing switch. The number of levels of multilevel inverters is increasing every day for high-power applications; the

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suggested system can be evaluated for 7 level and 9 level inverter systems.

4. CONCLUSION

This paper examines the malfunctioning transition fault diagnosis of a single-phase H-bridged cascaded 5-level inverter topology attached to the inductive motor. Specified output voltage waveform properties are explored through simulation research in various open-switch and short-switch fault conditions. This approach focuses on the similarity of the output voltage and indeed the modulated voltage signal, as well as on the effect of the modification of the multi-level inverters on the discrepancy. Digital filters may be created and implemented in the future for real-time applications while recording the output voltage signal to remove high-frequency noise. The suggested topology is restricted to a five-level multilevel inverter, but it may be expanded to seven, nine, eleven, and more levels. As the number of switches increases, so would the need for identification to locate a faulty switch. Also, the transients detected in the current signal during the open circuit or short circuit faults of the multilevel inverter may be studied and a diagnostic procedure created using this information for 7-level and 9-level inverters.

Conflicts of interest: The authors have no conflicts of interest to declare.

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