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International Journal of
Electrical and Electronics Research (IJEER)
Research Article | Volume 10, Issue 2 | Pages 341-346 | e-ISSN: 2347-470X

Design and Leakage Power Optimization of 6T Static Random Access Memory Cell Using Cadence Virtuoso

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ABSTRACT- Reduction of Leakage power at nano meter regime has become a challenging factor for VLSI designers. This is owing to the need for low-power, battery-powered portable pads, high-end gadgets and various communication devices. Memories are made up of Static RAM and Dynamic RAM. SRAM has had a tremendous impact on the global VLSI industry and is preferred over DRAM because of its low read and write access time. This research study proposes a new method has been proposed of 6T Static Random Access Memory cell to decrease the leakage current at various technologies. Three source biasing methods are used to minimize the 6T SRAM cell leakage power. The three methods are NMOS diode clamping, PMOS diode clamping and NMOS-PMOS diode clamping at 45 nm and 90 nm technology nodes. This paper also emphasizes on the implementation of 6T SRAM cell using Multiple Threshold CMOS (MTCMOS) technique at 45nm technology. The simulation is achieved and various power dissipations are analyzed at supply voltage of 0.9 V and 0.45 V for 90 nm and 45 nm technology respectively using cadence virtuoso tool. PMOS clamping has shown the reduction in an average power by 82.19% than compared to other two proposed techniques.

Keywords: Clamping diode, Forward body bias, Low Power, MTCMOS, Reverse body bias, Source biasing.

ARTICLE INFORMATION

Author(s): Sufia Banu and Shweta Gupta

Special Issue Editor: Dr. S. Muthubalaji
Received: 20/05/2022; **Accepted**: 16/06/2022; **Published**: 30/06/2022;
e-ISSN: 2347-470X;
Paper Id: 0322SI-IJEER-2022-26;
Citation: 10.37391/IJEER.100246
Webpage-link:
https://ijeer.forexjournal.co.in/archive/volume-10/ijeer-100246.html

This article belongs to the Special Issue on **Intervention of Electrical, Electronics & Communication Engineering in Sustainable Development**

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1. INTRODUCTION

In the past, performance and miniaturization of an integrated device was the major design concern of a VLSI designer. Technologies scaling from micro meter regime to nano meter regime yields in increased integration density referring to more number of semiconductor devices that are significantly smaller and quicker are embedded onto a single tiny piece of chip. This scaling is done to provide quicker speed and a greater operating frequency, resulting in increased power dissipation. With the growing popularity of portable battery-operated gadgets, power dissipation has become a crucial concern as these devices spend majority of the time in standby or sleep mode. Proper heat sinks are also necessary to dissipate the power in right manner in a circuit. Power dissipation also has an impact on packaging and reliability. Earlier days these battery-operated handheld gadgets had lower computing performances yielding to reduced power dissipation, while technology scaling led to higher performance than the non-portable devices. It is the need of an hour to prolong the life of the battery of these battery-operated portable gadgets and it's challenging for the circuit designers.

An Integrated Circuit is made up off combinational devices, sequential devices, memory units and input-output devices. Each circuit in an IC contributes to the total power dissipation. The portable battery-operated devices such as cell phones had a single core processor. With advancement in technology transistor density is increased with octa-core processors. Static RAM used in portable battery powered devices needs lower area and parallel lower power consumption [1]. Static RAM used in embedded controllers requires less read and write time. Due to the significant increase of lower power and lower voltage memory systems in recent years, SRAM has been emphasized in the research sector. On-chip memory is built utilizing arrays of tightly packed Static RAM cells to provide increased quality. As a memory cell, a 6T Static Random Access Memory (SRAM) is commonly utilized. The two most common kinds of power dissipation in an electronic circuit include Switching power and Static power dissipation. During the active mode of performance, when the device is under ON state, the power dissipation is majorly because of both switching power and static components of the semiconductor. While during the standby mode or sleep mode of operation, when the device is under OFF state, standby leakage current is responsible for the power dissipation. With technology scaling the leakage power is dominating that the dynamic power and hence is of major design concern to the VLSI designers as most of the portable devices are battery operated [2].

2. MAJOR LEAKAGE CURRENT COMPONENTS

There are numerous origins of leakage current for nanometer devices, which includes low threshold voltage causes subthreshold leakage current, extremely thin gate oxides cause gate leakage current, and the heavily doped halo causes Band-To-Band Tunneling (BTBT). [3].

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2.1 Sub-threshold Leakage Current

Subthreshold leakage occurs while the transistor is under weak inversion region of operation *i.e.* when gate to source potential of a semi-conductor is lesser than its threshold voltage *i.e.* $V_{gs}<V_{th}$ as well it is majorly comprised of diffusion current [4]. The two major subthreshold paths in 6T SRAM cell are from VDD to the GND and bitlines (BL, BLB) to the GND.

2.2 Gate Leakage Current

In the nanoscale era, excessive technology scaling amplifies Short Channel Effects (SCE) which includes V_{th} roll-off and Drain Induced Barrier Leakage (DIBL). Each technological generation must scale the oxide thickness (Tox) to manage the SCE. Excessive miniaturization of Tox results in a large electric field, which leads to a large direct-tunneling current along the semiconductor's gate insulator [5]. Gate oxide tunneling current refers to the tunneling of electrons or holes through a semiconductor's gate oxide. The three important gate leakage processes in semiconductor device are tunneling in the Electron Conduction Band (ECB), Electron Valence Band (EVB), and Hole Valence Band (HVB). In ECB, electrons tunnel from the substrate's conduction band to the gate's conduction band and vice versa. In EVB, tunneling of electrons takes place from the substrate's valence band to the gate's conduction band. In HVB, holes tunnel from the substrate's valence band to the gate's valence band and vice versa.

2.3 Junction Leakage Current

The semiconductor Metal Oxide Semiconductor (MOS) device comprises of two PN junctions i.e. drain region to well and source region to well. PN junction leakage current occurs when these junctions are reverse biased. When 'P' and 'N' junctions are doped heavily results in BTBT tunneling while it also dominates PN junction leakage current [6]. Junction leakage is typically smaller than compared to other sources of leakage currents and it exists across the access transistors of SRAM cell [7].

3. LEAKAGE CURRENT REDUCTION TECHNIQUES

Various leakage power reduction techniques have been proposed by researchers at the device, circuit, and architectural levels. At device level the leakage power is reduced by scaling the channel length, junction depth, oxide thickness [8-10]. Researchers have come up with newer transistor structure such as Fin-shaped FET (FINFET) having two or more gates resulting in lower short channel effect and lower subthreshold leakage current. At circuit level various leakage reduction techniques include DMOS, VTMOS, MTCMOS, STACKING (forced stack, sleep stack, lector, galore, sleepy keeper, and zigzag keeper), source biasing, body biasing, drain gating and many more [2]. At architectural level techniques include multiple modes management which puts the unutilized memory in sleep mode or standby mode thereby reducing leakage current which allows only a small part of the memory to be ON [11-12].

3.1 Body Biasing Scheme

The sub-threshold leakage current fluctuates exponentially as a function of device's threshold voltage (V_{th}). This is adopted to decrease the propogation delay and leakage current to a greatly by varying the threshold voltage. Body bias alters the V_{th} by applying the voltage across source and substrate terminal of a MOS device. The MOS transistor threshold voltage is related to source to substrate voltage as shown in Eq. (1) [13].

$$V_{th} = V_{to} + \gamma\sqrt{\emptyset s + V_{sb}} - \sqrt{\emptyset s} \qquad (1)$$

Where V_{th} is the threshold potential of semiconductor device, V_{to} is the threshold potential at zero body-bias, γ is the body effect factor, V_{sb} is the voltage across source and substrate and φ_s is the surface potential.

Reducing the voltage between source and substrate (V_{sb}), V_{th} voltage of the device decreases thereby increasing the performance of a device. By increasing the potential across source and substrate (V_{sb}), V_{th} of device increases thereby reducing the leakage current across OFF transistors [13].

In passive CMOS, the substrate terminal of PMOS is wired to VDD and substrate terminal of NMOS is wired to GND. Source to substrate (bulk) potential can be a non-zero value by adopting various body biasing schemes such as Forward Body Bias (FBB), Reverse Body Bias (RBB), DTMOS, VTMOS. Body biasing scales the threshold voltage of the device while supply voltage is kept constant. Body biasing either increases or decreases the V_{th} of the device. The FBB enhances the performance (decreases the delay) by decreasing the V_{th} of the device. The RBB minimizes the leakage current by boosting the V_{th} of the device. Hence by smartly choosing both the delay and leakage current of the semiconductor can be decreased. The body bias can also characterized as fixed, variable and dynamic depending on the application [14]. A set forward or reverse bias voltage is placed across the transistor's substrate terminal in a Fixed Body Bias configuration. Different bias voltages are used in variable and dynamic body bias. Body bias voltages must be generated by an extra control circuitry called a Body Bias Generator in variable and dynamic body bias systems (BBG).

3.2 Source-biasing Scheme

Source biasing approach is employed to reduce leakage by utilizing an additional clamping circuitry in line with the pull down NMOS semiconductor to accomplish data retention. In between SRAM cell's source lines and GND, a high threshold voltage NMOS transistor is introduced. [15]. The gate terminal of NMOS transistor is latched to the WL (word line) as illustrated in *Figure 5*.

During the active mode, WL goes logic high which tunes ON NMOS transistor. The SRAM device functions conventionally since resistance is very small thereby the virtual ground (V_{SL}) more or less functions as normal ground. During the standby mode, the WL goes low which turns OFF the NMOS transistor, results in decreasing the gate leakage and sub threshold leakage current. Drawback by using an extra NMOS transistor in the pull down network is that it increases dynamic energy, delay

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Research Article | Volume 10, Issue 2 | Pages 341-346 | e-ISSN: 2347-470X

and area. The pull-down semiconductor is frequently shared with a bank of SRAM cells to save space. During the standby when NMOS pull down transistor is turned off results in virtual ground where V_{SL} charges up to floating positive potential. This makes SRAM device more vulnerable to noise. To overcome this problem, an additional PMOS semiconductor device is introduced parallel to it, shorting the gate with drain terminals of PMOS makes a clamping diode as shown in *figure 7*.

3.3 Dynamic Threshold MOS (DTMOS)

Leakage reduction is attained by changing the threshold voltage V_{th} of a device dynamically called as DTMOS. In this, the gate and substrate terminals are tied together [16]. Due to this configuration, threshold voltage is dynamically changed as the substrate voltage is varied with the input gate voltage V_{IN}. Low V_{th} is used in active mode, resulting in improved speed, whereas high V_{th} is used in standby mode, resulting in lower static current.

3.4 Multiple Threshold MOS (MTCMOS)

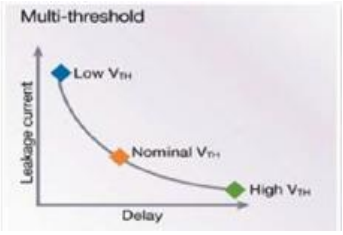

Figure 1: Multiple Threshold MOS Variation with Leakage Current

This technique makes use of multiple threshold voltages high and low threshold voltages V_{th} to optimize power and delay as shown in *figure 1*. High threshold transistor switch slower thereby reduces the leakage power. While low threshold transistors switch faster but have high leakage power. MTCMOS makes use of high threshold voltage transistors known as sleep transistors. During the active mode of operation, these are ON and the circuit will behave normally. While in sleep mode, these transistors are OFF thereby reducing the leakage power [17]. These sleep transistors aims in reduction of standby leakage power to larger extent during the OFF state of SRAM cell

4. CONVENTIONAL 6T SRAM CELL

Static RAM memory cells are made up of two inverters that are cross coupled as seen in *Figure 2* [18]. The inverter2's output (Q') is connected to the inverte1's input (A). When the voltage transfer characteristics of the first inverter (VoA v/s ViA) are compared with those of the second inverter (VoB v/s ViB), three alternative operating locations (A, B, and C) are obtained. Because the loop gain is less than one, the operation points A and B are stable. Inverter one's output is high, while inverter two's output is low, as shown in point A. Inverter one's output is low, but inverter two's output is high, as seen in point B.

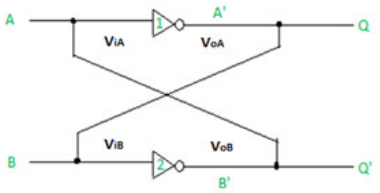

Figure 2: Cross Coupled Inverters (Basic bi stable element)

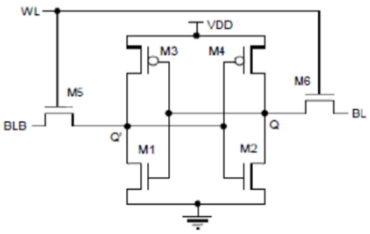

Figure 3: Conventional 6T SRAM Cell

This demonstrates that in any stable circumstance, the outputs of two inverters are complimentary. This attribute is used to create Static Random Access Memory cell (SRAM) cell. Two cross coupled inverters make up a traditional 6T SRAM memory cell which forms four CMOS transistors (M1,M2,M3,M4) which acts as memory and 2 access transistors formed by M5 and M6 which serves to regulate the cell while performing read and write operation as illustrated in *figure* 3. The access transistors are controlled by the word line WL, which is connected to the bit lines BL and BLB, providing access to the cell. The bit lines are used to transport data to and from the memory during write and read operations.

The cell's three phases of operation are as mentioned below [19].

Read Operation: During this, bit lines (BL and BLB) act as output lines and both are pre-charged with certain voltage normally Vdd/2 (logic 1). When the word line is asserted, both the access transistors M5 and M6 linked to the bit lines are enabled, causing the bit-line voltages to decrease slightly. The output of these bit line voltages is send to sense amplifier which acts as an op amp comparator. It compares the difference between BL and BLB. If voltage across BL>BLB, it outputs a logic 1 and if voltage across BL<BLB, it outputs a logic 0. The advantage of using a sense amplifier is that it sets the output quickly without fully charging or discharging.

Write Operation: Bit lines act as input lines during the write process. The value that is to be written into the cell is provided by these bit lines. The word line will be asserted to logic high to access the bitlines i.e. WL=1. If logic 1 is to be written, bit line bar is loaded to supply rail VDD while bit line is discharged to low potential, and Word line is asserted, resulting in successful data (logic 1) writing into the cell. If logic 0 is to be written, BLB is discharged to ground potential, while BL is loaded to VDD and Word line is asserted, resulting in successful data (logic 0) writing into the cell.

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Hold Operation: During the hold or ideal state, the word line is not connected i.e. WL=0 which does not turn on the access cells M5 and M6. This open circuits the cross coupled inverter from the bit lines (BL, BLB) and thereby the data is held in the memory cell. Hence is it said to be in hold state or ideal state as data is held in the latch mode. As long as the semiconductor is connected to the power source, it will continue to store the data.

5. PROPOSED 6T SRAM CELL

6T SRAM cell is implemented employing Cadence virtuoso software is as shown in *figure 4* at 90vnm and 45 nm technology nodes and various power parameters such as average power and leakage power are calculated. The idea for this implementation shows three different methods to minimize the leakage current in 6T SRAM cell. The traditional 6T SRAM device is as depicted in *figure 4*. The proposed work employs clamping of a) one extra high V_{th} NMOS transistor as shown in *figure 5*, *b*) one extra high V_{th} PMOS transistor as shown in *figure 6* c) a pair of high V_{th} NMOS-PMOS transistors in between the source terminal and ground of SRAM cell as shown in *figure 7*. The schematic of standard 6T SRAM cell is shown in *figure. 4* that comprises of two cross coupled inverters along with two access transistors thereby forming six transistors.

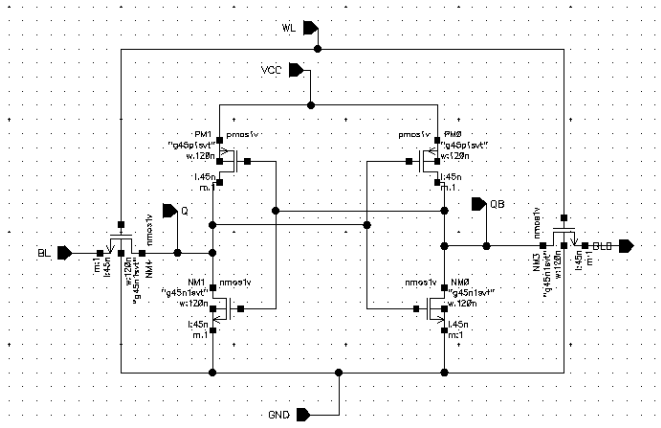

Figure 4: Conventional 6T SRAM Cell Schematic in Cadence

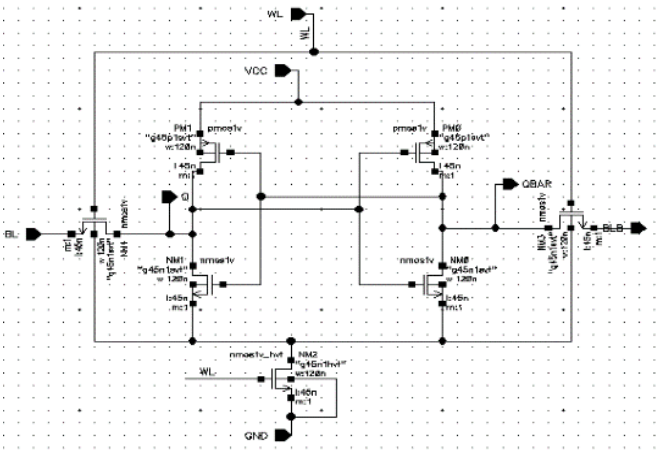

Figure 5: Conventional 6T SRAM Cell Schematic with NMOS Clamping Diode

By adding an extra high V_{th} NMOS transistor between the SRAM cell's source line V_{sL} and Ground (GND), leakage current across a 6T SRAM cell is considerably decreased. During active state, word line is activated (WL=1) which turns ON the NMOS transistor and the SRAM cell behaves normally, since the resistance is smaller across the circuit. During the standby state, word line is deactivated (WL=0) which turns OFF the NMOS transistor thereby the source line (V_{sL}) will be raised to greater potential that results in decreasing the subthreshold leakage current and gate leakage.

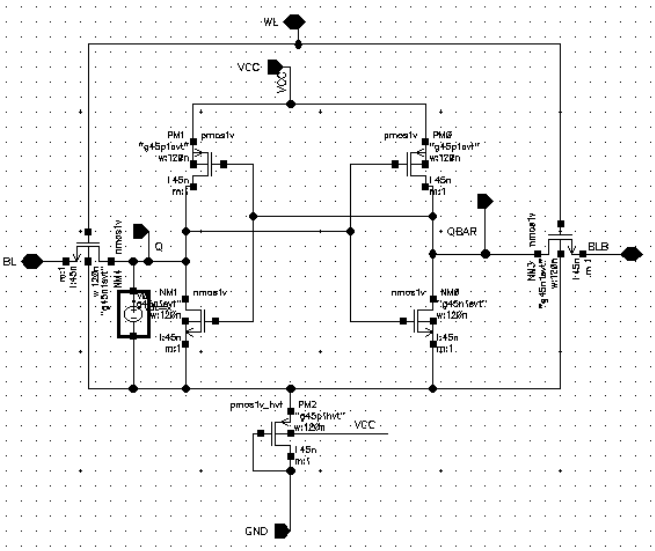

Figure 6: Conventional 6T SRAM Cell Schematic with PMOS Clamping Diode

During the standby when NMOS pull down transistor is turned off results in virtual ground where V_{sL} will be charges up to floating positive potential. The SRAM cell becomes more vulnerable to noise as a result of this. To overcome this issue, an additional PMOS cell is introduced in parallel to it, shorting the gate and drain terminals of PMOS makes a clamping diode as given in *figure 7*. A high V_{th} PMOS cell is added between the source terminal and ground terminal of SRAM cell instead of NMOS transistor as shown in *figure 6*.

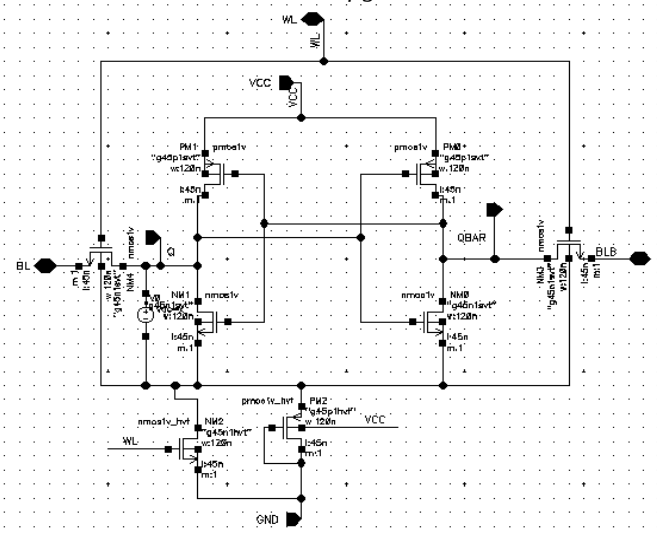

Figure 7: Conventional 6T SRAM Cell Schematic with NMOS-PMOS Clamping Diode

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Research Article | Volume 10, Issue 2 | Pages 341-346 | e-ISSN: 2347-470X

A pair of NMOS and PMOS high threshold voltage transistors inserted in parallel between the source terminal and ground terminal of SRAM cell is as depicted in *figure 7*. The transient analysis of 6T SRAM device is as shown in *figure 8*. The test schematic where the voltages are applied the inputs WL, BL and BLB is as available in *figure 9*. The symbol of 6T SRAM cell which is generated from the schematic is as shown in *figure 10*.

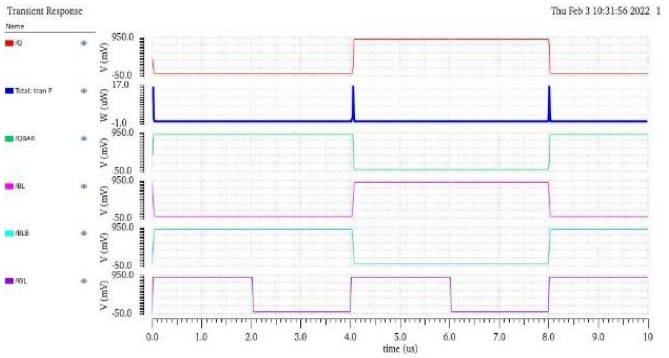

Figure 8: Transient Analysis of 6T SRAM Cell

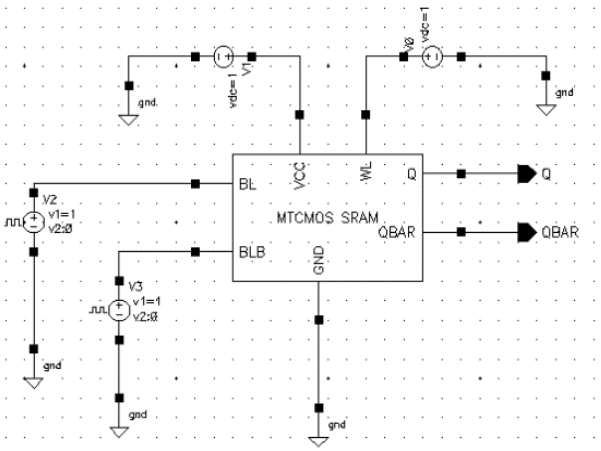

Figure 9: 6T SRAM Test Schematic

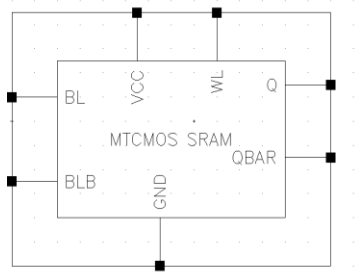

Figure 10: 6T SRAM Symbol

Multiple Threshold CMOS (MTCMOS) of 6T SRAM cell is as given in *figure 11*. Two additional high V_{th} transistors known as sleep transistors are used. A high V_{th} PMOS cell is added across the PUN and supply voltage and a high V_{th} NMOS cell is placed across the PDN & ground terminal. MTCMOS makes use of two threshold voltages in a circuit to obtain higher performance and lower leakage. During the active mode, these high V_{th} sleep transistors are turned ON and low V_{th} SRAM cell operates normally with small propagation delay. During the standby (Sleep) mode, these high V_{th} sleep devices are turned OFF while the conduction path that may arise from low V_{th} SRAM device is smartly cutoff thereby reducing the leakage current.

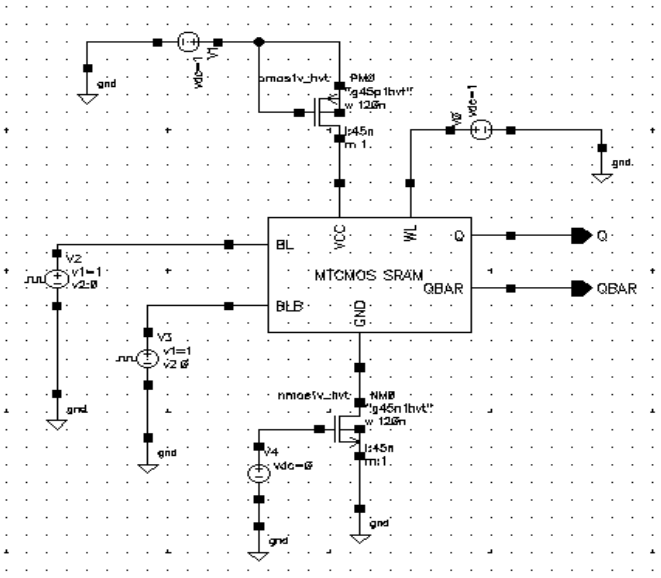

Figure 11: 6T SRAM MTCMOS Test Schematic

6. RESULTS AND DISCUSSION

Table 1 describes the average power of standard 6T Static Random Access Memory cell with proposed techniques having NMOS clamping, PMOS clamping and NMOS-PMOS clamping. PMOS clamping has shown the reduction in an average power by 82.19% than compared to other two proposed techniques.

Table 2 describes the dynamic power of standard 6T Static Random Access Memory cell with proposed techniques having NMOS clamping, PMOS clamping and NMOS-PMOS clamping. *Table 3* describes the leakage power of standard 6T Static Random Access Memory cell with proposed techniques having NMOS clamping, PMOS clamping and NMOS-PMOS clamping. PMOS clamping shown the best results compared to NMOS and NMOS-PMOS clamping. The leakage power analysis of 6T SRAM cell obtained by applying MTCMOS method is as given in *table 4*. The average power is reduced to about 92% using MTCMOS technique, thereby reducing the leakage power.

Table 1: Average Power Analysis of 6T SRAM Cell

Technology	6T SRAM	6T_SRAM NMOS	6T_SRAM PMOS	6T_SRAM NMOS PMOS
90nm	9.66E-08	4.99E-08	1.72E-08	5.36E-08
45nm	1.25E-10	5.43E-11	1.98E-11	5.39E-11

Table2: Dynamic Power Analysis of 6T SRAM Cell

Technology	6T SRAM	6T_SRAM NMOS	6T_SRAM PMOS	6T_SRAM NMOS PMOS
90nm	8.01E-08	4.49E-08	1.72E-08	4.84E-08
45nm	1.23E-10	5.29E-11	1.83E-11	5.23E-11

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Table 3: Leakage Power Analysis of 6T SRAM Cell

Technology	6T SRAM	6T_SRAM NMOS	6T_SRAM PMOS	6T_SRAM NMOS PMOS
90nm	1.65E-08	5.02E-09	4.58E-12	5.12E-09
45nm	1.77E-12	1.35E-12	1.54E-12	1.53E-12

Table 4: Leakage Power Analysis of 6T SRAM Cell using MTCMOS Technique at 45nm

	Average Power	Leakage Power
6T SRAM	1.96E-10	1.77E-12
MTCMOS	1.56E-11	1.59E-12

7. CONCLUSION

This paper describes the leakage power minimization methods that include body biasing, DTMOS, MT-CMOS and source biasing, for 6T SRAM cell at various technology nodes. We initially compare the conventional 6T Static Ram Memory Cell-SRAM cell with the proposed technique to minimize the power of the circuit. Section 2 emphasizes the various components of leakage current. Section 3 describes various leakage power reduction techniques. Section 4 describes the standard 6T SRAM Cell. Section 5 describes the proposed 6T SRAM cell which utilizes the clamping unit and power gating MTCMOS technique to reduce the leakage power at different technology nodes.

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