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Performance Analysis of 9T SRAM using 180nm, 90nm, 65nm, 32nm, 14nm CMOS Technologies

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ABSTRACT- The growing markets for low-power electronic devices energized by battery have created the need for smaller power-efficient chips to prevent frequent charging of the source. Nowadays the market capitalization of low-power appliances is expected to grow from USD 4.9 billion by 2022 to USD 7.9 billion by 2027 as per global forecast to 2027 published by markets. The main factor leading to growth of low power electronics market includes demand of energy saving components, miniaturization, and entry of IoT (Internet of Things) devices. In addition, increased investment by automotive OEM (Original Equipment Manufacturer) and governments to promote the adoption of electric vehicles is expected to create more market opportunities. In this digital era, memory components play a major role in power consumption and this incites the research interest these days. CMOS (Complementary Metal Oxide Semiconductor) technology is growing rapidly towards greater integration into a single chip, resulting to a decrease in chip sizes using less space. Speed and stability demand is also growing up. Combined chip density increases as downtime technology continues. Stability and reliability are an important issue for the static random access memory (SRAM) memory device. In this paper, the design and analysis of CMOS based 9T SRAM cell in a variety of technologies is presented. The main focus of this review paper is to analyze 9T SRAM to test performance on several CMOS technologies (180nm, 90nm, 65nm, 45nm, 32nm, 14nm) with the help of a predictable technology (PTM) file. The butterfly curve method is used to examine the consistency of the SRAM bit cell in terms of static noise margin (SNM). It is clearly shown in this paper that as it progresses from 180nm to 14nm the delay decreases with stability.

Keywords: SRAM, SNM, read access time, write access time, leakage power, RSNM, WSNM.

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1. INTRODUCTION

Energy efficient and high-speed non-volatile memory is very important key aspect of developing the non-volatile computing devices for Internet of Thing (IoT) application. The IoT is a novel field of innovation that is rapidly gaining as advances in computing, storage devices and wireless and communication technology. The basic concepts of IoT is pervasive presence around us through different sensors, devices, actuators, smart phones etc. These are able to interact with each other and communicate their neighbors to reach common goals. IoT is fastest growing market which is expected to connect 50 billion things by 2025[Nokia] and grow $3.7 billion market. IoT is promising market of like home automation, automatic agriculture, smarter heat care, smarter natural disaster management and ultimately smarter world. As it has many applications and future market business but it has many challenges. IoT architecture consists of processing unit, wireless module and power storage. Already wireless technology achieved very improvement for last decade. Presently researchers focuses to resolve the issue related charge storage battery because for IoT wire based supply deployment is not feasible. So high-capacity storage battery requirement to power up the IoT devices for month or year based on application like month for home automation application and years for satellite or space application of IoT devices.

Due to technological advances, the efficiency of microprocessors has greatly improved and therefore a drastic processor speed increase has been observed in recent years. However, the memory speed has not been significantly increased and therefore a gap between processor performance and memory increases over time. To reduce the gap between microprocessor and memory performance, in the chip assembly memory is used by the silicon industry to reduce data extraction time. To improve system performance, SRAM density has been increased by device scaling by the researchers. Nowadays, SRAM devices have stable and high processing speed that is used in cache memory. For the design of SRAM cell two aspects are more important. The first is improved stability and second is smaller cell area. The number of transistors is increase day by day [1], resulting in an increase in the delay. The performance of transistor gets suffers a low threshold voltage, however, an increase the transistor of threshold voltage, which leads to an enhanced the

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cell leakage and has an impact on the cell stability [2]. The objective of the researcher is reducing the delay of the SRAM by keeping performance. The cell area has been reduced by 30-50%. However, this area advantage will go down in future scaled down memory requiring reduced supply voltage. In comparison to the various 9T SRAM CMOS technology at different scaling node offers all data isolation by the bit lines of the memory cell, preventing sneak path, enabling higher data read and write stability, as well as lower leakage power. The SRAM cell of 9T is analyzed and carried out for its several parameters such as delay, power, voltage and temperature [3-5]. The CMOS based SRAM cell design having less power consumption. According to Moore's law, the transistor is doubled on the chip every two years due to decreasing of transistor size. As a results, the chip density increases while the device size decrease. For ultra-low-power applications, low power dissipation is a critical design issue. Leakage power has become a prominent factor of total power dissipation as technology advances. Voltage scaling is an effective technique to reduce the power dissipation of SRAM cell [6]**.** Demands of electrical vehicles increases day by day and to full fill the demands the manufactures require to produce more vehicles with in time. The functions of these vehicles are mainly controlled by the programmed ICs (Integrated Circuits) which require storage capacity to store the instructions. During last one year the automobile industry also faces chip crisis, due this the production of vehicles affected badly. OEM is a real manufacturer of vehicle parts that are fully compatible with the vehicle and manufactured with the same quality. We focus on the various designs of ultra-low power, durable logic circuits under process variation that decrease dynamic and static power consumption of 9T SRAM bit cells to a bare minimum. The memory technologies have seen advances in no-volatile memory such as ferromagnetic RAM (Fe-RAM), Phase change RAM (PCRAM), Resistive RAM (RRAM) and STT-MRAM (Spin-transfer torque magnetic random-access memory).

2. SYSTEM MODEL

In logic circuitry, an SRAM cell is having two stable states '0' or '1' and it is a semiconductor memory device for data storage. SRAM memory cells are organized in a matrix and can be individually addressed. The data read all the content with help of column decoder and stored in the SRAM cells. When a single bit line is connected to the drain terminal of a pass transistor, the noise margin tolerance capability is improved. During SRAM cell operation, control the stability, the bit line will pass through two input nodes of access transistor [7]. In the SRAM cell, the word line is responsible to enable the access transistor. The role of the bit line is transfer data of read and writes operation. There is no need for refreshing circuit in the SRAM cell [8]. An ideally SRAM cell is designed to be balanced device physically and electrically is perfectly between the two inverters.

3. EXSISTING WORK ON 9T SRAM CELL

Figure 1 displays an existing 9T of memory cell. It consists of two cross coupled inverter by the connected of pass transistor. Both input of access pass transistor is connected by the complementary of bitline. During the write and read operations, the gate of access pass transistors TN3 and TN4 are connected to the WL (word line) and allow data for write operation in the memory cell or read operation via the BL or BLB (bitlines).

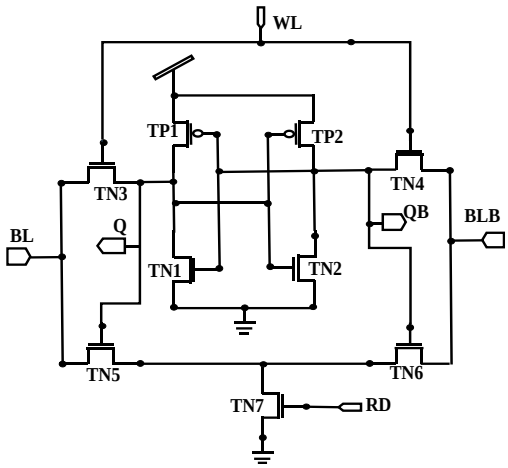

Figure 1: 9T of SRAM cell [34]

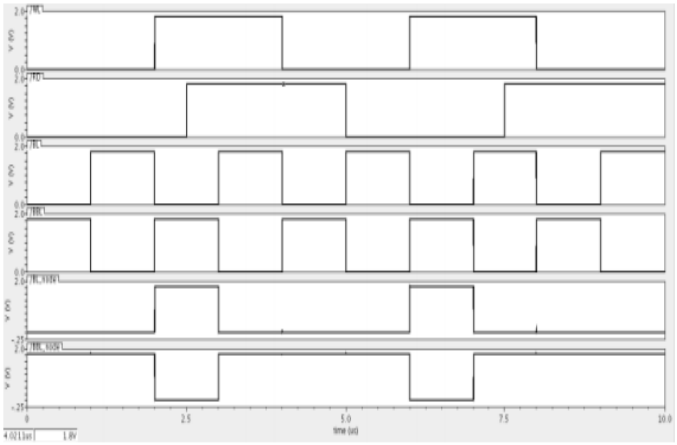

Figure 2: Waveform of the 9T SRAM cell [34]

3.1 Operation of 9T SRAM

Many researchers have focus on the various performance parameters (such as rising delay, falling delay, noise margin, power delay product, speed, stability and area) of 9T SRAM cell in the literature review. Many type of SRAM have already designed of 6T, 7T, 8T, 9T, 10T, and 12T based on CMOS technology. In this paper, we focus on the 9T SRAM cell because it is better performance excluding area in the SRAM cell. There are two sub-circuitry (lower and upper sub-circuit) in the 9T SRAM cell. It is essentially in terms of upper sub-circuitry of a 6T SRAM cell with small sized device composed of TP1, TP2, NM1, NM2, NM3, NM4 and lower sub-circuitry is essentially of TN5, TN6 and TN7 as shown in *figure 1*. Five transistors are used as access pass transistor in the 9T SRAM cell. The two access pass transistor (TN3 and TN4) are controlled by a write signal (W) and it is stored data within the upper sub-circuitry. The SRAM cell in the lower sub-circuitry

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has added an additional two access pass transistors (TN5 and TN6) for the bit line in the 6T SRAM cell and one access pass transistor (TN7) used for the read operation. The data is depending on node Q and QB and stored information by the access pass transistor TN3 or TN4. Singh et al. [9], discussed the comparative analysis of 9T SRAM proposed and existing SRAM design at 45nm technology. The group calculated the PDP with 36% improvement. In the SRAM structure are controlled by separate device of the read and write operation. For the read operation, the read word line (RWL) decide the transition. During the write operation, controls the transition by the access pass transistor NM3 and NM4 for column based write word-line (WWL). The two-stacked read port is enabled by the row-based high RWL and GND, and if QB = '1', the RBL is discharged, and sensing of Q = '0' is done by the sense amplifier. The reverse operation is used to read '1'. RBL is pre-charged by the VDD and WWL at low (‘0’V). The cross-coupled inverter is separated from the outer interconnect, when WWL, WBL and WBLB is kept LOW and the latch is no intrusion effect [10]. RBL is discharge and remain at VDD at depend on the data in the cross coupled inverter. As a result, the read data from latch indirectly worked by the reading stack. Read circuitry is disabled to execute the writing operation by keeping RWL at LOW level when WWL is asserted. After asserting the WWL, the data is loaded by the WBL and WBLB and the write operation is begun by pre-charging. After the write bit lines are pre-charged, the access pass transistors NM3 and NM4 are turn on by asserting the WWL signal, allowing the data to be accessed or passed from the word bit line to the cell as shown in *figure 3*. As a result, data is stored into the cell at the appropriate nodes.

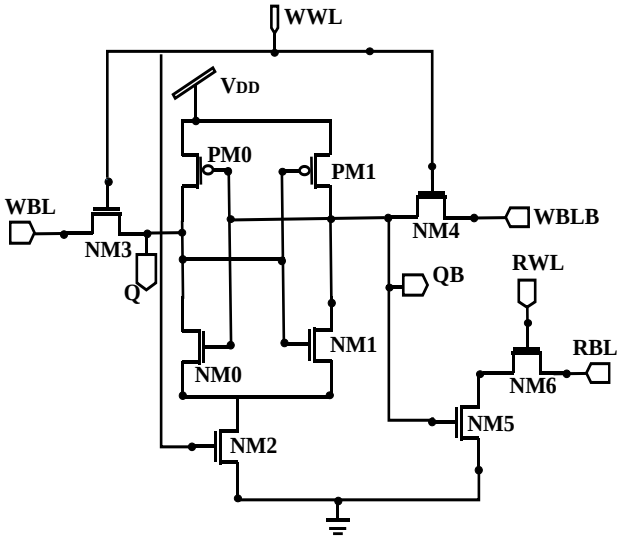

Figure 3: 9T of SRAM cell [8]

Mishra et al. [33] recently designed SRAM cell of 9T, which consist of a single read bit line which consists of 2T read port and one tail transistor for low power and high stability as depicted Fig.3. When compared to a simple 6T SRAM cell developed at the same technology, the proposed design has a 22% reduction in static power dissipation. Also compared to 6T SRAM cell and ultralow voltage 9T SRAM cell**,** it improves write stability by 42% and 34% respectively. Author discussed the read write operating mode at various signal as shown in *table 1* and comparative analysis of performance parameter as shown in table at 65nm CMOS technology.

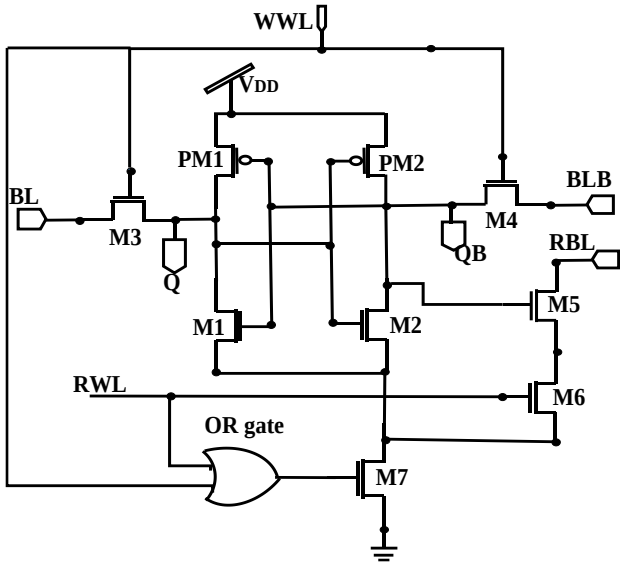

Figure 4: 9T SRAM using OR gate [33]

Table 1 shows the different signal operation for several modes of read write condition.

Table 1: Truth table for 9T SRAM using OR gate

Different Signal	Various Operating mode			
	Hold	Write ‘1’	Write ‘0’	Read
WWL	0	1	1	0
BL	0	1	0	0
BLB	0	0	1	0
RBL	0	0	0	1
RWL	0	0	0	1

3.2 Static Noise Margin (SNM)

The least possible DC noise voltage need to change the characteristics of the storage node is defined as static noise margin. In the SRAM cell, the sub-threshold voltage and channel length of the transistor have an exponential relationship. To preserve the SRAM cell strength at scaled technologies, the threshold voltage reduces with reduction in channel length [24, 25].

3.3 Read Static Noise Margin (RSNM)

The RSNM is calculated from the cell stability to read the saved data. Due to of the scaling of critical current in scaled technology nodes, the read current is interrupted when the saved data change repeatedly. If increase the voltage also increases the SNM during read operation [25]. In 9T SRAM cell the values of RSNM is decreases due to decrease the technology as indicated in *figure 6(a)*. The lowest value of RSNM is 170.2mV at 14nm technology.

3.4 Write Static Noise Margin (WSNM)

There are several topologies to enhance the WSNM value reported in literature [26, 27]. The WSNM can be improved by reducing the supply voltage or increase the virtual ground

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voltage of SRAM cell [28]. The WSNM of the SRAM cell is calculated using the butterfly curve [29]. The WSNM is 42% enhance against the conventional 9T SRAM cell [33].

3.5 Delay Calculation

3.5.1 Read and Write Access Time

The delay in SRAM cells is divided into two types: read and write access time. Read access time is the time that is required for data from storage node to appear on both bit-lines, while write access time is the time that is required for data from the write driver circuit to appear on the storage nodes of the cell. Normally, the W/L ratio of the transistor and the supply voltage determine the delay in an SRAM cell. After comparing it is observed that the read and write access time of 9T SRAM cell is improved. *Figure 5(a)* depicts the write access time for the topologies considered at various supply voltages. It is noted that the write access time is decreases after increase the supply voltage. In case of technology decrease the write access time increases as shown in *figure 6(b).*

3.5.2 Read/ Write energy

One of the most important parameter used to describe the performance of a device or system is energy. The read/write energy of the 9T SRAM cell is displayed in *figure 5(b*) after increase the supply voltage. In *figure 5(b)* it is shown that the read energy values is increase after increase the supply voltage and also write energy value is firstly decrease up to 0.7 V after that it increases.

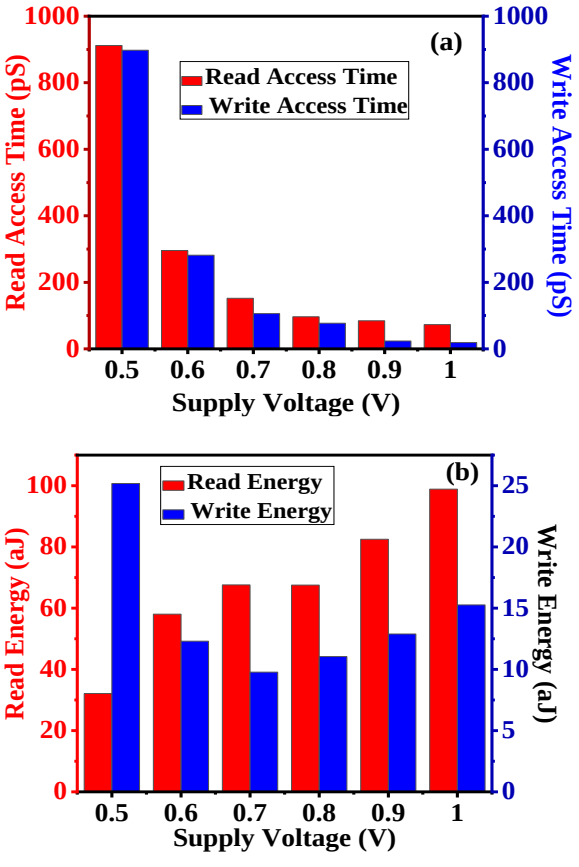

Figure 5: (a) Read and write access time at different supply voltage (b) Read and Write energy at different supply voltage [35]

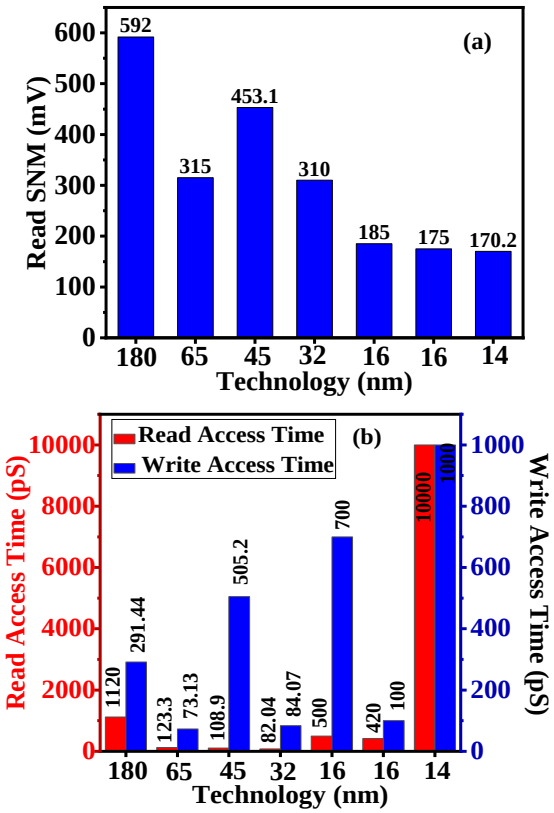

Figure 6: (a) Read SNM at different technologies (b) Read and Write access time at different voltage technology [35]

3.6 Area Comparison

The layout of the 9T SRAM cells are design based on CMOS design rule in ref. [36, 37]. The area for several of 9T SRAM cell is mention in the ref. [36, 37]. The layout is depend on the width of pull-up and pull-down transistor in the SRAM cell.

4. RESULT DISCUSSION OF EXISTING 9T SRAM

The performance of improvement as compared with existing work at various CMOS technology is shown in table 2-4 in terms of read & Hold SNM, read and write access time, leakage power and delay of 9T SRAM cell.

Table 2: Comparison of several parameters at various CMOS technology

Technology	Supply Voltage	Read SNM	Hold SNM	Standby power	Read Access Time	Write Access Time
180nm [12]	NA	592 mv	596 mv	NA	1.12 ns	291.44 ps
65nm [13]	0.6v	315 mv	na	2.58 nw	123.3 ns	73.13ps
45nm [14]	NA	453.1 mv	459.9 mv	NA	108.9 ps	505.2 ps
32nm [13]	0.6v	310 mv	na	4.951n w	82.04 ps	84.07ps
16nm [15]	0.6v	185 mv	180 mv	NA	0.5 ns	0.7 ns
16nm [16]	0.7v	175 mv	NA	NA	420ps	100ps
14nm [17]	0.4v	170.2 mv	NA	NA	10ns	1 ns

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Table 3: Comparison of Leakage power and delay at different CMOS technology of 9T SRAM

Technology	Leakage Power (µW)	Delay (ns)	Ref.
90nm	62.64	0.98	[9]
65nm	25.87pW	NA	[18]
32nm	33.38 nW	4.271 pS	[19]
16nm	2.9 nW	NA	[15]

Table 4: Comparison of read, write of delay, SNM, and power at different CMOS technology

Technology	Read delay	Write delay	Read SNM	Write SNM	Read Power	Write Power
180nm [20]	0.388 ps	0.181 ns	NA	NA	NA	NA
90nm [21]	98.85 ps	10ps	NA	NA	NA	NA
65nm [18]	NA	NA	447.5 mV	390m V	4.74 µW	257.5 µW
45nm [22]	NA	NA	453.1 mV	NA	77.19 nW	59.64 nW
16nm [15]	0.7nS	0.6nS	NA	NA	3.5 µW	1.1 µW

Table 5: Comparison of different 9T SRAM cell at 65nm technology

Parameters	**9T [30]**	**9T [31]**	**9T [32]**	**9T [33]**
Supply Voltage (V)	0.6	0.6	1.2	0.6
RSNM (mV)	250	210	470	225
WSNM (mV)	170	270	500	228
Static power dissipation	NA	NA	521nW	240pW
Write delay	1.2ns	7.9ns	NA	150ps
Read delay	3.7ns	609ns	NA	32ps
Area (µm)2	1.893	NA	1.768	8.03

To compares the performance parameters such as SNM, read and write access time and delay for various CMOS based 9TSRAM cell technologies in the tabulated form (Table 1-4). It is noted that the read and write delay is reduced with various scaled technologies by keeping the supply voltage. Herein, a CMOS based analysis of a 9T SRAM cell is done to determine the impact on its performance parameters i.e. SNM, read SNM, write RSNM, delay. In terms of cell stability, or SNM and delay, its disseminating improvement in comparison with already existing work is shown in *Table 1-4* in terms of cell stability i.e. SNM and delay [12-34].

5. CONCLUSION

This review has focused on the 9T SRAM cell using CMOS technology relevance for the storing data. The comparisons of 9T SRAM have been discussed by various CMOS technology (180nm, 90nm, 65nm, 45nm, 32nm, 14nm). 9T SRAM cell were analyzed taking into account various performance parameters like propagation delay, read/write SNM, read/write energy, read/write access time etc. with an aim to develop the understanding required for better performance. Different approaches, strategies have been displayed including incorporation of different technology, their cross coupled CMOS inverter and access pass transistor. The existing structure of 9T SRAM cell have their advantage as well as disadvantage and hence the way towards designing better performing SRAM is still a challenges and thus it can be seen as an area hosting immense opportunities for research. The constancy of 9T SRAM cell of all performance parameter is discussed in the form of tabulated. As a result of the thorough survey and comparison study conducted in this research, it can be stated that an SRAM cell can be constructed to be more potent by improving the trade-off between different performance parameters. In the future work, we will design a reversible logic gate based 9T SRAM cell having the better performance and low power consumption as compare to the existing 9T SRAM cell discussed in this review paper. The reversible logic gate will use in the row decoder and column decoder to reduce the power consumption.

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