

Current Conveyor Transconductance Amplifier (CCTA) based Grounded Memcapacitor Emulator

Anant Sinha¹, Bhawna Aggarwal², Shireesh Kumar Rai³ and Shweta Gautam⁴

^{1,2,4}ECED, Netaji Subhas University of Technology, New Delhi, India, ¹anantsinha897@gmail.com, ²kbhawnaagarg@yahoo.co.in,

⁴shwetautiet11@gmail.com

³ECED, Thapar Institute of Engineering and Technology, Patiala, Punjab, India, shireesh.raai@gmail.com

*Correspondence: Bhawna Aggarwal; Email: kbhawnaagarg@yahoo.co.in

ABSTRACT- A new emulator circuit for designing memcapacitor is proposed in this work. The suggested circuit is designed using a current conveyor transconductance amplifier (CCTA), a memristor and a capacitor. Behaviour of the proposed circuit has been examined for a frequency range of 0.6Hz to 6.4Hz with the help of simulations performed in LTSPICE using TSMC 180nm process parameters. It has been observed that the area inside lobes reduces with increase in frequency. In comparison to other emulators reported in literature, the suggested circuit uses fewer passive components and does not require analog multipliers, thus making it simple to design. The correctness and efficacy of the proposed design are verified using transient analysis, non-volatility analysis, and pinched hysteresis loops.

Keywords: Memcapacitor, CCTA, Emulator, Mem-element.

ARTICLE INFORMATION

Author(s): Ananta Sinha, Bhawna Aggarwal, Shireesh Kumar Rai and Shweta Gautam

Received: 28/02/2022; **Accepted:** 18/07/2022; **Published:** 10/08/2022;

e-ISSN: 2347-470X;

Paper Id: IJEER100306;

Citation: 10.37391/IJEER.100306

Webpage-link:

<https://ijeer.forexjournal.co.in/archive/volume-10/ijeer-100306.html>

This article belongs to the Special Issue on **Recent Advancements in the Electrical & Electronics Engineering**

Publisher's Note: FOREX Publication stays neutral with regard to Jurisdictional claims in Published maps and institutional affiliations.



1. INTRODUCTION

Prof. Leon Chua discovered the fourth basic passive circuit element, memristor, in 1971. This element satisfies the hidden relationship between magnetic flux (ϕ) and electric charge (q). Chua has theoretically explained that a memristor is a non-linear device whose resistance is determined by the charge that has passed through it. Thus, it behaves like non-linear resistance with memory [1-5]. In 2008, scientists at Hewlett-Packard laboratories realized the first physical model of memristor using titanium dioxide (TiO_2) and platinum electrodes [6-11]. Three fundamental properties of memristor can be stated as (a) pinched hysteresis curve formed between voltage and current when sinusoidal voltage is applied; (b) area inside the hysteresis loop and frequency are inversely related; (c) at higher frequencies memristor will behave like a normal resistor [12-15]. Prof. Chua later introduced two more members of mem-element family as memcapacitor and meminductor. These elements are based on the concept of memristor and possess memory behaviour through capacitance and inductance. Mem-elements offer a wide range of applications such as non-volatile memory applications (NVMAs), neuromorphic circuits, analog filters, programmable logic, signal processing, etc. The memcapacitor forms a relationship between flux (ϕ) and

integral of charge (σ). In 2009, Chua along with Di Ventra and Pershin reported a general model for memcapacitor system [15-20]. Equation defining n^{th} order voltage regulated memcapacitor is given as:

$$q(t) = M_C(x, V_C, t)V_C(t) \quad (1)$$

The charge stored in capacitor at time t is denoted by $q(t)$, the voltage is denoted by $V_C(t)$, and the memcapacitance is denoted by M_C . According to equation (1), memcapacitance depends on the state of the system. Pinched hysteresis curve is drawn between $q(t)$ and $V_C(t)$. Similarly, n^{th} order charge regulated memcapacitor can be defined as:

$$V_C(t) = M_C^{-1}(x, q, t)q(t) \quad (2)$$

Here, M_C^{-1} represents inverse memcapacitance.

The paper is divided into five sections, first of which is the introduction. Section 2 provides literature review. The characteristics of CCTA are presented in section 3. Proposed memcapacitor emulator circuit is presented in section 4. In section 5, the simulation results are reported. Section 6 has concluding observations.

2. LITERATURE REVIEW

In literature, various active building blocks are utilized for the realization of memcapacitor emulators. In [14] memcapacitor was realized for the first time using an operational amplifier, a memristor, a resistor, and a capacitor. In [13] memcapacitor was realized using a mutator circuit. Mutator translates the memristor behavior to memcapacitor. Two AD844 ICs, a resistor and a capacitor were used to realize the mutator circuit. In [12] memcapacitor emulator was realized using four second-generation current conveyor (CCII) blocks, a memristor, a resistor and an inductor. In [11] the reported circuit comprises of an analog multiplier, two operational amplifiers, a current-controlled current source, two resistors, and three capacitors. The circuit reported in [10] employs two current feedback

operational amplifiers (CFOAs), a multiplier, a resistor, two capacitors and a diode. In [9] the proposed circuit is realized using four CCII blocks, two resistors, one capacitor, and a memristor emulator. The memristor emulator is designed using two OP-AMPS, seven resistors, a capacitor, and a multiplier. In [7] the proposed emulator circuit was realized using an active device namely differential voltage current conveyor transconductance amplifier (DVCCTA), two capacitors, and one resistor. The circuit proposed in [6] utilizes an OP-AMP, a resistor, a capacitor, and a memristor. In [5] the proposed emulator circuit was realized using a dual X current conveyor differential input transconductance amplifier (DXCCDITA), 2 capacitors, and a resistor. The circuit reported in [4] was designed using 2 CCIIs, 3 capacitors, a resistor, and a multiplier. In [3] the proposed circuit utilizes voltage differencing current conveyor (VDCC) as an active block along with one capacitor and a memristor emulator. The memcapacitor emulator circuit proposed in [2] comprises two current conveyors, one Operational Transconductance Amplifier (OTA), two resistors, and two capacitors. The emulator circuit proposed in [1] was realized using a voltage differencing transconductance amplifier (VDTA), a memristor emulator, and a capacitor. The memristor emulator is also realized using a VDTA. It has been observed that most of the circuits, reported in literature for the realization of memcapacitor emulators are very complex. Many of them have either employed more than one active building block or an Analog multiplier. These circuits require many passive components. The memcapacitor emulator circuit proposed in this paper requires only one active device: CCTA along with a memristor, and a capacitor. No additional resistors are required.

3. CHARACTERISTICS OF CCTA

CCTA was introduced by Prokop and Musil [18-21] in 2005 as a novel active building block specifically designed for current-mode analog signal processing applications. It is a popular choice of designers for realization of hybrid circuits. CCTA is a two-stage device, first stage comprises CCII and the second stage is a transconductance stage, which employs an OTA. Figure 1 shows the block diagram of CCTA.

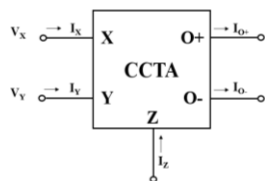


Figure 1: CCTA Block diagram

The input characteristics of CCTA can be described with the help of the current conveyor. The current drawn out of current conveyor stage is available at 'Z' terminal. The transconductance stage processes the voltage available at 'Z' terminal and translates it into two output currents having opposite polarity. The transconductance can either remain fixed or it can be electronically tuned. The following matrix equations illustrate the characteristics of CCTA.

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \\ I_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & \pm g_m & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ V_Z \\ V_O \end{bmatrix} \quad (3)$$

$$g_m = \frac{I_B}{2V_T} \quad (4)$$

here, V_T is thermal voltage and I_B represents the biasing current of OTA.

Current conveyors are active devices with unity gain. These devices offer various advantages as compared to voltage mode circuits such as large dynamic range, high linearity etc. CCII is considered as a fundamental block for the realization of current-mode circuits [2-3]. It is a three-terminal device as shown in figure 2.

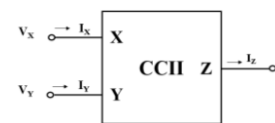


Figure 2: CCII Block diagram

The following port equations illustrate the behaviour of CCII.

$$I_Y = 0, V_X = V_Y, I_Z = I_X \quad (5)$$

An OTA is an active device that functions in the same way as a voltage-controlled current source (VCCS). In the dominion of Analog signal processing, it has numerous applications. The transconductance (g_m) of OTA can be electronically tuned with the use of differential input voltage [19].

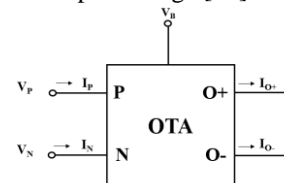


Figure 3: OTA Block diagram

The feature of electronic tunability makes OTA a popular choice among designers. The block diagram of OTA is shown in figure 3. Port equations of OTA can be given as:

$$\begin{bmatrix} I_P \\ I_N \\ I_{O+} \\ I_{O-} \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ g_m & -g_m \\ -g_m & g_m \end{bmatrix} \begin{bmatrix} V_P \\ V_N \end{bmatrix} \quad (6)$$

I_P and I_N are input currents that are available at P and N terminals. I_{O+} and I_{O-} represent currents drawn from the output terminals O+ and O-.

Implementation of CCTA using CCII and OTA is shown in figure 4 [16].

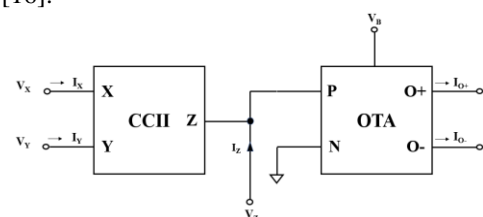


Figure 4: CCTA using CCII and OTA

4. PROPOSED MEMCAPACITOR EMULATOR

Figure 5 shows the proposed grounded memcapacitor emulator circuit. It is designed with a CCTA, a memristor, and a capacitor.

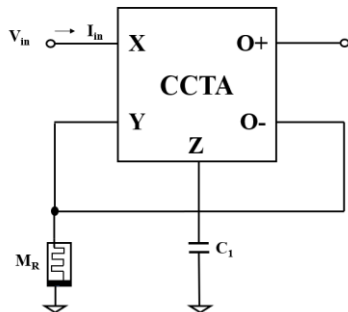


Figure 5: Proposed memcapacitor emulator

Following equations can be derived by performing routine analysis of the proposed circuit.

$$V_Y = g_m V_Z M_R \quad (7)$$

Using equation (3) and (7), V_Z can be computed as:

$$V_Z = \frac{V_{in}(t)}{g_m M_R} \quad (8)$$

$$V_Z = \frac{1}{C_1} \int I_Z(t) dt \quad (9)$$

Since, $I_Z = I_X = I_{in}$, hence equation (9) can be rewritten as:

$$V_Z = \frac{1}{C_1} \int I_{in}(t) dt \quad (10)$$

Using equation (8) and (10), we get,

$$\frac{V_{in}(t)}{g_m M_R} = \frac{1}{C_1} \int I_{in}(t) dt = \frac{1}{C_1} q_{in}(t) \quad (11)$$

Value of charge $q_{in}(t)$ can be computed as:

$$q_{in}(t) = \frac{C_1 V_{in}(t)}{g_m M_R} \quad (12)$$

By comparing equation (12) with (1), we can determine the value of memcapacitance M_C .

$$M_C = \frac{C_1}{g_m M_R} \quad (13)$$

Equation (13) shows that the memcapacitance of the proposed circuit is dependent on CCTA transconductance (g_m), capacitance (C_1), and memristance M_R .

5. SIMULATION RESULTS AND DISCUSSION

To demonstrate the memcapacitive behavior of the proposed design, transient analysis has been carried out using a 100mV amplitude sinusoidal voltage with a 5Hz frequency and a 90° phase shift. Figure 6 depicts the response.

One of the significant characteristics associated with all the mem-elements is non-volatility. The proposed memcapacitor emulator's non-volatility is investigated by observing the

voltage V_Z by applying a 10mV pulse signal having a time period of 1.2s and ON time of 0.5s, where V_Z is the voltage at Z terminal, representing charge (q). Observed results are plotted in Figure 7.

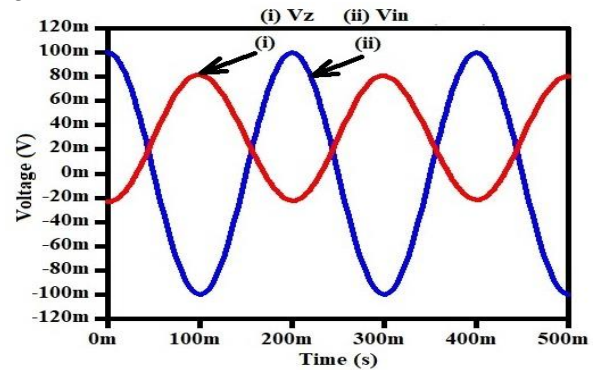


Figure 6: Transient response of memcapacitor emulator at 100mV, 5Hz sinusoidal

During ON period of the pulse an abrupt change in the value of V_Z can be observed, while the value of voltage is retained during OFF time. Hence the memory retaining property is verified for the proposed memcapacitor emulator.

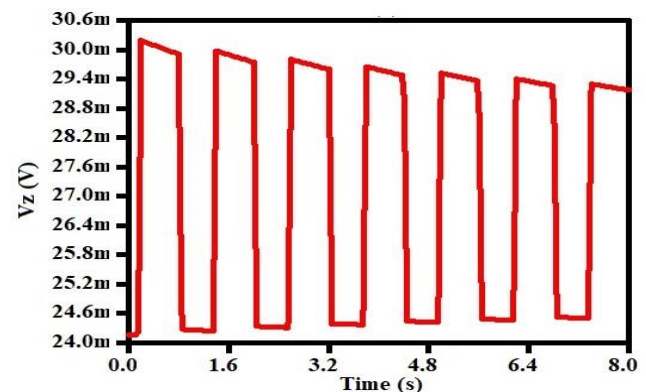


Figure 7: Non-volatile behavior obtained with 10mV pulse signal of 1.2s period with ON time of 0.5s

The pinched hysteresis loop plotted between V_{in} and V_Z is shown in figure 8. An 85μA sinusoidal signal with a frequency of 5Hz has been used to generate the curve. The value of capacitance C_1 is kept fixed at 1pF.

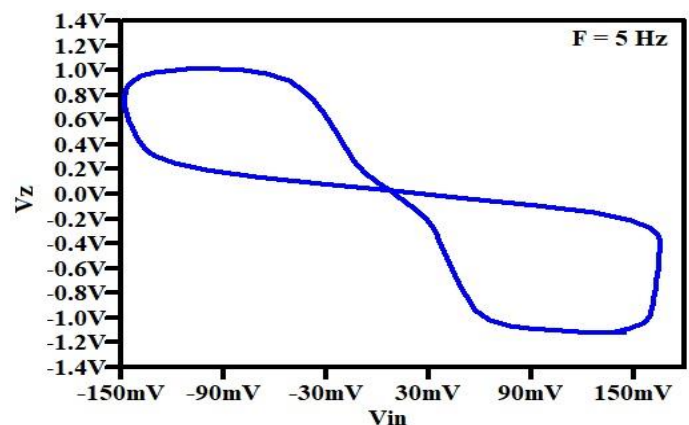


Figure 8: Pinched hysteresis curve with 85μA sinusoidal signals and 5Hz frequency

Pinched hysteresis loops at 0.6Hz, 0.8Hz, and 1Hz are shown in figure 9. It has been observed that as the frequency changes, the shape of the curve changes, also the area inside the loop varies inversely with the frequency.

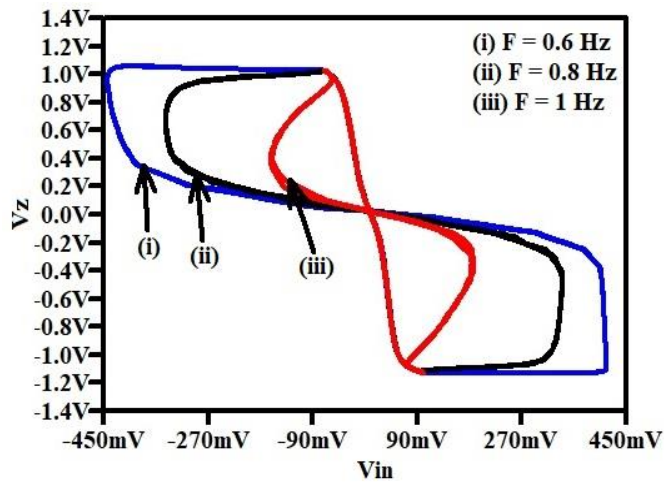


Figure 9: Pinched hysteresis curve with 85μA sinusoidal signals and frequencies 0.6Hz, 0.8Hz and 1Hz

Figure 10 shows pinched hysteresis loops obtained at 5.3Hz, 5.9Hz, and 6.4Hz. All these curves are having pinched hysteresis loops at the zero-crossing point.

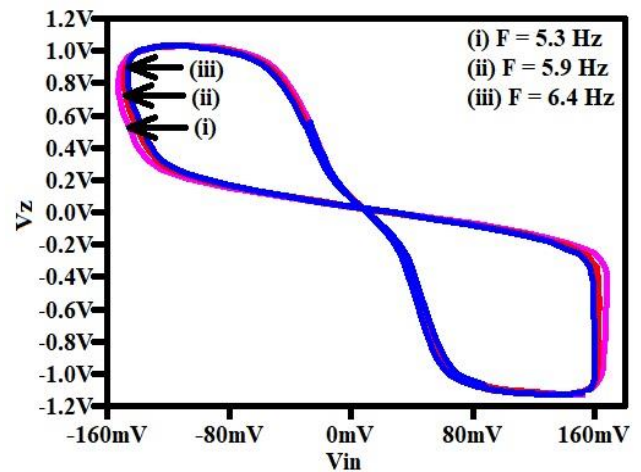


Figure 10: Pinched hysteresis curve with 85μA sinusoidal signals and frequencies 5.3Hz, 5.9Hz, and 6.4Hz

Table 1. Comparison of proposed circuit with existing circuits

Ref.	Active Devices	Passive Devices	Operating Frequency
[14]	1 OP-AMP	1 capacitor, 1 resistor, 1 memristor	8 Hz
[13]	2 AD844	1 memristor, 1 resistor, 1 capacitor	1 Hz
[12]	4 CCIIIs	1 resistor, 1 inductor, 1 memristor
[11]	2 OP-AMPs, 1 multiplier, 1 current-controlled current source	3 capacitors, 2 resistors	10 Hz
[10]	2 CFOAs, 1 multiplier	1 resistor, 2 capacitor, 1 diode	25 Hz
[9]	4 CCIIIs	2 resistors, 1 capacitors, 1 memristor	12 Hz
[7]	1 DVCCCTA	2 capacitors, 1 resistor	900 KHz
[6]	1 OP-AMPS	1 resistor, 1 capacitor, 1 memristor
[5]	1 DXCCDITA	2 capacitors, 1 resistor	500 KHz
[4]	2 CCIIIs, 1 multiplier	3 capacitors, 1 resistor	500 Hz
[3]	1 VDCC	1 capacitor, 1 memristor	700 KHz
[2]	2 CCIIIs, 1 OTA	2 resistors, 2 capacitors	500 KHz
[1]	1 VDTA	1 capacitor, 1 memristor	150 Hz
Proposed circuit	1 CCTA	1 capacitor, 1 memristor	6.4 Hz

6. CONCLUSION

A memcapacitor emulator based on CCTA, a memristor, and a capacitor is presented in this paper. Pinched hysteresis loops obtained from simulations confirms the operation of the proposed circuit for a frequency range of 0.6Hz to 6.4Hz. The area of the lobes has been found to be reducing with increase in frequency. Furthermore, non-volatility test confirms the memory characteristic of the proposed circuit. When compared with emulators available in literature, the proposed design has been found to be simple, requiring no analog multiplier and

only a few passive components. The proposed circuit can be utilized for the realization of chaotic oscillator.

REFERENCES

- [1] Hosbas, M. Z., Kaçar, F., & Yesil, A. (2022). Memcapacitor emulator using VDTA-memristor. *Analog Integrated Circuits and Signal Processing*, 110(2), 361–370. <https://doi.org/10.1007/s10470-021-01974-0>
- [2] Raj, N., Ranjan, R. K., Khateb, F., & Kumngern, M. (2021). Mem-elements emulator design with experimental validation and its application. *IEEE Access*, 9, 69860-69875.

- [3] Singh, A., & Rai, S. K. (2021). VDCC-based memcapacitor/meminductor emulator and its application in adaptive learning circuit. *Iranian Journal of Science and Technology, Transactions of Electrical Engineering*, 45(4), 1151-1163.
- [4] Yesil, A., & Babacan, Y. (2021). Electronically controllable Memcapacitor circuit with experimental results. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 68(4), 1443-1447. <https://doi.org/10.1109/tcsii.2020.3030114>
- [5] Vista, J., & Ranjan, A. (2020). Simple charge controlled floating memcapacitor emulator using DXCCDITA. *Analog Integrated Circuits and Signal Processing*, 104(1), 37-46. <https://doi.org/10.1007/s10470-020-01650-9>
- [6] Romero, F. J., Morales, D. P., Godoy, A., Ruiz, F. G., Tienda-Luna, I. M., Ohata, A., & Rodriguez, N. (2019). Memcapacitor emulator based on the Miller effect. *International Journal of Circuit Theory and Applications*, 47(4), 572-579. <https://doi.org/10.1002/cta.2604>
- [7] Vista, J., & Ranjan, A. (2019, March). Design of memcapacitor emulator using DVCCTA. In *Journal of Physics: Conference Series* (Vol. 1172, No. 1, p. 012104). IOP Publishing.
- [8] Adhikari, S. P., Sah, M. P., Kim, H., & Chua, L. O. (2013). Three fingerprints of memristor. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 60(11), 3008-3021.
- [9] Yu, D. S., Liang, Y., Chen, H., & Iu, H. H. (2013). Design of a practical memcapacitor emulator without grounded restriction. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 60(4), 207-211.
- [10] Sah, M. P., Yang, C., Budhathoki, R. K., Kim, H., & Yoo, H. J. (2013). Implementation of a memcapacitor emulator with off-the-shelf devices. *Elektronika ir elektrotehnika*, 19(8), 54-58.
- [11] Fouda, M. E., & Radwan, A. G. (2012). Charge controlled memristor-less memcapacitor emulator. *Electronics letters*, 48(23), 1454-1455.
- [12] Pershin, Y. V., & Di Ventra, M. (2010). Emulation of floating memcapacitors and meminductors using current conveyors. *arXiv preprint arXiv:1011.4620*.
- [13] Bielek, D., & Biolkova, V. (2010). Mutator for transforming memristor into memcapacitor. *Electronics letters*, 46(21), 1.
- [14] Pershin, Y. V., & Di Ventra, M. (2009). Memristive circuits simulate memcapacitors and meminductors. *arXiv preprint arXiv:0910.1583*.
- [15] Di Ventra, M., Pershin, Y. V., & Chua, L. O. (2009). Circuit elements with memory: memristors, memcapacitors, and meminductors. *Proceedings of the IEEE*, 97(10), 1717-1724.
- [16] Jaikla, W., Silapan, P., Chanapromma, C., & Siripruchyanun, M. (2009, February). Practical implementation of CCTA based on commercial CCII and OTA. In *2008 International Symposium on Intelligent Signal Processing and Communications Systems* (pp. 1-4). IEEE.
- [17] Strukov, D. B., Snider, G. S., Stewart, D. R., & Williams, R. S. (2008). The missing memristor found. *nature*, 453(7191), 80-83.
- [18] Prokop, R., & Musil, V. (2005). New modern circuit block CCTA and some its applications. In *The Fourteenth International Scientific and Applied Science Conference-Electronics ET* (Vol. 2005, pp. 93-98).
- [19] Sanchez-Sinencio, E., & Silva-Martinez, J. (2000). CMOS transconductance amplifiers, architectures and active filters: a tutorial. *IEEE proceedings-circuits, devices and systems*, 147(1), 3-12.
- [20] Chua, L. (1971). Memristor-the missing circuit element. *IEEE Transactions on circuit theory*, 18(5), 507-519.
- [21] Sedra, A., & Smith, K. (1970). A second-generation current conveyor and its applications. *IEEE Transactions on circuit theory*, 17(1), 132-134.



© 2022 by the Anant Sinha, Bhawna Aggarwal, Shireesh Kumar Rai and Shweta Gautam. Submitted for possible open access publication under the terms and conditions of the Creative Commons Attribution (CC BY) license (<http://creativecommons.org/licenses/by/4.0/>).