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Voltage Differencing Buffered Amplifier (VDBA) Based Grounded Meminductor Emulator

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ABSTRACT- A new meminductor emulator using a capacitor, a memristor and a voltage differencing buffered amplifier (VDBA) is proposed in this paper. This reported realization of meminductor is very simple than proposed in literature as it needs only 1 active block. The proposed emulator has been found suitable for low frequency operations with electrical tunability, and multiplier free topology. The characteristics of the proposed emulator have been verified for a frequency range of 1.8Hz to 4.9Hz using the LTspice simulation tool with 180nm CMOS technology parameters. Pinched hysteresis loops observed in flux versus current plane verifies its meminductive behavior. Moreover, the non-volatility test of the proposed emulator proves its memory behavior. The pinched hysteresis loops obtained through simulations show that the lobe area reduces with increase in frequency.

Keywords: VDBA; meminductor; Pinched hysteresis loop; memristor.

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1. INTRODUCTION

Earlier there were only three known fundamental circuit elements: inductors, resistors, and capacitors. L. Chua [25] in 1971, proposed a fourth fundamental circuit element named memristor [25]. Its memristive concepts were studied in detail in 1976. However, this theory was not of much use until its first physical realization was done using TiO_2 in 2008 by HP labs [24]. After the realization, this idea of memristor has been extended to capacitors and inductors giving the concept of memcapacitor and meminductor [21]. All these elements: memcapacitor, meminductor, and memristor have memory retaining capabilities and hence their performances are affected by past values [1]. However, these devices' elements are not available in commercial form, so researchers discovered their alternative in the form of emulators [20]. The memcapacitor and meminductor emulators were created with the help of resistors, capacitors, operational amplifiers (op-amps), operational transconductance amplifiers (OTAs), and memristors. Various meminductor emulator realizations have been proposed in the literature. In [22], a meminductor emulator realization using a second-generation current conveyor (CCII), op-amp, floating memristor emulator, multiplier, one capacitor, and three resistors has been proposed. In the emulator design proposed in [9], a generalized emulator has been designed using two AD844s, a memristor, a resistor, and a capacitor that can imitate the behavior of a meminductor and a memcapacitor. Three trans-impedance operational amplifiers, a floating memristor, buffers, resistors, and capacitors were used to create a universal mutator [10]. As evidenced from the literature review, the designing of meminductor emulators can be broadly categorized into two categories. The first approach majorly depends on creating meminductor emulators by transforming a memristor emulator using a mutator circuit. This is the primary strategy backed by the majority of meminductor emulator circuits published in the literature. The downside of this technique is that meminductor emulator characteristics are inextricably linked to memristor emulator features. The memristor-less architecture of the meminductor emulator is the second approach. The circuits of the meminductor emulators that are designed using the second method are complex because of an excessive number of active/passive components and analog multiplier. The objective of this work has been to design a meminductor emulator with a simple structure. The work in this paper has been carried out with the aim of designing a robust meminductor emulator circuit with fewer active and passive components which are free from the requirement of a multiplier. The proposed meminductor emulator has been designed using a VDBA, a memristor, and a capacitor. The paper is divided in *6 Sections* including the introduction section. The properties of VDBA have been discussed in *Section 2*. The methodology of the proposed meminductor emulator along with its mathematical analysis is given in *Section 3*. LTspice simulation results of the proposed emulator are presented in *Section 4*. A comparison with state-of-the-art meminductor emulators has been given in *Section 5*. This paper's conclusion is given in the *Section 6*.

2. CHARACTERISTICS OF VDBA

In *Figure 2* of MOS-based VDBA, it's a combination of voltage to current converter (or transconductance amplifier) and the voltage follower.

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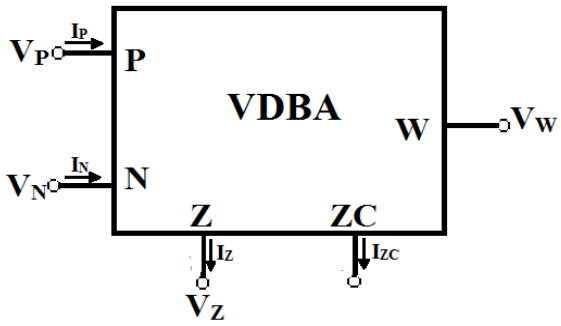

Figure 1: VDBA block [18]

In *Figure 1* VDBA block diagram depicting various terminals and the corresponding port currents is shown. It has a pair of high-impedance input voltage terminals (V_N and V_P), a low-impedance output voltage terminal (V_W), and a high-impedance output current terminal (I_Z). Matrix equation of VDBA, depicting its terminal properties is given as:

$$\begin{bmatrix} I_P \\ I_N \\ I_Z \\ I_{ZC} \\ V_W \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ gm & -gm & 0 \\ -gm & gm & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_p \\ V_N \\ V_Z \end{bmatrix} \quad (1)$$

where g_m denotes the transconductance gain of VDBA and is given as:

$$g_m = \frac{\sqrt{\beta_1 \beta_9}}{\sqrt{2}} (V_{B1} - V_{SS} - V_{th}) \quad (2)$$

here, b_1 and b_9 are transconductance parameters of MOSFET M1 and M9 respectively, V_{B1} is DC biasing voltage applied at the gate terminal of MOSFET M9 and V_{th} is the threshold voltage of NMOS. The MOS-based circuit of voltage differencing buffered amplifier (VDBA) in *Figure 2* is an alternative active building block that is slew-free and handles voltage signals. The VDBA, as its name implies, employs a voltage differencing input stage and generates a current output that is equal to the multiplication of the transconductance gain and differential input voltage. The fact that the transconductance has a biased current dependent allows for electrical circuit parameter tweaking [9]. As a result, the circuit design is simpler, with fewer passive components. It also has a buffered voltage output, resulting in architectures that are easily cascadable [10]. Furthermore, the VDBA's ability to output both voltage and current adds to the design freedom [11]. As a result, for the analog application, VDBA has emerged as a viable option.

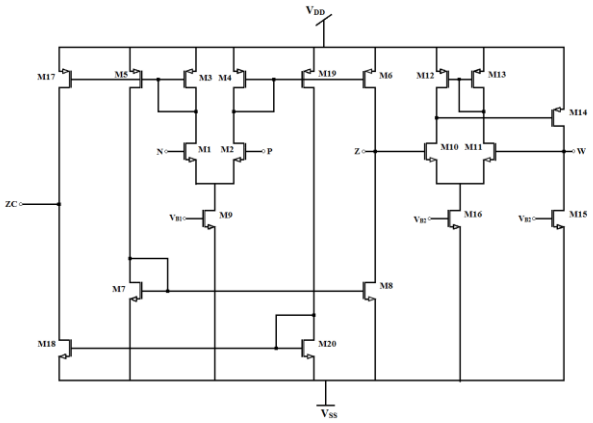

Figure 2: MOS based Circuit diagram of VDBA block [18]

3. METHODOLOGY AND PROPOSED MEMIDUCTOR EMULATOR

The complete circuit of VDBA based proposed meminductor emulator is shown in *Figure 3.* It consists of a memristor M_R connected between nodes N and W of VDBA. A floating capacitor is connected between nodes Z and ZC. The input voltage is applied at node N. From *Figure 3 i*t can be analyzed that the circuit needs only 1 active block (VDBA), 1 memristor, and 1 capacitor for its realization. In this circuit, none of the terminals of VDBA is left open, giving low noise architecture. Furthermore, one of the differential input terminals of VDBA (p-terminal) is grounded leading to the robust configuration preferred by circuit designers.

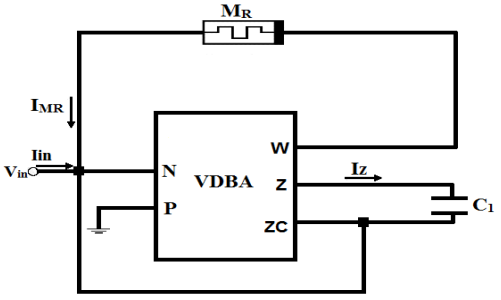

Figure 3: Proposed VDBA-based Meminductor Emulator

For a meminductor understanding, variables *p* and q are used *q* is the time integral of current (*I(t)*) and *p* is the time integral of flux *Φ(t)*and are mathematically defined as

$$p(t) = \int_{-\infty}^{t} \Phi(t)\, dt \quad (3)$$

$$q(t) = \int_{-\infty}^{t} I(t) dt \quad (4)$$

Meminductance (M_L) of a meminductor is characterized by the following relation [25]:

$$\Phi(t) = {}_{M_L} I(t) \quad (5)$$

A meminductor is characterized by pinched hysteresis loop observed in *Φ(t) vs. I(t*) plane. The flux *Φ(t)* of the meminductor is defined as:

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$$\Phi(t) = \int V_{in}(t)\,dt \quad (6)$$

where $V_{in}(t)$represents the applied input voltage at the meminductor. Performing routine analysis of the circuit and using characteristic port equations of VDBA Eq. (1), the current equations obtained at different terminals of the emulator circuit are given as:

$$\left.\begin{aligned} I_{in} + I_{MR} &= 0 \\ I_{MR} = I_W &= \frac{V_W - V_{in}}{M_R} \\ I_Z &= g_m (V_Z - V_{in})\, sC_1 \end{aligned}\right\} \quad (7)$$

Further simplifying Eq.(7) using Eq.(1), the equations obtained are as follows:

$$\left.\begin{aligned} (sC_1 - g_m)V_{in} &= sC_1 V_Z \\ I_{MR} &= \frac{V_Z - V_{in}}{M_R} \end{aligned}\right\} (8)$$

Substituting Eq. (7) in Eq. (8), along with port equations given by Eq. (1), after simplification yields:

$$I_{in} = V_{in}\frac{g_m}{sC_1 M_R} \quad (9)$$

Expressing Eq. (9) in time domain form, we get:

$$I_{in}(t) = \frac{g_m}{C_1 M_R}\int V_{in}(t)\,dt \quad (10)$$

Using Eqs. (6) and (10) can be written as:

$$I_{in}(t) = \frac{g_m}{C_1 M_R}\Phi(t) \quad (11)$$

Comparing Eqs. (11) and (9) yields:

$$M_L = \frac{M_R C_1}{g_m} \quad (12)$$

M_L given by Eq. (12) represents the meminductance (M_L) of the proposed meminductor emulator and shows that it is directly dependent on capacitance (C_1), and memristance M_R, while it is inversely proportional to VDBA transconductance (g_m). In this configuration, the non-volatility characteristics are obtained due to 'M_R'. The proposed emulator circuit has the following advantages:

1. It possesses a very simple structure.
2. Realization is free from any multiplier requirement.
3. Structure is very robust, as one of the differential input terminals is grounded.
4. Less affected by noise, as none of the active block terminals is left open.

4. RESULTS AND DISCUSSIONS

The proposed meminductor emulator designs are simulated in the LTspice tool. A supply voltage of ±1.5V is provided to CMOS-based VDBA shown in *Figure 2*. For proper operation, a bias voltage of 100mV is connected to V_{B1} and V_{B2}. The aspect ratios of MOSFETs used in the design of CMOS-based VDBA block are summarized in *Table 1*.

Table 1: Aspect ratios of MOSFETs used in the design of CMOS based VDBA

MOSFET	W (µm) / L (µm)
M1, M2, M3, M4, M9, M10, M11, M15, M16	7/ 0.35
M5, M6, M17, M19	21/ 0.7
M7, M8, M18, M20	7/ 0.7
M12, M13, M14	14/ 0.35

The results of the suggested meminductor emulator's transient analysis are shown in *Figure 4*. A signal of 200mV amplitude, capacitor C_1 in the proposed meminductor has shown *Figure 3* is taken 45nF and 2Hz frequency has been used to observe this curve. It can be clearly analyzed from the transient response shown in *Figure 4 that* curves of input current I(V1) and V(flux) lead to the curve of the input voltage Vin(V), confirming the inductive behavior of the proposed emulator.

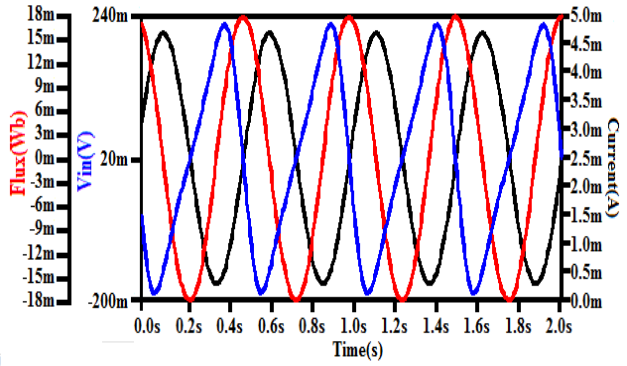

Figure 4: Transient response of meminductor emulator with a sinusoidal voltage signal of 200mV amplitude and 2Hz frequency

The non-volatility behavior observed with 20mV pulse signal of 5ms period with ON time of 1ms is shown in *Figure 5*, a linear increase of meminductance (M_L) value till particular value. In the non-volatility behavior shown in *Figure 5* it can be observed that the meminductance retains its value when the input pulse goes off and with the next pulse get ON its value starts from the previously stored meminductance (M_L) value. This behavior proves the memory retention characteristic of the proposed emulator.

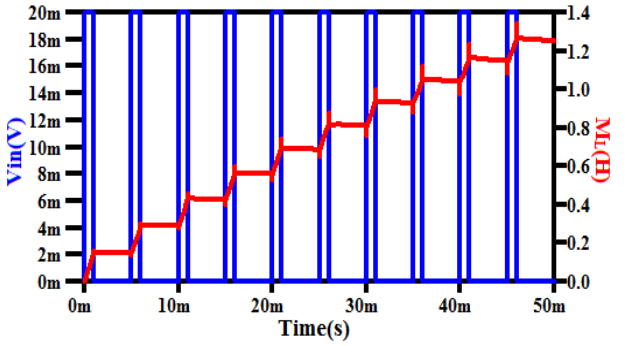

Figure 5: Non-volatility behavior observed with 20mV pulse signal of 5ms period having ON time of 1ms

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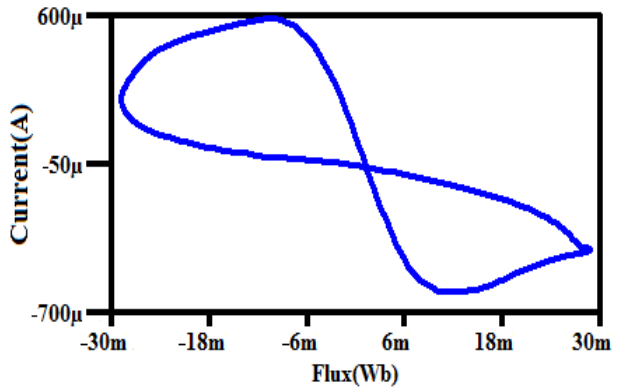

Figure 6: PHL curve between Φ(t) vs I(t) plane at 4.7Hz frequency

The simulation result observed in *Φ(t) vs. I(t)* plane is shown in *Figure 6*. Pinched hysteresis loop (PHL)with zero-crossing observed in the PHL curve between *Φ(t) vs. I(t)* shown in *Figure 6* confirms the meminductive behavior of the proposed circuit. *Figure 6* has been plotted for a sinusoidal input signal of 4.7Hz frequency and 850mV amplitude.

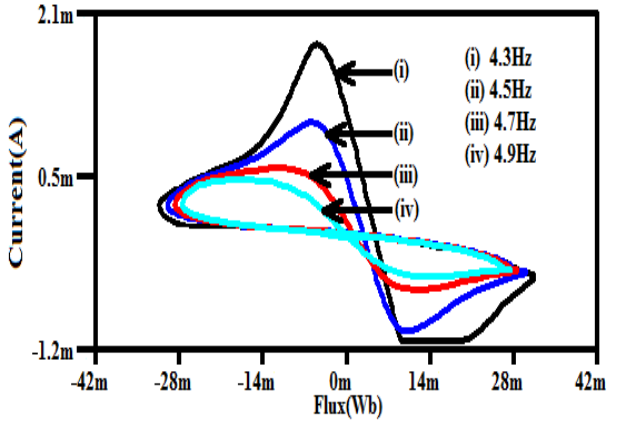

Figure 7: PHL between Φ(t) vs I(t) plane at frequencies 4.5Hz, 4.7Hz, and 4.9Hz

PHL curves observed at different frequencies of 4.3Hz, 4.5Hz, 4.7Hz, and 4.9Hz are shown in PHL between *Φ(t) vs I(t)* plane at *Figure 7*. Similar curves for frequencies 1.8Hz, 2Hz, and 2.2Hz are plotted in *Figure 8*. All these curves confirm that the increase in frequency area inside the lobes reduces.

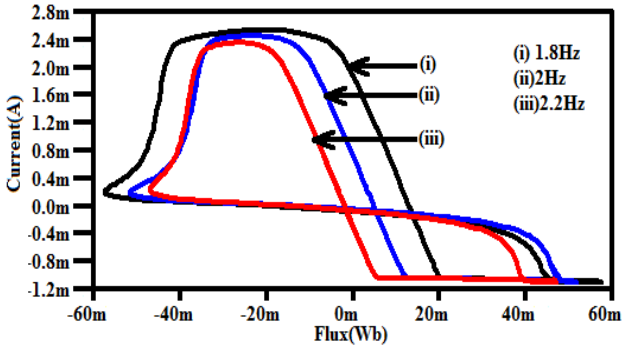

Figure 8: PHL between Φ(t) vs I(t) plane at frequencies 1.8Hz, 2Hz, and 2.2Hz

5. COMPARISON OF PROPOSED MEMINDUCTOR WITH STATE-OF-THE-ART MEMINDUCTORS AVAILABLE IN LITERATURE

To prove the usefulness of the proposed meminductor, the proposed emulator has been compared to meminductor emulators that have been mentioned in the literature. All the key parameters of the proposed meminductor emulator have been compared with various meminductors reported in *Table 2*, along with similar parameters of state-of-the-art meminductor emulators available in the literature. *Table 2* compares the proposed meminductor emulator to existing meminductor emulators in terms of operating frequency range and active/passive elements quantity.

Table 2: Comparison with various meminductors reported in literature

Ref.	Active Elements	Passive Elements	Operating Frequency
[22]	1 AD633, 5 Op amps, 8CCII+	3C, 11R	8Hz
[19]	2CCII,1 Memristor	1R,1C	-------
[9]	2AD844,1 Memristor	1R,1C	1KHz
[11]	2 Op-amps ,4CCII+	2C, 8R	36.9H
[12]	10 MOS transistors, 3-Op-amp,1Multiplier,	2R,2C,1L	300Hz
[13]	4 Op-amps, 2CCII+, 1 Multiplier	2C, 7R	800Hz
[17]	3AD844,1AD633, 3Opamp	2C, 10R	16Hz
[10]	1Multiplier ,3 Op-amps 3CCII+,1Memristor	3R,1C	21.1Hz
[14]	1Multiplier, 3CCII+, 1 Adder	2C,3R	10Hz
[15]	3Op-amp,1 Integrator	3R,2C	10Hz
[5]	4 AD844, Varactor diode, 1 Op-amp	1C,5R	8KHz
[6]	2Analog Multiplier , 7CCII ,1Op-amp	6R ,2C	5KHz
[7]	7 Op-amp	3C,14R	200Hz
[8]	2 VDTA	2C,1R	1MHz
[2]	1 CBTA ,1 Memristor	1C	200Hz
[3]	11 Multiplier ,9 Op-amp	26R	140Hz
[4]	1OTA ,2CCII, 1Multipler, 1CFOA	7R,2C	5KHz
Proposed Work	**VDBA, 1 Memristor**	**1C**	**4.9Hz**

From comparison with various meminductors reported in literature *Table 2*, the following points can be inferred for the proposed meminductor emulator:

1. Meminductor emulators reported in [6, 15, 20, 21, 24] use multiple active components, while the proposed meminductor emulator is implemented using only one VDBA hence it reduces the complexity of the proposed circuit.
2. The proposed meminductor emulator has no resistance, but the meminductor emulator is described in [6, 7, 8, 12,

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13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 24, 25] use resistance in their design. Resistance increases the size of the emulator and thermal dissipation of the circuit.

3. The meminductor emulators described in [8, 14, 15, 17, 20, 24, and 25] use multipliers in addition to active and passive elements, while the proposed meminductor emulator does not need any multiplier for its operation. The use multiplier in the circuit has required large value capacitors which produce low current.

6. CONCLUSION

A voltage differencing buffered amplifier, a memristor, and a capacitor have been used to create the suggested meminductor emulator. The suggested meminductor emulator operates for a frequency range from 1.8Hz to 4.9Hz. The non-volatility test confirms its memory behavior, and the pinched hysteresis loop proves its meminductive nature. PHL curves are observed to have a smaller area with an increase in frequency. The suggested emulator offers the advantages of simple circuitry, low voltage operation electrical tunability, and multiplier-free topology. It possesses a robust and less-noise structure, as one of its differential input terminals is connected to the ground and none of the VDBA terminals is left open. It is a good choice for circuit designers working in low-frequency zone. The VDBA can be realized using commercially available IC OPA860 and make the suggested meminductor economically viable.

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