FOREX Publication
Open Access | Rapid and quality publishing

International Journal of
Electrical and Electronics Research (IJEER)
Research Article | Volume 10, Issue 3 | Pages 501-507 | e-ISSN: 2347-470X

Multilevel Inverter with Predictive Control for Renewable Energy Smart Grid Applications

Abhimanyu Kumar[1] and Dr. Sanjay Jain[2]
[1]*Research Scholar, Department of Electrical Engineering, RKDF University, Bhopal (M.P), India,*
[2]*Associate Professor, Department of Electrical Engineering, RKDF University, Bhopal (M.P), India,*

***Correspondence:** Abhimanyu Kumar; Email: abhimanyurkdf@gmail.com

ABSTRACT- In a world where climate changes and power management are becoming increasingly important, research work focuses on renewable energy based smart grid to meet adequate demands of energy. The smart grid is a modernized autonomous power network that can transmit electricity effectively, conserve resources and costs, and increase the local grid's stability. As a result, a smart grid connected multilevel inverter is presented in this work. The inverter is controlled using a model predictive control algorithm with increased levels with the primary goal of controlling the injected power generated by the renewable source, improving the quality of the current waveform, lowering THD, and eliminating the shift phase among the injected current and the grid voltage in effort to match the smart grid network's requirements. Therefore, this paper aims to show the performance analysis of multilevel inverters with predictive control for renewable energy smart grids application. The major concern was observed with most of the multi-level inverters are that with increased level total harmonic distortion (THD) is increased if switching control is not designed properly. Therefore, in this case predictive control is implemented on renewable energy based smart grid inverters to increase level with minimum voltage THD and current THD. The case analyzed voltage and current THD in the different levels of multilevel inverter. The result analysis was performed on 7, 11, 17, 21, 27, 31, 37 and 41 respectively. From result analysis it was observed that minimum THD was observed with level 31, i.e., 0.35% and at level 41 it was increased up to 0.55% which is still not high as compared to other existing MLI architectures. The result findings of proposed approach decreased THD with varying levels and outperforms better as compared to other works.

Keywords: Inverter, Multilevel Inverters, Predictive Control, Renewable Energy, Smart Grid.

ARTICLE INFORMATION
Author(s): Abhimanyu Kumar and Dr. Sanjay Jain;
Received: 13/05/2022; **Accepted**: 10/08/2022; **Published**: 25/08/2022;
E- ISSN: 2347-470X;
Paper Id: IJEER220514;
Citation: 10.37391/IJEER.100317
Webpage-link:
https://ijeer.forexjournal.co.in/archive/volume-10/ijeer-100317.html

Publisher's Note: FOREX Publication stays neutral with regard to jurisdictional claims in Published maps and institutional affiliations.

1. INTRODUCTION

Power electronics inverters have become more significant nowadays for a variety of implementation, including motor drives system, electric power systems, as well as clean energy (which is renewable). Multilevel inverters had also now garnered considerable interest because of their various benefits, including high-quality output waveforms, reduced voltage stress upon switches, decreased switching losses, but also improved efficiency. Multilevel inverters MLIs work on the principle of employing a large quantity of semiconductor switches for doing power conversion using tiny voltage increments. These MLIs have been widely employed in high or medium power operations including variable-speed drives as well as static VAR compensator (SVC) reactive power compensation [1]. MLIs also were applied to low-power operations like solar power systems (PV) and hybrid e-mobiles. The neutral point clamped (NPC), recently developed flying capacitor (FC), and to produce inverted AC from separate DC sources the cascaded H-bridge (CHB), these considered as 3 fundamental topologies of MLI. The fundamental drawback of the NPC inverter is unmatched voltage sharing among series capacitors, which causes grossly imbalanced of DC-link capacitance and necessitates the use of extra clamping diodes [2]. Recently developed Flying capacitors are used as clamping diodes in the FC inverter. In compared to NPC inverters, this design provides a number of benefits, including equivalent voltage sharing across semiconductor switches. Such kind of topology, however, necessitates a large quantity of storage capacitors for high voltage steps. The cascaded H-bridge CHB inverters are made up of H-Bridge cells that are coupled in series including an isolated dc supply. Depending upon the values by dc voltage supply VS, the CHB inverters split into 2 major sections: symmetric and asymmetric topologies. The symmetric topology employs equal-valued dc input VS like battery or generator. This characteristic provides high modularity by giving only some levels as in output waveform when comparison with asymmetric one, that uses various dc VS to provide increased output voltage levels [3]-[5]. Multilevel inverters biggest drawback is the enormous amount of switches needed. As a result, much work has gone into developing novel MLI topologies with fewer power semiconductor devices (or say switches). A novel topology implementing cascaded multilevel inverters was described in [6]. MLI's novel design for a fuel-cell microgrid system includes a transformer-free 5-level MLI. To create five-levels, a simplified Multilevel inverters suggested in [7] employs just 6 power semiconductor devices (or say switches) rather of the 8 utilized in a standard cascaded H-Bridge MLI. Mentioned

FOREX Publication
Open Access | Rapid and quality publishing
International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 10, Issue 3 | Pages 501-507 | e-ISSN: 2347-470X

topology, however, necessitates the use of a step-up converter (DC to DC power convertor) as well as combination of Inductor and capacitor L-C filter. As growing output levels, several different topologies have been created to decrease usage of switches necessary.

2. RELATED WORK

In [8], author improved 13-level framework and analysis of PUC-MLI is suggested in this work. To eliminate harmonic, the suggested inverter employs 8 switches device and 3 Voltage sources, which are effectively controlled SPWM method. The resultant currents and voltages were examined, revealing that the MI is dependable and performs well. To reduce undesirable harmonic, an LPF filter is built in the MI output. The suggested inverter has a low harmonic distortion, which results in great power quality and a compact frequency response. In comparison to traditional MI, the proposed inverter employs just 8 switching device and 3 DC sources. To examine the results of the designed MI simulations are run by using Matlab/Simulink program. The improved output waveform and decreased THD are highlighted, demonstrating the suggested PUC-MI efficiency. Without utilizing any harmonics filters, the output voltage's THD is 10%. It's 0.05 percent after filtration. For the applicability of distributing generated systems, in [9] author proposed a novel single-phase DC-AC MI based on cascaded transformers MLI (CTMLI). 19-level voltage output synthesizing are used to validate the suggested CTMLI procedure. The suggested inverter reduces THD to 5.607 percent up to 500 kHz without the use of a filter, and to 3.08 percent with the use of a filter. The suggested work uses a 7 level, 19, 37 level output with 8, 12, and 16 number of switches. Utilizing 9, 13 and 17-level MLI topologies, in [10], author offered a redesigned MLI architecture. A HRES is constructed that is coupled to a redesigned Cascaded Half-Bridge Multi Level Inverter (CHB-MLI), with switching driven by an ANN model. The suggested hybrid renewable energy method includes ten Metal (MOSFETs) with 17 levels. With a minimal components and lower THD, the suggested architecture works well. The suggested system's CHB-MLI performance is evaluated by creating a methodology in the MATLAB/SIMULINK environment To demonstrate the efficacy of the suggested model, the simulated performance of suggested CHB-MLI for the renewable energy application are evaluated and the results of current models were discussed. For 17 level MLI has ten MOSFET switching devices, the THD rate is reduced to 3.58 percent. In [11] author proposed design has a lower number of Dc voltage sources, switches, component count level factor, lower TSV, greater effective, lower THD, and is less expensive than existing Proposed topology. The 9 and17-level MLIs are also investigated with various cascaded load. The suggested inverter is robust under non-linear loading condition and is well suited for grid-connected FACTS and sustainable energy uses. THD is 8.49 percent for 9 level with 7 switches and 4.12 percent for 17 level with 12 switches, respectively. The 9th and 7th levels are 95 and 92 percent efficient, respectively. In [12] author designed and tested a grid-connected solar energy conversion system based on a binary hybrid MLI. Ten semiconductor switches and three binary weighted isolated DC-sources make up the 15-level BHMLI. At dynamic load and PV changes, balanced, sinusoidal, and in-phase grid currents are obtained. As a result, SECS operation maintains grid power quality within IEEE-519 guidelines. 1.35 percent is the computed THD. In [13] proposed a microprocessor-based digital output. Besides, Pseudo Random Multi-Carrier (PRMC) involves two random PWM strategies to minimize the harmonic order for 9- a level cascaded multilevel H-bridge (CHB) inverter and a 9-level Modular Multilevel inverter are introduced. In [14] author proposes a three-phase hybrid cascaded modular Multi - level inverter architecture based on a modified H-bridge modules is suggested in this study. In comparison to traditional CHB and flying capacitance (FC), the FC has fewer switches, lower capacitor requirements, and lower VBC. When compared to a three phase 9-level cascaded H-bridge Inverter, it lowers switch count by 50%, gate drive demand by 43.75 percent, and energy source requirement by 58.33 percent. In [15] author presented in this study an asymmetrical cascaded H-bridge MLI for solar systems. Under the level shifted modulation approach, the output voltage vs. time plot displays a THD of 3.84 percent spectrum. In [16] author proposed 11-level multilevel inverter prototype. To achieve Nstep for the load, the proposed architecture requires minimal switches and gate driver circuits with low standing voltage on switching devices. In [17], the response time of the PI and FLC controllers for a Photovoltaic seven level MLI a three-phase induction generator was investigated in this research. Two distinct controllers are used to assess the motor's efficiency. The FLC outperforms the PI controller in terms of rising time, error, THD as well as output waveform quality. As a result, the FLC with seven multi-level inverters generates a better output than the traditional PI controller. The THD is 17.04 percent with a frequency of 19.29 Hz as a result. In [18], a novel multilevel inverter architecture for a three-phase grid-connected solar (PV) system is proposed in this research. In comparison to typical symmetric multilevel inverters, the suggested symmetric multilevel inverter creates seven levels with fewer power switches. The suggested architecture is simulated, and the modification of capacitor voltages, inverter output voltage, and grid injected current are provided in order to evaluate the proposed seven-level multilevel inverter's performance. The proposal has a Harmonic distortion of 3.28 percent, according to the results. In [19] author created a novel cascaded asymmetric MLI for solar electricity production with fewer switching circuitry. There are three main sources plus 11 switching device in the circuit. The cascaded structure's voltage THD is 0.34 percent, while the current THD is 0.13 percent, both of which are within IEEE519 harmonic standards. In [20] author proposed an advanced MLI circuit with the primary goal of reducing the number of electrical components. The suggested circuit's functioning and sequence of operations are explained and demonstrated. To create the power circuits' controlling pulses innovative various carrier controlling technique is applied in the elements. THD was 1.89 percent and requires 16 switches.

FOREX Publication
Open Access | Rapid and quality publishing
International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 10, Issue 3 | Pages 501-507 | e-ISSN: 2347-470X

3. SYSTEM DESCRIPTION AND PRINCIPLE OF OPERATION

Figure 1 depicts the power circuit of the Multilevel inverters. Only N unidirectional switches, N diodes, with N/3 asymmetric dc supply are used by suggested approach. The essential DC sources are separated and can be provided by renewable energy sources like photovoltaics and fuel cells. The suggested MLI focuses on lowering MLI complexities with optimizing output voltage levels in order to enhance power quality. The amount of unidirectional switches (control a current in one direction only), bidirectional switches (services in both directions), or power amplifier like gate drivers, capacitors (2-terminal, electrical component), as well as DC sources all have a role in mitigating the MLI's complexities. By earlier analysis, the no. of the symmetric level for given MLI (Nlevel) can be written as this equation.

Figure 1 depicts the power circuit of the multilevel inverters. Only N unidirectional switches, N diodes, with N/3 asymmetric dc supply are used by suggested approach. The essential DC sources are separated and can be provided by renewable energy sources like photovoltaics and fuel cells. The suggested MLI focuses on lowering MLI complexities with optimizing output voltage levels in order to enhance power quality. The amount of unidirectional switches (control a current in one direction only), bidirectional switches (services in both directions), or power amplifier like gate drivers, capacitors (2-terminal, electrical component), as well as DC sources all have a role in mitigating the MLI's complexities. By earlier analysis, the no. of the symmetric level for given MLI (Nl_{evel}) can be written as this equation.

$$N_{level}=2\left(\frac{Vdc1+Vdc2+Vdc3+Vdc4}{Vdc1}\right)+1 \qquad (i)$$

This classification of MLI, a simplest approach is employed to generate pulses. As illustrated in Figure 5.10, such approach comprises of 4 phases: reference sine-wave signal, for compares two voltages or currents using comparators, logic circuits (electric circuit), and driving circuits to generate appropriate pulses for the switches.

The reference signal (RS) is split by same amount of levels as the output waveform's levels required. The peak value (V_p) and the number of levels requested (N) define the values of the voltage step (V_{step}) of the RS as follows:

$$V_{step} == \frac{2Vp}{N-1} \qquad (ii)$$

The voltage level (V_i) written as; considering positive half cycle:

$$V_i == (i -- 1) * V_{step} \qquad (iii)$$

Here, I = order of level and variation from 0 to (N+1)/2

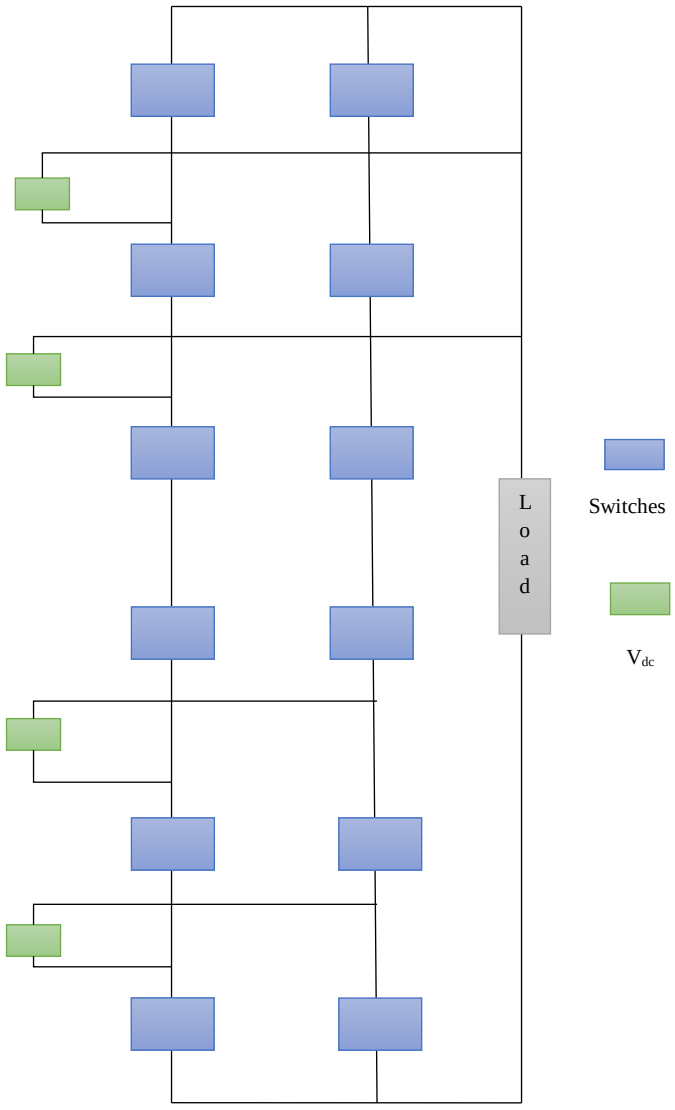

Figure 1: Multilevel Inverter's Power Circuit Diagram

To avoid DC coefficient of output waveform, for other negative half cycle having equal voltage level, difference is that it is of a negative value. Within that procedure, the switching angles are determined using a comparator. The switching instants are generated by comparison of the reference signal to critical levels. The critical value is where the reference sine wave transitions from one level on to another. It's set as the halfway point between the 2 levels to guarantee of output waveform, resulting in a wave having little numbers of harmonics. The comparator switch's critical values were evaluated as follows:

$$V_{cri} == \frac{V_i+V_{i+1}}{2} \qquad (iv)$$

Here, (i) == order of the level

FOREX Publication
Open Access | Rapid and quality publishing
International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 10, Issue 3 | Pages 501-507 | e-ISSN: 2347-470X

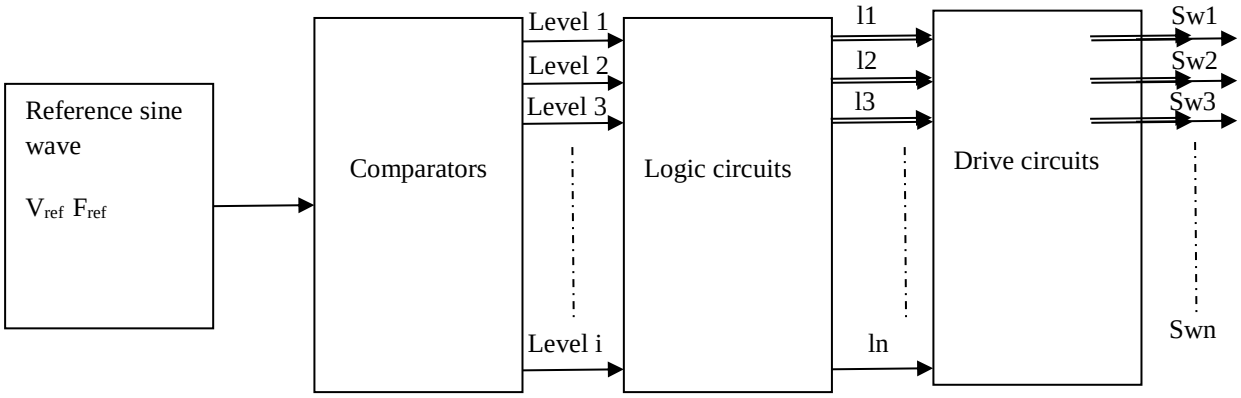

Figure 2: Switching pulse system phases

4. RESULT ANALYSIS

In this section, implementation details about results and discussion on this research work. In this section, performance evaluation parameters as well as result analysis is discussed. MATLAB was used as implementation platform for proposed architecture. *Table 1* shows the parameters description with their values including resistance, Inductance, Capacitance, DC voltage, Frequency, Load type and levels. *Table 2* represents the switching state of 7-level MLI presented in the paper.

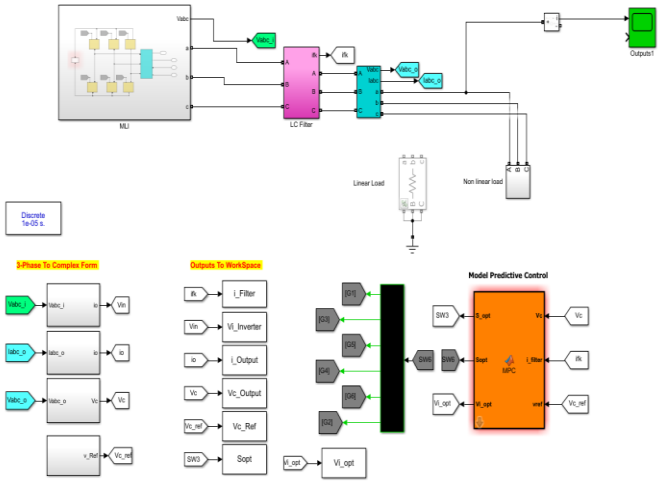

Figure 3: Simulation of Smart grid with predictive MLI

Table 1: Parameters Description

Input Parameters	Values
Resistance	1 ohm
Inductance	2e-3 H
Capacitance	1e-3 F
DC voltage	220 volt
Frequency	50Hz
Load Type	Resistance
Levels	7-41

Figure 4 and 5 show output variable with the switching variable to generate 7 level output and Output voltage generated for 7-level MLI. *Figure 6* shows the output voltage created for 11-level MLI with varying duration between 0-0.2 second and *Figure 6* shows output variable with switching variable to generate 11 level output. *Figure 8* shows output variable with the switching variable to generate 17 level output and *Figure 9* shows the Output voltage generated for 17-level MLI with varying time between 0-0.2 second. *Figure 10* shows output variable with the switching variable to generate 21 level output and *Figure 11* shows the Output voltage generated for 21-level MLI with varying time between 0-0.2 second. *Figure 12* shows output variable with the switching variable to generate 27 level output and *Figure 13* shows the Output voltage generated for 27-level MLI with varying time between 0-0.2 second. *Figure 14* shows output variable with the switching variable to generate 31 level output and *Figure 15* shows the Output voltage generated for 31-level MLI with varying time between 0-0.2 second. Figure 16 shows output variable with the switching variable to generate 37 level output and *Figure 17* shows the Output voltage generated for 37-level MLI with varying time between 0-0.2 second. *Figure 18* shows output variable with the switching variable to generate 41 level output and *Figure 19* shows the Output voltage generated for 41-level MLI with varying time between 0-0.2 second.

Table 2: Switching State of 7-level MLI

Voltage Level	S1	S2	S3	S4	S5	S6	S7
$+2V_{in}$	1	1	0	0	0	1	0
$+1.75V_{in}$	1	1	1	0	0	1	0
$+1V_{in}$	1	1	0	0	1	0	1
0	1	1	0	0	0	0	0
$-1V_{in}$	0	0	1	1	1	0	1
$-1.75V_{in}$	0	1	1	1	0	1	0
$-2V_{in}$	0	0	1	1	0	1	0

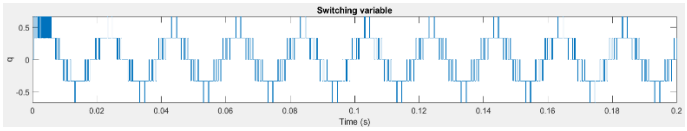

Figure 4: Switching Variable to generate 7 level output

FOREX Publication
Open Access | Rapid and quality publishing
International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 10, Issue 3 | Pages 501-507 | e-ISSN: 2347-470X

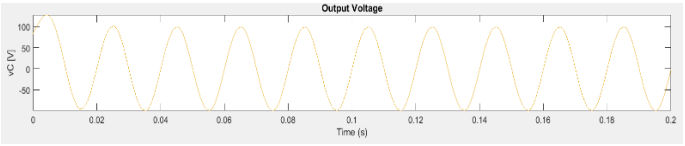

Figure 5: Output voltage generated for 7-level MLI

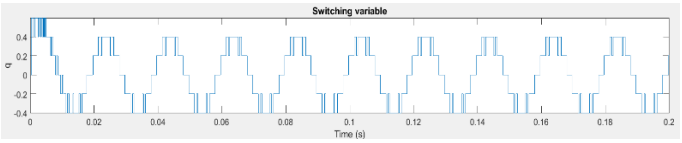

Figure 6: Switching Variable to generate 11 level output

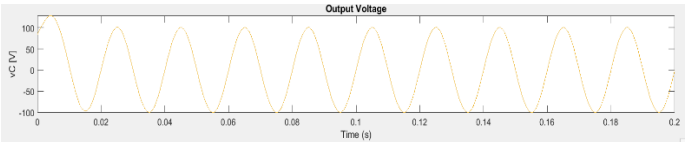

Figure 7: Output voltage generated for 11-level MLI

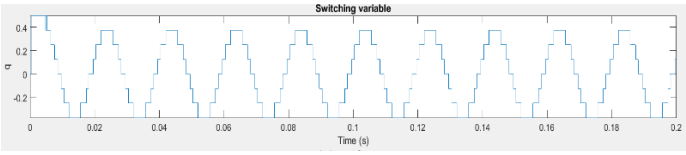

Figure 8: Switching Variable to generate 17 level output

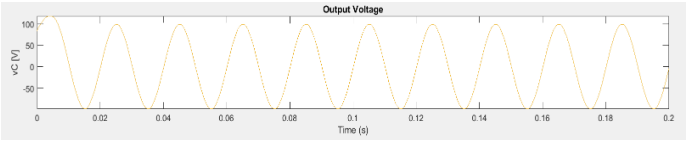

Figure 9: Output voltage generated for 17-level MLI

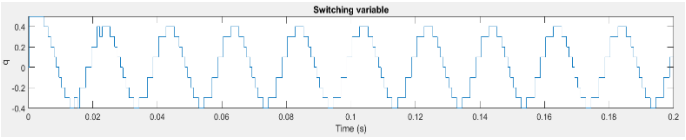

Figure 10: Switching Variable to generate 21 level output

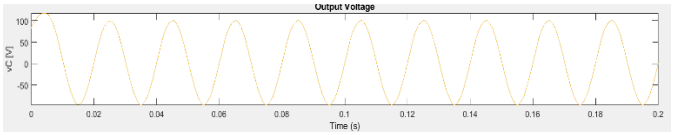

Figure 11: Output voltage generated for 21-level MLI

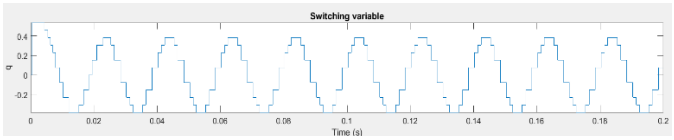

Figure 12: Switching Variable to generate 27 level output

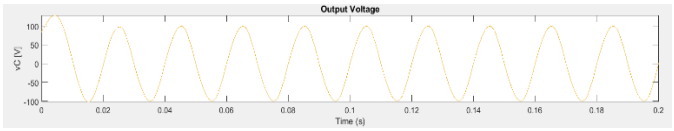

Figure 13: Output voltage generated for 27-level MLI

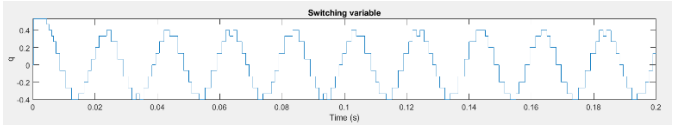

Figure 14: Switching Variable to generate 31 level output

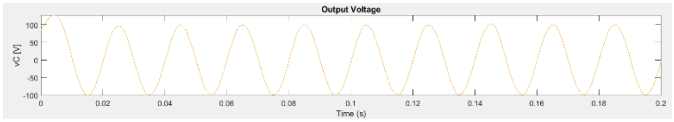

Figure 15: Output voltage generated for 31-level MLI

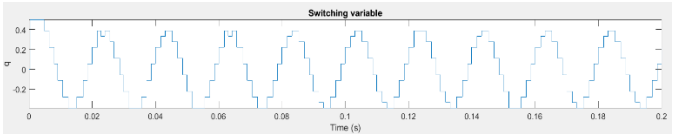

Figure 16: Switching Variable to generate 37 level output

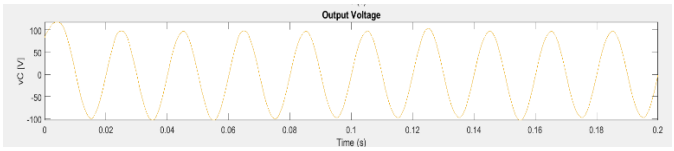

Figure 17: Output voltage generated for 37-level MLI

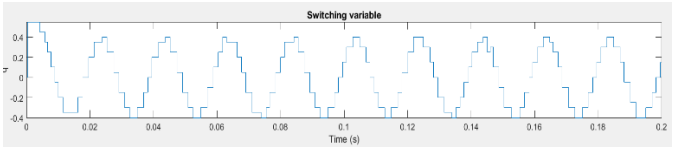

Figure 18: Switching Variable to generate 41 level output

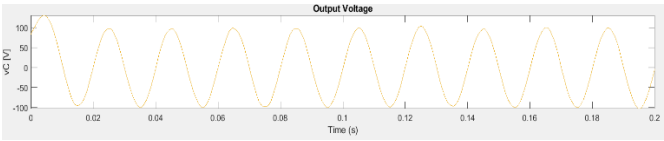

Figure 19: Output voltage generated for 41-level MLI

Table 3 shows THD analysis with the variable levels, THD in dB and percentage as well. Level 7 has THD -43.56 dB and 0.663 in %. Whereas Level 11 has slightly lower THD -44.33dB and 0.607 %. Level 17 has -46.2 THD in dB and 0.499 in %. Level 21 has -36.53 dB and 1.49 THD in percentage. Level 27 has highest THD around -33.14 dB and 2.20 percentage. Level 31 and 37 has almost same THD around -39.23 dB and -39.27 dB THD and 1.092% THD and 1.087 %. Level 41 has lowest THD -46.28 dB and 0.4850% THD. *Table 4* shows the voltage and current HD analysis with different levels varied from 11 to 41. Level 11 has THD voltage 0.6074 and 1.6969 current, which is highest in all the levels. Level 17 has lowest THD in terms of voltage and current i.e. 0.499 and 1.4612. Level 31 has minimum THD for both voltage and current around is 0.3519 for voltage and 1.0623 for current. Level 37 has THD 0.4469 and 1.4214 voltage and current respectively. Level 41 has 0.5576 and 1.5105 THD for voltage and current respectively. A state of art comparison is presented, *Table 5*. Andrade and Manjunatha [1] proposed a 31-level MLI and achieved 2.83% of THD. Rupesh and Vishwanath [4] proposed a fuzzy logic MLI with 1.58% of THD. Arikesh and Parvathy [21], presented a

FOREX Publication
Open Access | Rapid and quality publishing
International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 10, Issue 3 | Pages 501-507 | e-ISSN: 2347-470X

modular MLI that gives 1.89% of voltage THD. Whereas Mamatha et al. [8] presented cascaded transformer based MLI and achieved 3.58% of THD respectively. As compared to these MLI techniques, this paper presented the predictive MLI with increased level that reduced the voltage THD up to 0.55%.

Table 3: THD Analysis with variable levels

MLI levels	THD (in dB)	THD (in %)
Level 7	-43.56	0.663
Level 11	-44.33	0.607
Level 17	-46.2	0.499
Level 21	-36.53	1.49
Level 27	-33.14	2.20
Level 31	-39.23	1.092
Level 37	-39.27	1.087
Level 41	-46.28	0.4850

Table 4: Voltage and Current THD Analysis

MLI levels	THD (voltage)	THD (current)
Level 11	0.6074	1.6969
Level 17	0.4999	1.4612
Level 31	0.3519	1.0623
Level 37	0.4469	1.4421
Level 41	0.5576	1.5105

Table 5: Comparative State-of-art

Ref	THD (in %)
[1]	2.83
[4]	1.58
[8]	3.58
[21]	1.89
Ours	0.55

5. CONCLUSION

In this paper, a multi-level inverter with increased levels are designed and implemented for renewable energy smart grid applications. The MLI family's main benefit is that it solves the issue of total harmonic distortion, EMI, and dv/dt switch stress. Even more products based on multi-level inverter topologies are becoming available in the industrial or commercial markets. Still layout complexity as well as control circuits are the subjects of ongoing research. The major concern was observed with most of the multi-level inverters are that with increased level total harmonic distortion (THD) is increased if switching control is not designed properly. Therefore, in this paper predictive control is implemented on renewable energy based smart grid inverters to increase level with minimum voltage THD and current THD. The paper analyzed voltage and current THD in the different levels of multilevel inverter. From result analysis it was observed that minimum THD was observed with level 31, i.e. 0.35% and at level 41 it was increased up to 0.55% which is still not high as compared to other existing MLI architectures. In future, the work will be proceeded on controlling efficiency improvement with integration with filters such as LC filter and LCL filters.

REFERENCES

[1] S. Andrade and Y. R. Manjunatha, "A 31-level inverter with optimal number of switches for power applications," 2016 IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT), 2016, pp. 221-225, doi: 10.1109/RTEICT.2016.7807816.

[2] Kaustubh P. Draxe, Mahajan SagarBhaskarRanjana "A cascaded asymmetric multilevel inverter with minimum number of switches for solar applications" 2014 POWER AND ENERGY SYSTEMS: TOWARDS SUSTAINABLE ENERGY.

[3] Kurundkar, Kalyani, and G. A. Vaidya. "Application of HFPSO-TOPSIS approach for optimally locating and sizing of reactive power compensating devices for voltage control ancillary service." IJEER 9(3), 16-26, 2021.

[4] Femy P. H., Jayakumar J., "A Review on the Feasibility of Deployment of Renewable Energy Sources for Electric Vehicles under Smart Grid Environment", IJEER 9(3), 57-65, 2021. DOI: 10.37391/IJEER.0903061.

[5] M Rupesh, Dr. T S Vishwanath, "Fuzzy and ANFIS Controllers to Improve the Power Quality of Grid Connected PV System with Cascaded Multilevel Inverter", IJEER 9(4), 89-96, 2021. DOI: 10.37391/IJEER.090401.

[6] J. Ebrahimi, E. Babaei and G. B. Gharehpetian, "A New Multilevel Converter Topology With Reduced Number of Power Electronic Components," in IEEE Transactions on Industrial Electronics, vol. 59, no. 2, pp. 655-667, Feb. 2012, doi: 10.1109/TIE.2011.2151813.

[7] Y. Liao and C. Lai, "Newly-constructed single-phase multistring multilevel inverter for fuel-cell microgrid," 8th International Conference on Power Electronics - ECCE Asia, 2011, pp. 1440-1444, doi: 10.1109/ICPE.2011.5944453.

[8] Sandhu, Mamatha; Thakur, Tilak (2020). Modified Cascaded H-bridge Multilevel Inverter for Hybrid Renewable Energy Applications. IETE Journal of Research, (2020), 1–13. doi:10.1080/03772063.2020.1784802

[9] C. Dhanamjayulu, D. Prasad, S. Padmanaban, P. K. Maroti, J. B. Holm-Nielsen and F. Blaabjerg, "Design and Implementation of Seventeen Level Inverter With Reduced Components," in IEEE Access, vol. 9, pp. 16746-16760, 2021, doi: 10.1109/ACCESS.2021.3054001.

[10] C. M. Nirmal Mukundan, P. Jayaprakash, U. Subramaniam and D. J. Almakhles, "Binary Hybrid Multilevel Inverter-Based Grid Integrated Solar Energy Conversion System With Damped SOGI Control," in IEEE Access, vol. 8, pp. 37214-37228, 2020, doi: 10.1109/ACCESS.2020.2974773.

[11] C. Bharatiraja, S. Jeevananthan and J. L. Munda, "A Timing Correction Algorithm-Based Extended SVM for Three-Level Neutral-Point-Clamped MLI in Over Modulation Zone," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 6, no. 1, pp. 233-245, March 2018, doi: 10.1109/JESTPE.2017.2723518.

[12] Muhammad Humayun, Muhammad Mansoor Khan, Ali Muhammad, Jianming Xu, Weidong Zhang," Evaluation of symmetric flying capacitor multilevel inverter for grid-connected application", International Journal of Electrical Power & Energy Systems, Volume 115, 2020, 105430, ISSN 0142-0615, https://doi.org/10.1016/j.ijepes.2019.105430.

[13] T. Kaliannan, J. R. Albert, D. M. Begam, and P. Madhumathi, "Power Quality Improvement in Modular Multilevel Inverter Using for Different Multicarrier PWM," Eur. J. Electr. Eng. Comput. Sci., vol. 5, no. 2, pp. 19–27, 2021, doi: 10.24018/ejece.2021.5.2.315.

[14] R. R. Karasani, V. B. Borghate, P. M. Meshram, H. M. Suryawanshi and S. Sabyasachi, "A Three-Phase Hybrid Cascaded Modular Multilevel Inverter for Renewable Energy Environment," in IEEE Transactions on Power Electronics, vol. 32, no. 2, pp. 1070-1087, Feb. 2017, doi: 10.1109/TPEL.2016.2542519.

[15] S. Kumar and Y. Pal, "A Three-Phase Asymmetric Multilevel Inverter for Standalone PV Systems," 2019 6th International Conference on Signal Processing and Integrated Networks (SPIN), 2019, pp. 357-361, doi: 10.1109/SPIN.2019.8711605.

International Journal of
Electrical and Electronics Research (IJEER)
Research Article | Volume 10, Issue 3 | Pages 501-507 | e-ISSN: 2347-470X

[16] Babaei, E., & Hosseini, S. H. (2009). New cascaded multilevel inverter topology with minimum number of switches. Energy Conversion and Management, 50(11), 2761–2767. https://doi.org/10.1016/j.enconman.2009.06.032

[17] S. Chandrasekaran, S. Durairaj, S. Padmavathi, A Performance evaluation of a fuzzy logic controller-based Photovoltaic-fed multi-level inverter for a three-phase induction motor, Journal of the Franklin Institute, Volume 358, Issue 15, 2021, Pages 7394-7412, ISSN 0016-0032, https://doi.org/10.1016/j.jfranklin.2021.07.032.

[18] H. K. Jahan and M. Abapour, "Switched-Capacitor-Based Multilevel Inverter for Grid-Connected Photovoltaic Application," in IEEE Transactions on Power Electronics, vol. 36, no. 9, pp. 10317-10329, Sept. 2021, doi: 10.1109/TPEL.2020.3035598.

[19] Ahmed, Taiea A.; Mohamed, Essam E.M.; Youssef, Abdel-Raheem; Ibrahim, A.A.; Saeed, Mahmoud S.R.; Ali, Ahmed I.M. (2020). Three phase modular multilevel inverter-based multi-terminal asymmetrical DC inputs for renewable energy applications. Engineering Science and Technology, an International Journal, (), S2215098619310663–. doi:10.1016/j.jestch.2019.11.003

[20] S. Fouda, M. S. Salem, A. Saeed, A. Shaker and M. Abouelatta, "Thirteen-Level Modified Packed U-Cell Multilevel Inverter for Renewable-Energy Applications," 2020 2nd International Conference on Smart Power & Internet Energy Systems (SPIES), 2020, pp. 431-435, doi: 10.1109/SPIES48661.2020.9243059.

[21] A., A., & Parvathy, A. K. (2020). Modular multilevel inverter for renewable energy applications. International Journal of Electrical and Computer Engineering (IJECE), 10(1), 1–14. https://doi.org/10.11591/IJECE.V10I1.PP1-14.

[22] M Rupesh, Dr. T S Vishwanath (2021), Fuzzy and ANFIS Controllers to Improve the Power Quality of Grid Connected PV System with Cascaded Multilevel Inverter. IJEER 9(4), 89-96. DOI: 10.37391/IJEER.090401.

[23] Femy P. H., Jayakumar J. (2021), A Review on the Feasibility of Deployment of Renewable Energy Sources for Electric Vehicles under Smart Grid Environment. IJEER 9(3), 57-65. DOI: 10.37391/IJEER.0903061.

[24] Himabindu Eluri, M. Gopichand Naik (2022), Energy Management System and Enhancement of Power Quality with Grid Integrated Micro-Grid using Fuzzy Logic Controller. IJEER 10(2), 256-263. DOI: 10.37391/IJEER.100234.