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International Journal of
Electrical and Electronics Research (IJEER)
Research Article | Volume 10, Issue 3 | Pages 508-517 | e-ISSN: 2347-470X

Performance Analysis of Renewable Integrated UPQC

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ABSTRACT- The enhancement in electric power quality using a single-stage solar PV integrated Unified Power Quality Conditioner (UPQC) has been discussed in this paper. The UPQC is the combination of Distributed static compensator (DSTATCOM) and Dynamic Voltage Restorer (DVR) having the common DC voltage supply link. The DSTATCOM compensates for the load current associated problems like load power factor improvement, even and odd current harmonics elimination etc. Also, it performs the additional work of transferring power from the solar PV system to the load of the distribution system. The DVR compensates the voltage-associated power quality problems like source voltage sag, source voltage swell, and voltage distortion. Discussed UPQC with distributed generation system works on modified synchronously rotating reference frame theory. With the help of the discussed system, the two outcomes are achieved such as clean and renewable energy generation and power quality enhancement. The system is designed in MATLAB Simulink environment and then system performance is verified on Real-Time Digital Simulator (OPAL-RT OP4510) in Software in Loop Simulation (SIL) and Hardware in Loop Simulation (HIL) platforms.

Keywords: UPQC, SRF, PV-UPQC, DSTATCOM, OPAL-RT, DVR, DG, MPPT, PV

ARTICLE INFORMATION
Author(s); Sachin B. Shahapure, Vandana A. Kulkarni (Deodhar) and Ramchandra P. Hasabe;
Received: 19/05/2022; **Accepted**: 20/07/2022; **Published**: 25/08/2022;
E- ISSN: 2347-470X;
Paper Id: IJEER220519;
Citation: 10.37391/IJEER.100318
Webpage-link:
https://ijeer.forexjournal.co.in/archive/volume-10/ijeer-100318.html

Publisher's Note: FOREX Publication stays neutral with regard to jurisdictional claims in Published maps and institutional affiliations.

1. INTRODUCTION

India is a country that is located near the equator, and the geographical location stands in favor of solar PV installation in India as it gets nearly 3000 hours of sunshine every year which is equivalent to 5000 trillion kWh of energy. The major factors that should be considered for installing the solar power plant in a particular region are sunlight, the total cost of the project, solar PV panels with PV material availability, and the interest of the consumer. In India central government as well as several state governments are trying their best to increase solar PV installations. The government of India had set up the goal of reaching 100 GW by the end of the year 2022. In recent years researchers have carried out a study and stated that the energy generated using solar systems can become as cheap as energy generated from thermal power stations in the next decade. The technological development in battery energy storage systems is allowing more usage of solar energy in various sectors including commercial, residential etc. [1-2]. The superiorities of solar energy are geographical advantage for distributed generation, employment prospects clean and green energy [3-7]. Ultra mega solar power projects, power generation in NTPC/ NVVN, ministry of defense, and paramilitary with viability gap funding (VGF) are necessary, and MNRE implementing the projects under the national solar mission [8-14]. As solar PV systems are expanding in India the power quality concerns related to voltage and currents are also increasing. Use of solar energy is also affecting the stability of the national grid [22]. The solar PV system can be combined with the power quality improvement devices [15-18]. The voltage quality using DVR and current quality using DSTATCOM is enhanced combined using unified power quality conditioner (UPQC) shown in *figure 1*.

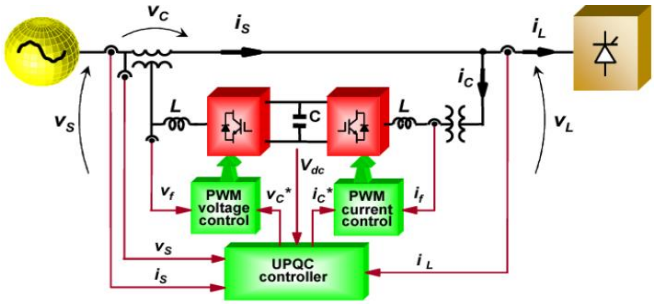

Figure 1: Conventional UPQC system

The UPQC with the help of synchronously rotating reference frame theory based control presented in this paper. For implementing the system, the OPAL-RT real-time simulator is used. The advantages of this system are an integration of power quality enhancement device UPQC with a clean energy generation solar PV system. Discussed system is stable under various dynamic conditions such as voltage sag/swell and load unbalanced condition with simultaneous source voltage and load current quality improvement. The performance of the proposed system is analyzed extensively under both dynamic and steady-state conditions using Matlab-Simulink software and OPAL-RT software.

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2. UPQC SYSTEM

Usually, nonlinearities in the system cause the harmonics. There are many sources of nonlinearity that can arise in circuits in real-world conditions. Integration of renewable energy such as solar PV systems with power quality improvement devices is the current trend in power systems.

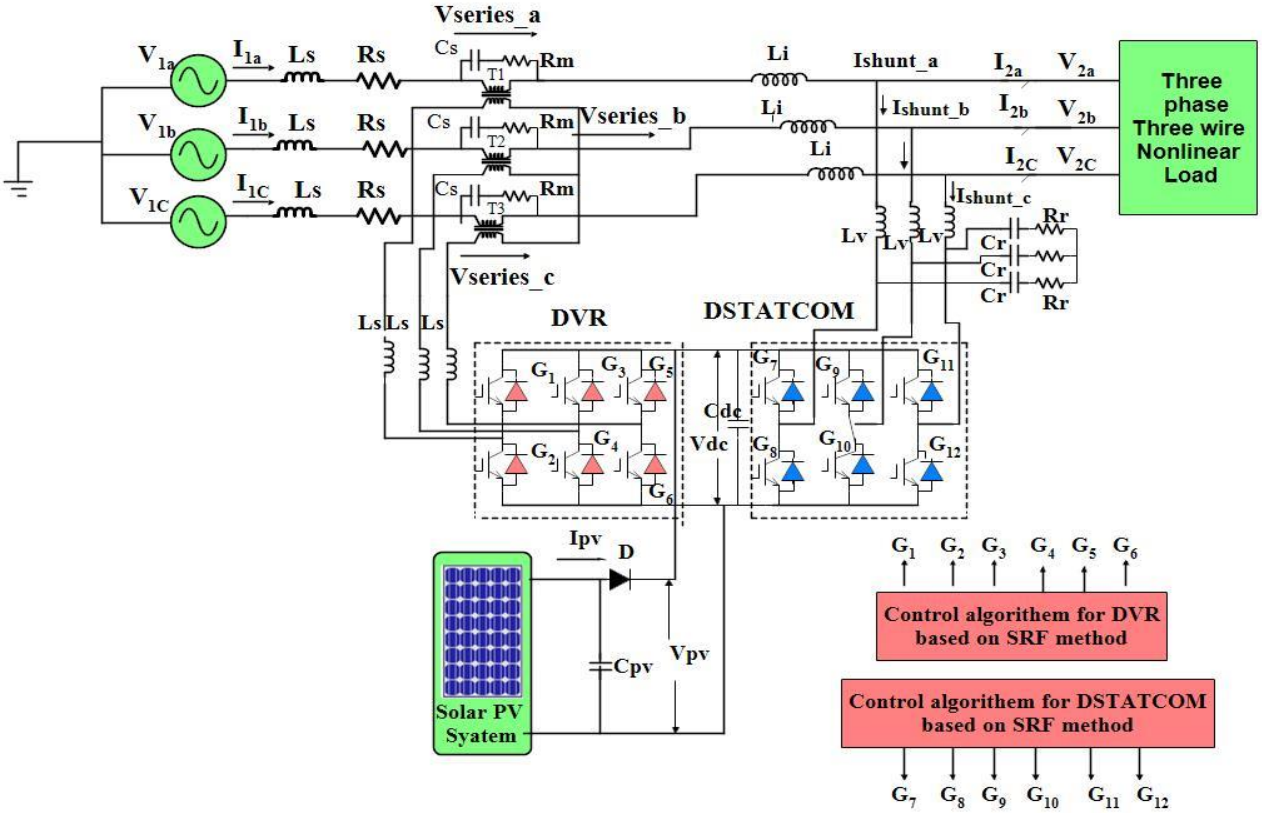

Figure 2: PV- UPQC system

2.1 PV-UPQC System

The UPQC is the merger of DVR and DSTATCOM. The UPQC is having several configurations and classifications based on their supply, connections such as right shunt left shunt and their working principle. In UPQC the DVR compensates the voltage-related power quality problems such as voltage harmonics, and voltage sag/swell/ unbalance. The DSTATCOM compensates for all the current related power quality problems such as current harmonics, power factor correction, etc. There are various combinations for UPQC such as UPQC-P, UPQC-S, and UPQC-Q as consideration of power supplied and left shunt UPQC, right shunt UPQC after consideration of system design. In the research, the right shunt UPQC is considered for analysis purposes and the development of the new control algorithm. The PV-UPQC consists of the two voltage-sourced pulse width modulated inverters having a combined dc link. The input power for that DC link comes from the solar PV system. The transformer is placed in series with the line in the left part of the UPQC system called DVR. The PWM inverter is connected in shunt with the right part of the UPQC system which is called DSTATCOM [7]. The three-phase three-wire nonlinear load is connected to the system. Because of the high switching frequency operation, the ripples are generated and to minimize these ripples the RC filter is connected to the circuit. Figure 2 shows the PV-UPQC System [20-22].

2.2 PV-UPQC Design

PV-UPQC system design consists of the design of DSTATCOM and DVR with its ripple filters, design of the DC link ratings, series-connected transformer, and selection of switching device with switching frequency, design and of solar PV system for appropriate operation of UPQC. The system of PVUPQC (DSTATCOM and DVR) depends upon power and voltage ratings required to compensate for the full load condition. The power rating of UPQC is always matched with the proportional power rating of Load.

2.1.1 DC-Link Design

The capacitor is connected to the DC link for keeping the DC link voltage stable and constant. The two PWM inverters are getting power from the solar PV system through a connected DC link for the satisfactory operation of the PV-UPQC system. The formula for DC link voltage is given in equation 1.

$$V_{dc} = \frac{2V_{LL}\sqrt{2}}{m\sqrt{3}} \quad \ldots\ldots (1)$$

Where m is the modulation index, V_{LL} is line voltage.
From the principle of energy conservation, the formula for the capacitor is shown in *equation 2*. From this formula, the magnitude of the capacitor for the capacitor connected to the DC link of the UPQC can be calculated.

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$$C_{dc} = \frac{3KaI_{sh}V_{ph}t}{0.5(V^2_{dc} - V^2_{dc1})} \quad \ldots\ldots (2)$$

Where, V_{dc} is dc link voltage, V_{dcl} is the least voltage which is slightly lower than DC link voltage, a is the overburden factor constant, I_{sh} is the phase current of the shunt compensation system, C_{dc} is DC link Capacitance, and V_{ph} is the phase voltage of the system, t is the minimum time needed for fulfilling steady state value after a disturbance, k factor considers variation in energy during dynamics.

2.1.2 Series Injection Transformer

The voltage, current and power rating of series injection transformer is dependent on overall capacity of PV-UPQC. It mainly depends on the power rating and voltage rating of DVR. The turn ratio for the transformer is given in equations 3 and 4.

$$V_{DVR} = X * V_S \quad \ldots (3)$$

Where V_{DVR} is the DVR injecting voltage into system and X is the reactance offered by the system.

$$K_{DVR} = \frac{V_{VSC}}{V_{DVR}} \quad \ldots (4)$$

Where V_{VSC} is the voltage across voltage source converter. The current through series VSI of DVR is the same as the grid current. The used parameters and values are given in Appendix A.

2.1.3 Interfacing Inductors for PV-UPQC

The theoretical equations for the calculation of the interfacing inductance required from inductors with ratings for the DVR and DSTATCOM differently of the discussed system are given in *equations 5 and 6*.

$$L_{rdstat} = \frac{mV_{dc}\sqrt{3}}{12af_{sh}I_{cr,pp}} \quad \ldots\ldots (5)$$

$$L_{rdvr} = \frac{mV_{dc}K_{SE}\sqrt{3}}{12af_{SE}I_r} \quad \ldots\ldots (6)$$

Where m = Modulation Index, F_{sh}= Switching Frequency, $I_{cr,pp}$ = Peak-Peak current, a = Constant

2.1.4 Design of Ripple Filter

As the switching operation of the switches (whether IGBT or MOSFET switches) of DVR and DSTATCOM should be very fast to get the better dynamic response as well as better performance and fast operation of the overall system as it is necessary. For this, the switching frequency should be high in terms of kilohertz. And in the proposed system the switching frequency is selected as 10 kHz.

Selecting the very high switching frequency has some disadvantages as well such as ripples in voltage and currents are injecting into the system and electromagnetic interference will be increased. Hence it is necessary to use a ripple filter in the system. The ripple filter Ratings for DSTATCOM and DVR are given in *Appendix A*.

3. CONTROL ALGORITHM FOR UPQC BASED ON SRF METHOD

The control methods are mainly classified as time-domain methods and frequency domain methods. The time-domain methods such as instantaneous active reactive theory, synchronous rotating reference frame theory, and artificial neural network (ANN). The time-domain control methods are very fast operational characteristics but are not as precise and accurate as frequency-domain methods hence used in devices those control power in the system such as DSTATCOM, STATCOM, DVR, UPQC, etc. The frequency-domain methods are highly precise and accurate hence these frequency-domain methods are used in power quality monitoring devices where operating time is not important. The disadvantages of PQ theory are given as follows. The PQ method uses a large number of voltage and current transducers and is poor in compensation if the source current is not sinusoidal. Also this method is most sensitive to harmonics and imbalance in supply voltage. The advantages of DQ theory are given as follows. The DQ method is easily implementable and robust and it is most suitable for harmonic compensation with sinusoidal source voltage. Also, this method is accurate as compared with PQ theory.

3.1 Control Algorithm for DVR

In this presented PV-UPQC, a series-connected compensator which is called the dynamic voltage restorer (DVR) injects voltage in the same phase with respect to utility grid voltage, which emerges in the required series injection or supply voltage by the DVR. The fundamental component of the point of common coupling sensed voltage is separated using a phase lock loop and then generates the reference axis in the DQO domain for the control operation based on the SRF method. The utilized load voltage reference is extracted using the phase angle and voltage and current frequency information of PCC voltage acquired using the phase lock loop. The point of common coupling voltages and voltages across the connected load is converted into the DQO domain using Clarke and parke transform which are given in *equations 7 and 8.* The DVR is connected in series at the distribution end in the right shunt UPQC hence the voltage or power can be injected into the system using DVR. The source-side voltage and load-side voltage is sensed using voltage sensors (LM sensors). The modified SRF control method is used for the conversion of that voltage and current signals from one reference frame to another reference frame. As the reference load voltage is to be in phase with the PCC voltage, the d-axis component value is set by the required reference value and as there is no requirement for reactive power hence the q-axis component is kept at zero. Clarke transform for voltage is as follows The difference between the connected load reference voltage and the point of common coupling voltage indicates the reference voltage for the DVR and that voltage is necessary to compensate hence this voltage is passed through the PI controller and again converted into ABC domain using inverse Clarke and inverse park transform and given to PWM voltage controller to initiate required PWM signals for DVR inverter.

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$$\begin{bmatrix} V0 \\ V\alpha \\ V\beta \end{bmatrix} = \sqrt{2}/\sqrt{3} \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ \frac{1}{\sqrt{2}} & -\frac{1}{2} & -\frac{1}{\sqrt{2}} \\ 1 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} Va \\ Vb \\ Vc \end{bmatrix} \quad \ldots\ldots. (7)$$

-Inverse Clarke transform for voltage

$$\begin{bmatrix} Va \\ Vb \\ Vc \end{bmatrix} = \sqrt{2}/\sqrt{3} \begin{bmatrix} \frac{1}{\sqrt{2}} & 1 & 0 \\ \frac{1}{\sqrt{2}} & -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V0 \\ V\alpha \\ V\beta \end{bmatrix} \quad \ldots\ldots. (8)$$

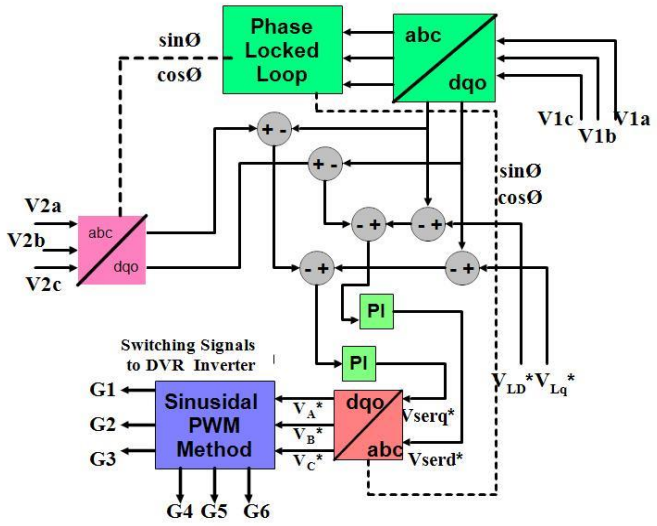

Figure 3: Control method for DVR

The PV-UPQC system is working on active Power only and also compensates for active power therefore reference value for the d-axis component is set at the peak value of the load voltage and q-axis reference component is set at zero because PV–UPQC does not compensate reactive power in the system. Figure 3 shows the block diagram of the control method used for DVR based on the SRF algorithm. The actual signal and the reference signal are passed through the proportional and Integral (PI) controller and then switching signals are generated by using the sinusoidal pulse width modulation (SPWM) method.

3.2 Control Algorithm for DSTATCOM

The DSTATCOM is connected in a shunt at the distribution end. The source side of PV-UPQC is DSTATCOM and hence DSTATCOM side currents and load side currents are sensed using current sensors. The modified SRF control method is used for the conversion of that signals into various reference frames such as ABC and DQO reference frames.

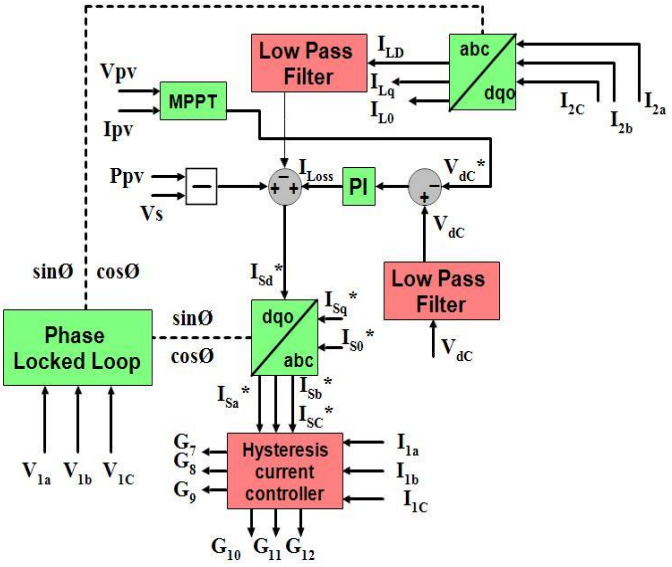

Figure 4: Control method for DSTATCOM

To perform the load current compensation using distributed static compensator (DSTATCOM) the active component of load current is required and is extracted using the synchronously rotating reference frame method. These load currents are converted from the ABC domain to the DQO domain using PLL (phase and frequency) and parks transformation. The DSTATCOM compensated the current related power quality problems such as harmonics, power factor improvement, etc. Figure 4 shows the block diagram of the control method used for DSTATCOM based on the SRF algorithm [19]. The DC power fed to the DC link of both the inverters is from the PV system. After giving the reference values of I sd*and I sq* (I so*=0 because UPQC-P operation is considered) which are given in equations 9, 10, 11 and comparing with the actual converted values using the SRF method the signal is passed through space vector pulse width modulation (SPWM) and generated switching signals which are given to the DSTATCOM PWM inverter.

$$I^*_{sq} = 0 \quad \ldots (9)$$

$$I^*_{so} = 0 \quad \ldots (10)$$

$$I^*_{sd} = I_{L\,df} + I_{L\,oss} - I_{Pvg} \quad \ldots (11)$$

4. SOLAR PV SYSTEM

The PV arrays are built up with combined series/parallel combinations of PV solar cells, which are usually represented by a simplified equivalent circuit model such as the one given in *figure 5* and by an *equation 12* The PV cell output voltage is a function of the photocurrent that is mainly determined by load current depending on the solar irradiation level during the operation.

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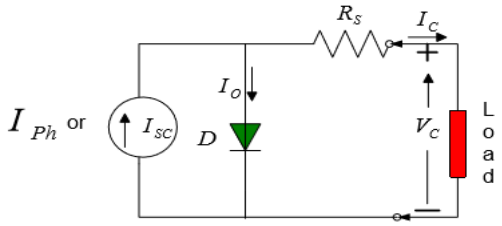

Figure 5: Blok diagram of single diode model of solar cell

$$V_C = \frac{AKT_C}{e} \ln\left(\frac{I_{ph} + I_O - I_M}{I_O}\right) - R_S I_M \quad \text{.....(12)}$$

Where the symbols are defined as follows:

e: electron charge (1.602×10^{-19} C).

k: Boltzmann constant (1.38×10^{-23}J/°K).

I_C: cell output current, A.

I_{ph}: photocurrent, function of irradiation level and junction temperature (5 A).

I_0: reverse saturation current of diode (0.0002 A).

R_S: Series resistance of cell (0.001 Ω).

T_C: reference cell operating temperature (20 °C).

V_C: cell output voltage, V.

$$C_{TV} = 1 + \beta_T (T_a - T_x) \quad \text{... (13)}$$

$$C_{TI} = 1 + \frac{\gamma_T}{S_C} (T_x - T_a) \quad \text{.....(14)}$$

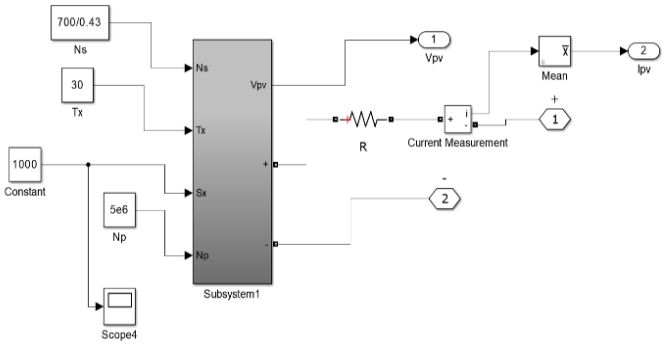

Figure 6: The mathematical model for PV system in Matlab

Where, $\beta_T = 0.004$ and $\gamma_T = 0.06$ for the cell used and $T_a = 20$ °C is the ambient temperature. If Sx level increases from S_{x1} to S_{x2}, the cell Tx and Iph will increase from T_{x1} to T_{x2}. These effects are elaborated in the model by the solar irradiation coefficients C_{SV} and C_{SI} which are given in the following equation

$$C_{SV} = 1 + \beta_T \alpha_S (S_X - S_C) \quad \text{... (15)}$$

$$C_{SI} = 1 + \frac{1}{S_C} (S_X - S_C) \quad \text{... (16)}$$

The constant α_s represents the slope of the change in the cell operating temperature due to a change in Sx and is equal to 0.2. Using correction factors in voltage and currents based on temperature and irradiation such as C_{TV}, C_{TI}, C_{SV} and C_{SI} and the new values of the V_{CX} and I_{phx} are obtained for the new T_x and S_x are given in below equations

$$V_{CX} = V_{TV} C_{SV} V_C \quad \text{... (17)}$$

$$I_{Phx} = C_{TI} C_{SI} I_{Ph}.. \quad \text{… (18)}$$

The mathematical modeling of the solar PV system using the above solar cell voltage equation using MATLAB Simulink is given in *figure 6*.

5. MATLAB RESULTS FOR PV-UPQC SYSTEM

The steady-state and dynamic performance of solar integrated UPQC are determined with the help of simulation using Matlab software. The external load is used in the system as a three-phase diode bridge rectifier (DBR) with R-L connected load. The solver used for Matlab simulation is Tustin/Backward Euler with step size used is 1e-5s. The result analysis of PV UPQC is verified at the various abnormal and dynamic conditions in the power systems. At the load end, the conditions are voltage sag, swell and three-phase load unbalance. The simulation results for the above-mentioned conditions are shown below. The detailed PV-UPQC system Matlab simulation parameters consisting DVR, DSTATCOM and Solar PV system are given in *appendix A*.

5.1 Source Voltage Sag and Swell Condition

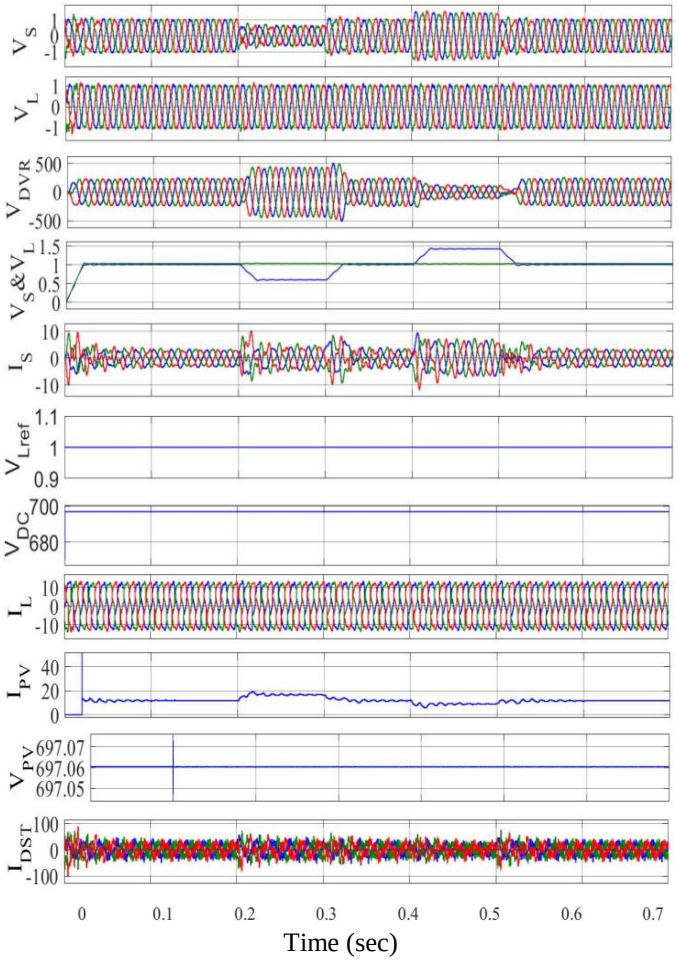

Figure 7: PV-UPQC during source voltage sag/swell condition

The AC source voltage Vs sag condition and Vs swell condition are the two abnormal conditions that are generally observed in power systems. The stable system can work properly even under these abnormal conditions. The performance of PV-UPQC is also demonstrated under these conditions and it is observed that the discussed system works properly with appropriate results which are shown in the below figures. *Figure 7* consists of the simulation results

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diagram which shows the waveforms of source voltage, load voltage, DVR injected voltage, source current, DC link voltage, load current, PV system voltage, PV system current, and DSTATCOM current. The sag and swell are carried out in source voltage with the help of programmable voltage block and then verified the operational performance of PV-UPQC and PV-UPQC operated correctly. The sag in Vs of 0. 4 per unit (Pu) and swell in Vs of 0.4 Pu are exaamined in the AC three-phase three-wire source voltage variations for the operation. It is observed that voltage across the load remains constant under sag and swell conditions.

5.2 Three Phase Load Unbalanced Condition

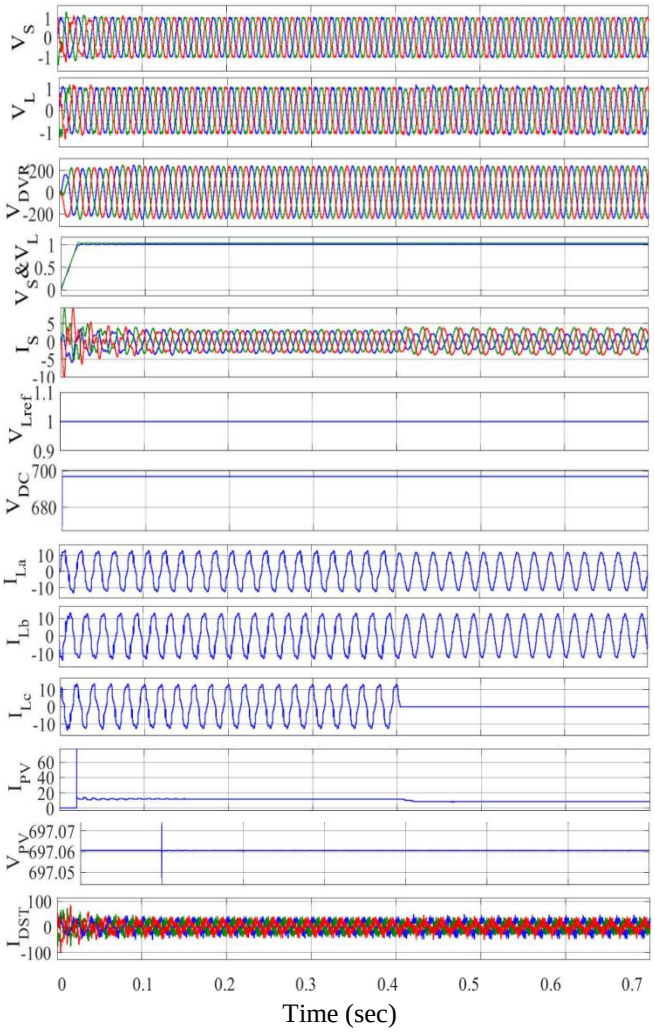

Figure 8: PV-UPQC during load unbalance condition

Along with load unbalancing different power quality problem is also faced such as source voltage sag and swell, harmonics in source voltage, and voltage notching. *Figure 7* shows the simulation results diagram of PV-UPQC which consist again the currents and voltages same as sag and swell condition. For creating the load unbalance condition in a three-phase supply while the simulation is running the phase C among the three phases of the load is turned off at a particular instant of time which is shown in *figure 8* After the load unbalancing the control operation of the PV-UPQC is verified and it is observed that the system is working properly in this condition as well and there are no effects on the load. The Vs sag and Vs swell condition and three Phase load unbalance situation is verified with the help of Matlab simulation software.

6. HARDWARE IMPLEMENTATION OF PV-UPQC SYSTEM

Setup for solar integrated UPQC with result analysis with the waveforms, switching signals waveforms of the system using power quality analyzer is discussed in following paragraphs.

6.1 Real-Time Software in Loop Simulation of PV-UPQC

This research consists of the real-time digital simulator OP4510 based on evaluating and examining the performance of discussed PV-UPQC. There are chances of the utilization of real-time digital simulators considering the various fields such as industry, academic, research, and many more because of the advantages it offers. These advantages are reduction or lower cost required for hardware implementation for a particular system, increased test functionalities are possible on that system, as well as reduced human inference hence personal risks. The various specifications of the real-time digital simulator are as given in *Table 1*. The hardware setup of OP4510 is shown in *figure 9* and *figure 10* shows the Matlab model compatible with OPAL-RT which consists of two separate files named as SM-Master (Matlab model) along with SC-Console (all measurements blocks) which runs on 20 Micro second step time.

Table 1: Parameters specification of OP-4510

S.No	OP4510 Device parameter	Specification
1	No of cores	4 Core
2	Operating Frequency	3.5 GHz
3	Analog in	16 Channels
4	Analog out	16 Channels
5	Digital in	32 Channels
6	Digital out	32 Channels
7	FPGA Version	Kintex 7
8	RAM and SSD	16 and 128 GB
9	Communication protocol between host computer and target computer	RS 232 and TCP IP 4

The software in loop (SIL) and hardware in loop (HIL) operations are executed for the PV-UPQC Matlab model on OPAL-RT. For the communication of two subsystems, the OPCOMM block is used. The analog signals in HIL simulation are taken out from OP4510 by using the OP CONTROL block and OP ANALOG OUT block. The OPAL-RT output signal waveforms are shown in *figure 11* show the source voltage and source current without UPQC on DSO. *figure 12* shows the source voltage and source current with UPQC on digital oscilloscope *figure 13* shows the THD analysis of source voltage and source current without UPQC which is for source voltage it is 24.58% and for source current it is 27 %. *Figure 14* shows the THD analysis of V_s and I_s with UPQC and it comes for V_s is 0.06 % and for I_s it is 5.05 %.

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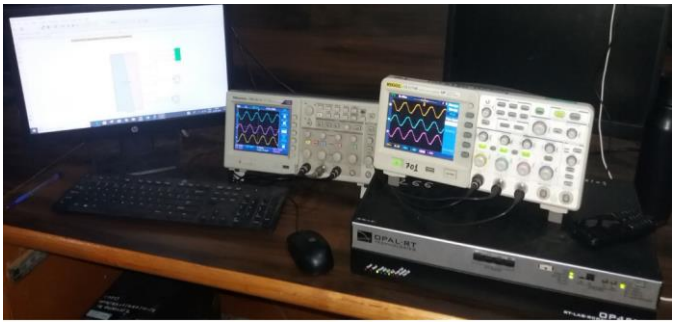

Figure 9: SIL Setup for PV-UPQC based on OP4510

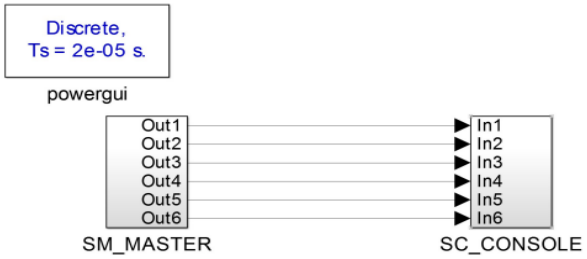

Figure 10: PV-UPQC Matlab software model on OP4510

Table 2: Integration of UPQC with DG

	Superiority	Drawback
UPQC With DG (Common DC Link)	1.Overall system costs will be reduced because of the Removed DG Inverter 2.System operation in Islanding mode is possible 3.Active power transfer during grid interfacing is possible 4.Compensation of voltage interruption is achievable	1. Overall Capacity enhancement is multilevel inverter is complex and difficult 2. Control method implementation complexity is high
UPQC With DG (Separate DC Link)	1.Active power transfer during grid interfacing is possible 2. Control method implementation is simple 3.OverallCapacity enhancement is multilevel inverter is achievable	1. Compensation of voltage interruption may not be possible 2. System operation in Islanding mode is may not possible 3. System cost is high

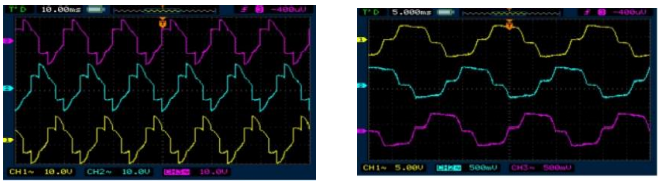

Figure 11: V_s and I_s without UPQC on DSO

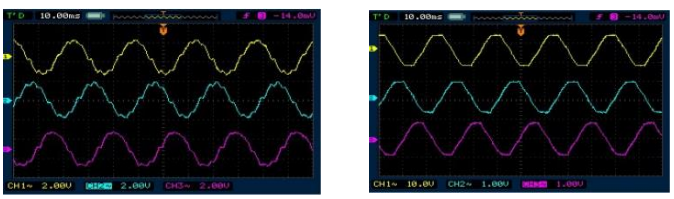

Figure 12: V_s and I_s with UPQC on DSO

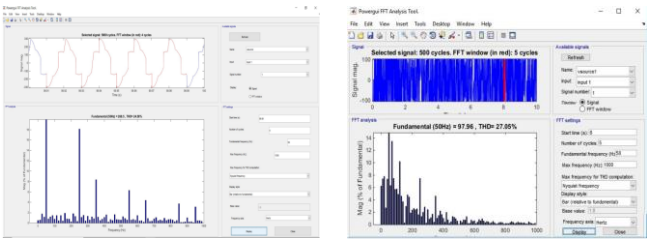

Figure 13: Vs and Is without UPQC THD analysis

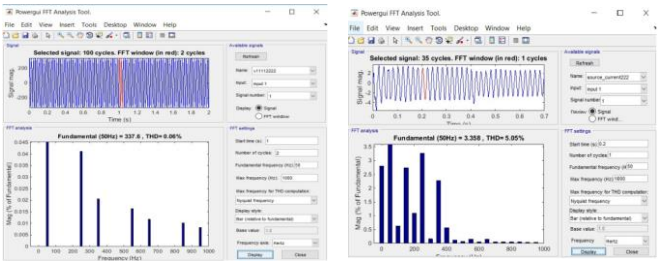

Figure 14: Vs and Is with UPQC THD analysis

6.2 Hardware Setup for PV-UPQC

The simulation results of any model in any software give the performance which is nearer to the hardware circuit not exact the hardware results. That's why hardware implementation is an important part while developing any system. For the hardware implementation of the system, the devices are used such as SEMIKRON inverter, OPAL-RT, power analyzer (Yokogawa), and host PC. The inverter is of the three-phase three-wire voltage sourced pulse width modulated inverter and OPAL-RT is used for switching signal generation for the operation of DVR and DSTATCOM.

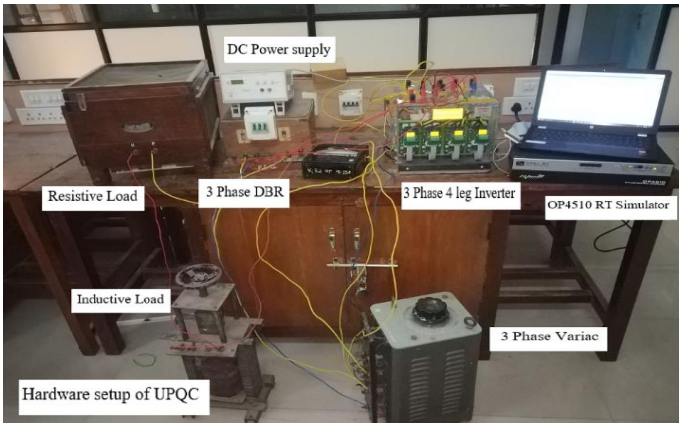

Figure 15: Hardware setup for PV-UPQC system

Figure 16: Three Phase Power Analyzer (Yokogawa)

In the hardware setup, OPAL-RT (OP4510) is used for switching signal generation. This device is based on KINTEX

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7 FPGA processor having 32 DI and 32 DO, 16 AI, 16 AO channels. It consists of the target computer which has ratings of 16 GB Random Access Memory (RAM) and 128 GB Solid State Drive (SSD). The working capability of the UPQC system is mainly depending on various ratings of the components of that system. While developing the hardware of the system the power handling capability as well as the power dissipation capability are important factors to be considered. *Figure 15 and figure 16* show the hardware diagram for the system with its components. In earlier days the thyristor is used as the switching device in converter and inverter circuits. Because of the disadvantages of the thyristor as a switching device, the main focus is on other self-commutating devices like IGBT and MOSFETS. The IGBT is used as the switching device in this system.

6.3 Hardware Results for PV-UPQC

The power quality analyzer is used for the analysis of the voltage quality and power quality and current quality. The various results for hardware circuits are switching signals for the DVR circuits, and switching signals for the DSTATCOM circuit.

6.3.1 Switching signals for DSTATCOM

Currently, the FPGA processors are most widely used for device control purposes. The switches used in DSTATCOM inverter circuit switch G_7, G_8, G_9, G_{10}, G_{11}, and G_{12}. The switchesG_7 and G_8 are shown in *Figure 17 (a)*. The switch G7, switch G_8 and switch G_9, switch G_{10} are in the same leg of the DSTATCOM inverter. The switches G_9 and G_{10} are shown in *Figure 17 (b)*. The switch G_{11} and switch G_{12} are in the same leg of the inverter which is shown in *Figure 17 (c)*. The voltage source inverter is used for the operation of the DSTATCOM device. The switching pulse waveforms which are given to the PWM inverter are taken out from OPAL-RT and stored with the help of a digital oscilloscope.

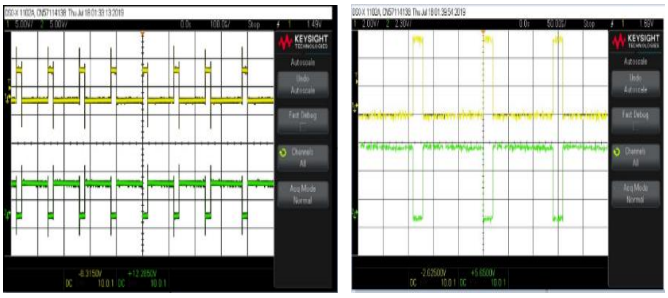


Figure 17: (a) Switching signals for G_7, G_8 **(b)** Switching signals for G_9, G_{10}

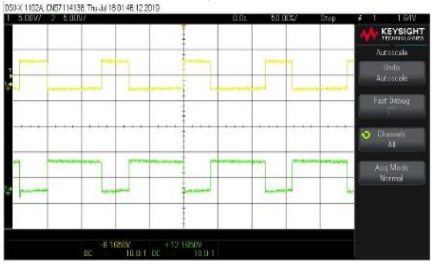


Figure 17 (c) Switching signals for G_{11}, G_{12}

The switching frequency for the operation of the DSTATCOM and DVR is 10 kHz. The switching device OPAL-RT OP 4510 is used in the proposed system and consists of the latest FPGA processor which is based on programmable logic blocks (PLD).

6.3.2 Switching signals for DVR

The waveforms for magnitudes of the switches G1 and G2 (Leg 1) are shown in *figure 18 (a)*. The magnitude waveforms for the switches G3 and G4 (Leg 2) are shown in *figure 18 (b)*. The magnitude waveforms for the switches G5 and G6 (Leg 3) are shown in *figure 18 (c)*. The switching pulses for the same legs of the inverter are always magnitude inverted and the delay in two signals is provided to avoid the shoot through a fault in the inverter.

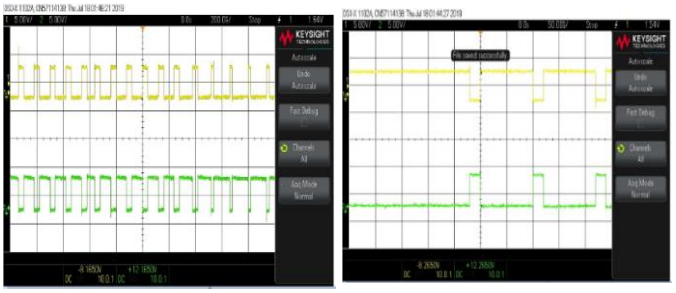


Figure 18: (a) Switching signals for G_1, G_2 **(b)** Switching signals for G_3, G_4

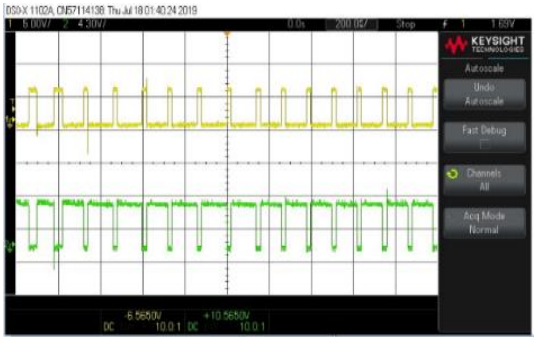
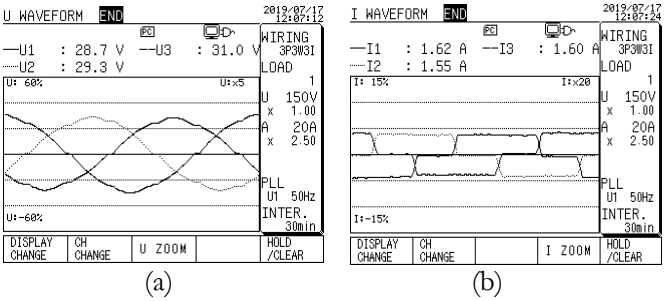


Figure 18 (c): Switching signals for G_5, G_6

6.3.3 Hardware Results for Test System without UPQC

The hardware results for the test systems are shown in *Figures 19 (a) and (b)*. The waveforms without UPQC for the source voltage and source current are taken with the help of a three-phase power quality analyzer which is shown in *figure 16*.



(a) (b)

Figure 19: Source voltage and source current without UPQC

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The three-phase source line voltages in the test system are 28.7 volts, 31 volts, and 29.3volt. The source current per phase for the test system is 1.63 amp. The proposed system is three phases three-wire that why the neutral current is absent. The source voltage waveforms for the test system are given in *figure 19 (a)* The source current waveform for the test system is given in *figure 19 (b).*

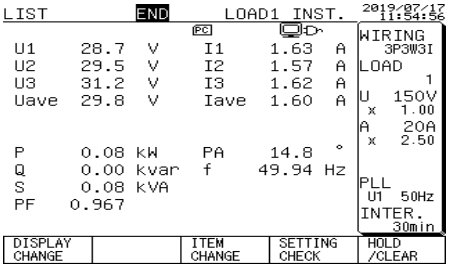
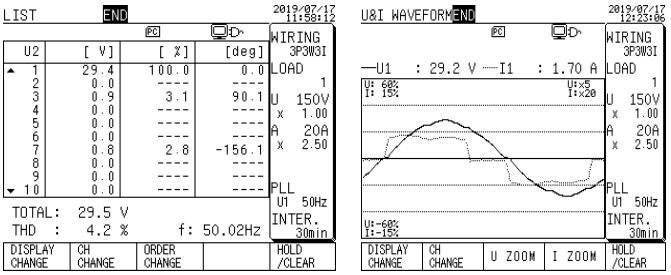


Figure 20: Source voltage and source current magnitudes

The source voltage magnitude and source current magnitude is given in *figure 20*. The total power consumed for the operation of the test system required is 80 watts and the power factor for the operation is 0.967. The KVA rating for the test system is 80VA with a frequency of 50Hz.



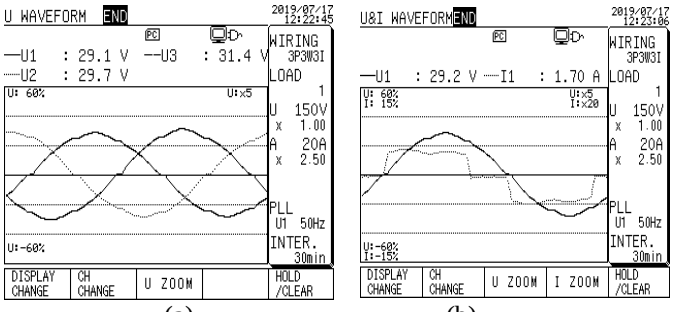
(a) (b)

Figure 21: Source voltage and source current Harmonics

The power dissipated in the test system comes as 80watt. The power factor for the test system is 0.96. The average current in the test system comes as 1.60 amp. The total harmonic distortion of the source voltage waveform THD for the test system is 4.1% and for the source, current THD comes as 23.7%.

The dominant harmonic component in the system is fifth harmonics and which is odd harmonic. The THD analysis of the source voltage for the test system is given in *figure 21 (a)* and the THD analysis of the source current for the test system comes as 23.7 % on power quality analyzer.

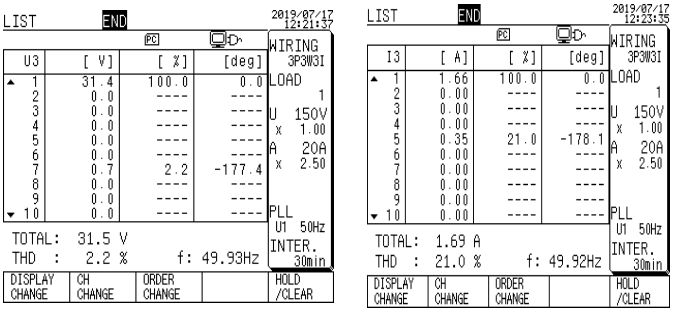
6.3.4 Hardware Results for Test System with UPQC



(a) (b)

Figure 22: Source voltage (a) and current (a) waveforms

The three-phase source line voltages in the test system are given in *figure 22 (a)* which are 28.7 volts, 31 volts, and 29.3volt. The source current per phase for the test system is given in Figure 22 (b) which is 1.63 amp. Figure 23 (a) shows the THD analysis for the source voltage after UPQC operation and Figure 23 (b) shows the THD analysis of the source current which 21.0 % is after UPQC operation



(a) (b)

Figure 23: Source Voltage THD (a) source current THD (b)

7. CONCLUSION AND FUTURE WORK

In this paper, the enhancement in power quality in the three-phase three-wire system using a single-stage solar PV system integrated UPQC is discussed with MATLAB simulation and hardware implementation. The DVR and DSTATCOM combined are considered with the solar PV system. The OPAL-RT (OP4510) is used for the switching signal generation as it consists of the KINTEX 7 FPGA processor. For the validation of the control algorithm the various abnormal conditions such as source voltage sag, swell and load current unbalance conditions are considered in simulation as well as in hardware im plementation. The results are verified after considering the IEC 61000 standards. Instead of a solar PV system, integration of UPQC with a wind energy system can also be possible. Both the solar and wind energy integration with UPQC is also achievable.

8. ACKNOWLEDGMENTS

As an author, thanks to AICTE for starting a scholarship program called the ADF (AICTE Doctoral Fellowship). This program helps improve the research environment in the country. I am also grateful to the research center GEC Aurangabad and WCE Sangli for their valuable support.

APPENDIX A*: *Simulation Parameters

DSTATCOM interfacing inductor: 4 mH; DVR interfacing inductor: 2 mH; DC-link Capacitor: 10 mF; DC-link Voltage: 700 V; PI gains for DC link: K_P= 1.5, K_I = 0.1; Ripple Filter: 25μF, 0.2Ω; Switching frequency of UPQC Inverters: 10 kHz; $V_{PCC\text{-}line}$:415 V, Supply Frequency=50 Hz; Load: Three phase bridge rectifier rating of 1kW; PV array parameters:Voc = 750 V, Isc = 13.5 A; Number of series cells = 700, Number of parallel cells=$5e^6$, Vmpp=697 V; Impp=11.84A; Ppv= 8.1 kW.

APPENDIX B: Experimental Parameters

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Research Article | Volume 10, Issue 3 | Pages 508-517 | e-ISSN: 2347-470X

Real-Time Simulator OPAL-RT (OP-4510)-FPGA (kintex-7) processor Target computer=16 GB RAM and 128 GB ROM, Host computer- Windows operating system with 8 GB RAM and one TB ROM and Intel I5 core processor. Three-phase autotransformer (Source side) - Primary voltage 230 volt and Secondary Voltage 100 volts to 400 volts. Three-phase power quality analyzer (Yokogawa). Three-phase diode bridge rectifier (Load Side) – Input voltage 230volt ac, output voltage 560 volts dc. R-L series load -400 volts, 30amp (12 kW). Three-phase diode bridge rectifier (Source side connected with Semikron Inverter) having output dc voltage of 400 volts, Three Phase Semikron Inverter- 3 KVA, 415 volt output 30 Amp max current, IGBT Ratings (Inverter) -100-amp and 1 kV, Series compensator interfacing inductor: 3.8 mH; Shunt compensator interfacing inductor: 1.5 mH; C_{DC}: 20 mF; $V_{DC\text{-}link}$: 200 V; Ripple Filter: 20μF, 10Ω; Switching frequency for UPQC Inverters: 10 kHz; $V_{PCC\text{-}line}$: 415 V, 50 Hz; Solar PV system parameters Voc = 45.8 V, Isc = 9.5 A; Vmpp = 36.7 V; Impp = 9.13 A; Ppv= 2 kW (330W_p*6 No)**.**

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