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Low-Power VLSI Implementation of Novel Hybrid Adaptive Variable-Rate and Recursive Systematic Convolutional Encoder for Resource Constrained Wireless Communication Systems

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ABSTRACT- In the modern wireless communication system, digital technology has tremendous growth, and all the communication channels are slowly moving towards digital form. Wireless communication has to provide the reliable and efficient transfer of information between transmitter and receiver over a wireless channel. The channel coding technique is the best practical approach to delivering reliable communication for the end-users. Many conventional encoder and decoder units are used as error detection and correction codes in the digital communication system to overcome the multiple transient errors. The proposed convolutional encoder consists of both Recursive Systematic Convolutional (RSC) Encoder and Adaptive Variable-Rate Convolutional (AVRC) encoder. Adaptive Variable-Rate Convolutional encoder improves the bit error rate performance and is more suitable for a power-constrained wireless system to transfer the data. Recursive Systematic Convolutional encoder also reduces the bit error rate and improves the throughput by employing the trellis termination strategy. Here, AVRC encoder ultimately acquires the channel state information and feeds the data into a fixed rate convolutional encoder and rate adaptor followed by a buffer device. A hybrid encoder combines the AVRC encoder and RSC encoder output serially and parallel, producing the solid encoded data for the modulator in the communication system. A modified turbo code is also obtained by placing interleaver between the two encoder units and building the stronger code word for the system. Finally, the conventional encoder system is compared and analyzed with the proposed method regarding the number of LUT's, gates, clock cycle, slices, area, power, bit error rate, and throughput.

Keywords: Recursive Systematic Convolutional encoder; Adaptive Systematic Convolutional encoder; Throughput; Bit Error Rate; Turbo code; Interleaver; Trellis termination strategy.

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1. INTRODUCTION

In today's wireless communication system, Error Correction Code plays a crucial role to provide the reliable data transfer between the transmitter and receiver section. Error Correction Code consists of both encoder unit and decoder unit where encoder unit generates the redundancy bit and produce the digital information to transmit over wireless channel. At the receiver side, received redundancy bit is compared with the newly generated redundancy bit, if any matches found, indicate the presence of error in the received bit. .Error Correction Code method is available as channel coding technique for Additive White Gaussian Noise based wireless channel. Convolutional code is the suitable channel coding method to facilitate the better error correction and detection code compared with block coding method. Convolutional code is applied to a continuous data stream, instead of applying to block of data as happened in block code. Convolutional encoder is used in many wireless communication system such as CDMA, GSM to encode the information prior to transmission indicates added redundancy bits to it, which is then used at the receiver section to recover the original information sequence effectively by reducing the possibilities of error due to open wireless noisy channel. Similarly, at the receiver side, Viterbi decoding method uses maximum likelihood decoding is used to reconstruct the original information from the encoded data bit. In this paper, proposed hybrid convolutional encoder consists of both adaptive Variable-Rate and Recursive Systematic Convolutional Encoder unit. It provides better bit error rate performance and high throughput due to its serial and parallel connection of encoder unit. It also use the maximum likelihood method in Viterbi decoding unit to regenerate or reconstruct the original bit information from the received bit. The following are the main objective aim of this research work

- To design and implement the hybrid adaptive convolutional encoder and decoder unit.
- To propose the novel modified turbo encoder by interleaved the block of data between the AVRC encoder and RSC encoder unit.

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- To make the modified RSC encoder unit by adding the trellis termination strategy in the encoding unit.
- To decode the original bit information by employing the Modified Maximum likelihood method in Viterbi Decoder unit.

The paper is organized as follows to meet the objectives of the research works mentioned above. Initially, introduce the importance of channel coding and its types in digital communication along with main contribution of the research work. *Section II* summarizes about recent related works processed toward the convolutional encoding techniques. *Section III* describes about the proposed hybrid convolutional encoder unit. *Section IV* shows the implemented results and discuss about the result towards the objective of the work. Finally, paper concludes the research work.

2. RELATED WORKS

X. Gao et al., [1] presented Neural Network based chinese text detection and verification methods by designing a model for encoder-decoder network that optimises the SSD model depending on scene text properties, allowing it to better adapt to natural scene text detection. The network predicts text areas in input images directly and obtains candidate text bounding boxes via a typical non-maximum suppression technique, obviating the need for numerous time-consuming intermediate steps. Second, an encoder-decoder network-based Text Verification Model is created. The model identifies texts in candidate bounding boxes found by the text localization neural network and excludes non-text areas that are incorrectly classified as text areas, boosting the precision of natural scene text identification even more. B. Sansoda and S. Choomchuay [2] elucidates how convolutional code (CC) is used in conjunction with a MIMO scheme to lower bit error probability in WBAN channels that use binary Phase Shift Keying (BPSK) for channel modulation. The results show that the combination method outperforms the conventional system, especially as the constraint length rises. The STBC system's diversity gain improves performance as distance rises. By raising the constraint length with recognized high complexity, the bit error rate can be improved. T. Le and Y. Duan [3] amalgamates skip-connections and a feedback loop into an encoder-decoder network, as well as a simple and effective Gaussian blurring based data augmentation, the deep learning algorithms used for edge detection will be improved. A synthetic data augmentation strategy that uses Gaussian blurring to push the network to learn more salient edges while also reducing overfitting. The system is fully trainable from start to finish and runs at 3.4 frames per second, which is a realistic speed. In comparison to state-of-the-art techniques, REDN performs exceptionally well on typical datasets like as BSDS500, NYUD, and Pascal Context. For establishing high confidence in artificial digital-noise-source based FPGA emulations, a converging criterion is suggested and shown by Y. Cai, [4]. The performance of the Concatenated Staircase and Hamming Code (CSHC) as a function of outer staircase code decoding iterations is explored, and emulation findings reveal that 6 staircase decoding iterations is the most common choice.

L. Liu and S. Liao demonstrate an optical encoder and decoder based on a PC L3 nano cavity in the lab [5]. The nonlinear effects could be amplified in a PC nanocavity with a limited mode volume. As a result, the equipment transmission properties might be fine-tuned while consuming little power. Luis-J et al., [6,7] evoked the integration of double error detection with multiple adjacent error correction, resulting in new Ultrafast SEC-xAEC-DED codes, is the main invention provided in this study. Different designs were implemented in VHDL hardware description language, and they were evaluated and compared using CMOS standard cell synthesis. Although ultrafast codes have been proposed as a feasible solution for register protection, it is noteworthy that their utility is not limited to this situation. Ultrafast codes allow fast encoding and decoding procedures with a moderate size and power overhead if the requisite redundancy is reasonable. For illustration, they can be used to secure high-speed memories or caches. To confirm the error coverage and assess the latency, area, and power overheads, ultrafast codes were developed and synthesized. SRAMs is used to emulate TCAMs on FPGAs have been recommended by P. Reviriego et al.,[8] as a way to protect them. The system is predicated on the fact that not all values can be stored in those SRAMs, implying that the memory contents have some inherent redundancy. When the memories are secured with a parity bit to detect faults, this redundancy is employed to repair most single-bit error patterns. The suggested technique drastically decreases the resources required to safeguard memory, making it a suitable option for systems where consistency is important but resources are constrained. This brief's concept can be applied to a variety of memory architectures. It can be used to identify defects on an unprotected memory by cleaning the contents to ensure that they are correct on a regular basis. It could also be used to fix multiple bit defects when the memory is protected with a more robust algorithm that can identify multiple bit faults. M. Karimzadeh-Farshbafan et al., [9] propounds a new programming problem for reliability-aware service placement that considers both the primary and backup servers at the same time. Researchers analyse a multi-infrastructure (multi-InP) provider scenario in which each InP provides the Network Operator (NO) with servers that are stable. Authors propose an optimization problem that takes into account both the primary and backup server assignments. The original optimization problem is reformulated as a mixed integer convex programming (MICP) problem, for which there are well-suited techniques. For solving the optimization problem, they suggest the Viterbi based reliable service placement (VRSP) algorithm, which is a sub-optimal solution. The decision measure in the suggested technique is based on the sum of the placement cost and a penalty term for failing to meet the specified reliability. M. V. Burnashev [10] suggested a time-invariant non-catastrophic convolutional encoder and the Viterbi decoder are used to transmit an endless binary information sequence over a stationary memoryless channel. The traditional proofs of the "union upper bound" for convolutional code decoding performance have significant mathematical flaws. These justifications presume that all information symbols must be decoded at some point, and that the decoded path on the trellis diagram must eventually "meet" the genuine path. These truths

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must be shown, even though they appear intuitive. The purpose of this note is to prove these facts for both a binary symmetric and a general stationary memoryless channel.

3. PROPOSED HYBRID ADAPTIVE SERIAL CONVOLUTION ENCODER FOR WIRELESS COMMUNICATION SYSTEM

In order to overcome the limitation mentioned in the related works, a novel hybrid adaptive variable-Rate and Recursive Systematic Convolutional Encoder method is proposed for resource constrained wireless system. The proposed system uses the benefits of both adaptive Variable Rate Convolutional Encoder as well as Recursive Systematic Convolutional Encoder. In order to understand the concept of Variable-Rate Convolutional encoder, a basic block diagram is shown in *figure 1* and it consist of fixed rate convolutional encoder, rate adaptor and buffer device. Since most of the wireless system are provided with time varying channel condition, a fixed-rate convolutional encoder is not suitable for this. So, in the proposed system, a Variable-Rate Convolutional encoder is used to provide the adaptive rate encoded data which is more suitable for dynamic channel condition by completely acquiring and utilizing the channel state information. The fixed-rate convolutional encoder produces the output from the two adders based on the input from the information source. FRC encoder output is fed as input to the rate adaptor, which generates the coded bits concerning the instantaneous rate of the channel. But, in real-time, it's impossible to modulate and transmit the generated encoded bit. So, the proposed encoder technique introduces the buffer device to store the encoded bit that comes from the rate adaptor device to ensure the transmission and modulation of the encoded bit at a fixed rate. Recursive Systematic Convolution Encoder is shown in *Figure 2*, and it is constructed by using two adders and D-Flip-flops to reduce the Bit Error Rate (BER). It is derived from the non-recursive systematic convolutional encoder by feedback the output of one flip-flop as input.

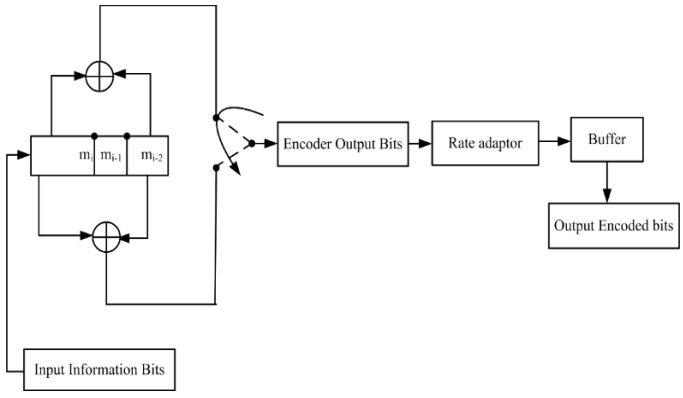

Figure 1: Block Diagram of Adaptive Variable Rate Convolutional Encoder (AVRC)

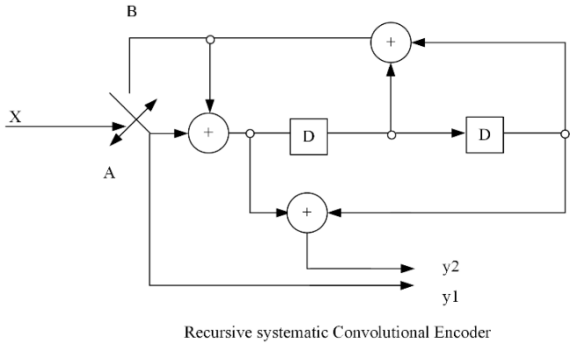

Figure 2: Recursive Systematic Convolution (RSC) Encoder

The proposed Hybrid Adaptive Convolutional Encoder is shown in *Figure 3* which consist of both Adaptive Variable Rate Convolutional (AVRC) encoder and Recursive Systematic Convolutional (RSC) Encoder. The output of AVRC Encoder is given as input to RSC encoded and encoded output is fed as input to modulator for modulation and transmission of encoded bits. At the receiver side, received signal is demodulated and give as input to the most famous maximum likelihood decoder method along with Viterbi decoder with trellis termination method. The RSC encoder is derived from the conventional variable convolutional encoder by setting the feedback of the first output represented by s1 to the input and it's represented by s1= [1 1 1].

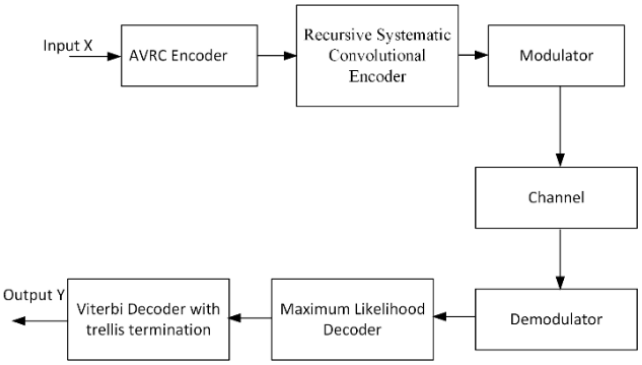

Figure 3: Block Diagram of Proposed Hybrid Adaptive Serial Convolutional Encoder

Figure 4 shows the enhanced hybrid turbo convolutional encoder by involving the interleaver with r = 1/3 between Variable Rate Convolutional encoder and Recursive Systematic Convolutional encoder to enhance the speed of the operation of the encoding techniques. The main purpose of interleaver is to provide the randomness of the input sequences and increases the weight of the code words. The enhanced hybrid turbo convolutional encoder produces high-weight code (y1) and low-weight code (y2), in addition to systematic code (y3). Here, interleaver is used to avoid the second RSC encoder to produce the low-weight recursive output sequence, instead it produce high-weighted code to improve the BER performance of the system. The interleaver block helps directly affects the distance properties of the code to improve the performance of turbo code. *Figure 5* gives the parallel connection of AVRC encoder and RSC encoder information along with Modulator, Maximum Likelihood Decoder and Viterbi Decoder with trellis

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termination. Parallel form of generation method of code word gives better code rate than the serial form of connection between the encoders mentioned in the *figure 3.* Interleaver is used between the encoders helps to improve the BER and randomness of the code, also turbo code uses the parallel connection of encoder circuits whereas turbo code uses the serial connection of decoder circuits.

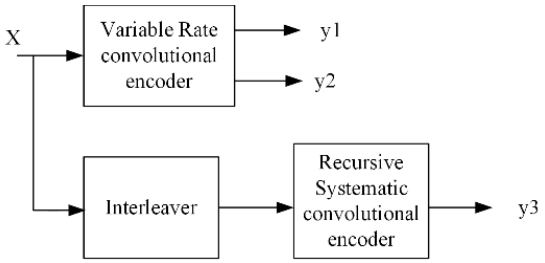

Figure 4: Enhanced Hybrid Turbo Convolutional Encoder

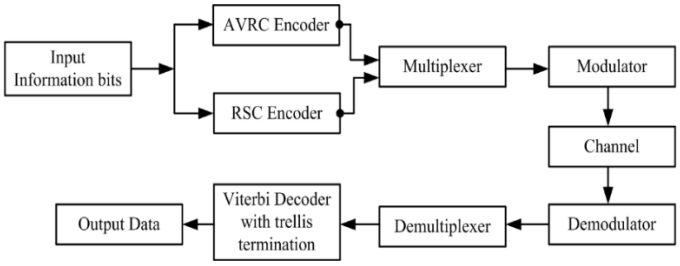

Figure 5: Communication Model using AVRC and RSC Encoder in parallel Connection

4. RESULTS AND DISCUSSION

The proposed hybrid adaptive variable convolution encoding techniques was implemented by using the Xilinx ISE 14.2 simulator operated by windows 11 operating system with Intel i5 8th generation processor and 6 GB RAM. Here, a hybrid adaptive variable convolutional encoder module is developed with the help of recursive Systematic Convolutional encoder for encoding the input data bits. The length of the input bit assigned for entire process of encoding and decoding is 4 bits. Then the viterbi decoder is connected serial manner to decode the encoded data bits even encoders are connected in serial or parallel way. Viterbi decoder helps to reconstruct the original input data bit which is transmitted from the transmitter side. Bit Error Rate (BER) and Signal to Noise Ratio (SNR) are the two parameters used to analysis the proposed hybrid AVRC and RSC encoder in both series and parallel connection. The bit error rate (BER) is the proportion of incorrect bits to all the bits received during a transmission. The signal-to-noise ratio is a scientific and engineering metric that contrasts the strength of a desired signal with the strength of background noise.

4.1 Performance Analysis

The proposed hybrid variable convolutional encoding technique was implemented and analyzed with the help of different FPGA devices such as Vertex 4, Vertex 5 and Vertex 7. The different simulation parameters such as number of LUT's, Number of Slices, Power, processing time, throughput, Bit Error Rate are analyzed to show and compare the performance of proposed encoder techniques with existing encoder techniques. *Figure 6* shows the comparison results of both fixed and variable convolution encoder for the input bit [0 1 0 1 1 1 0 0 1 0 1 0 0 0 1] and results shows that variable conventional encoder achieves better Bit Error Rate compared with fixed conventional encoder. Proposed encoder technique suitable and work for any input bit.

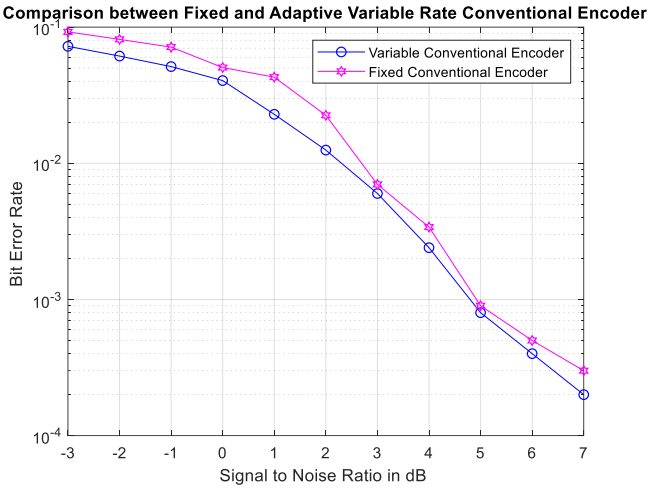

Figure 6: Comparison between Fixed and Adaptive Variable Rate

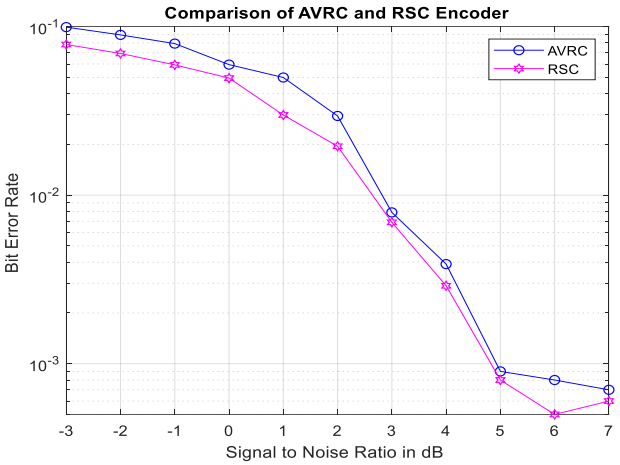

Figure 7: Comparison of both AVRC and RSC Encoder Conventional Encoder

Figure 7 shows the performance of Adaptive Variable Rate Conventional Encoder and Recursive Systematic Encoder techniques in terms of BER and SNR values and proves that RSC Encoder technique achieves good BER value compared with AVRC encoder techniques. However, still the proposed encoder techniques BER values is improved by connecting the AVRC and RSC encoder in series and parallel connection as show in *figure 8* and *figure 9* shows the importance of interleaver method in the proposed enhanced turbo convolutional encoder technique, by indicating the lesser BER values for the encoder with the presence of interleaver and however, it provides greater BER values for the system without interleaver. In order to analyze the proposed hybrid Adaptive Variable Rate Convolutional encoder technique in terms of power, area, clock cycle, number of gates and number of LUT's, it has been implemented in Xilinx software and results are

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discussed in the following figures. There are three FPGA devices such as Virtex 4, Virtex 5 and Spartan 6 are used to analyze the proposed recursive systematic and AVRC based hybrid encoder technique. *Table 1, 2 and 3* shows the comparison of different FPGA device with respect to area, delay and power for AVRC, RSC and Hybrid encoder techniques. The power consumed by FPGA Virtex 4 to perform the hybrid encoder techniques is very less compared to Virtex 5 and Spartan 6. Similarly, Virtex 4 required very less area and less delay to implement the proposed encoder technique compared with other FPGA devices.

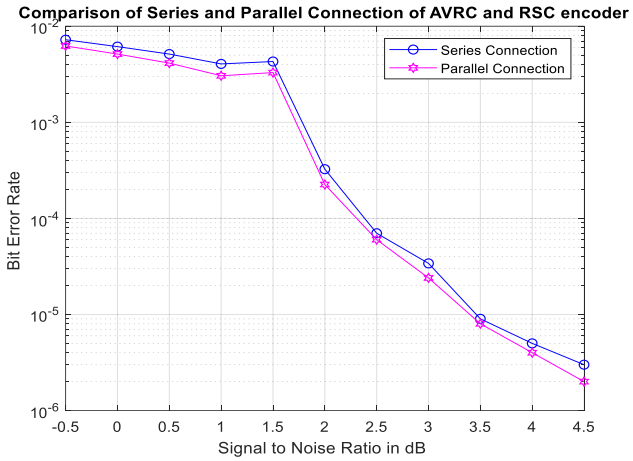

Figure 8: Comparison of Series and Parallel Connection

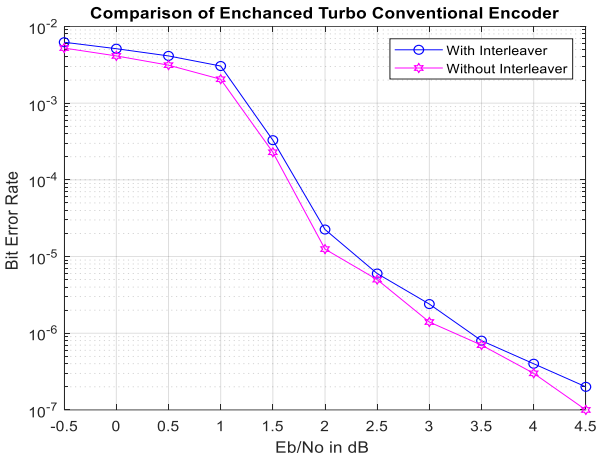

Figure 9: Comparison of Enhanced Turbo Convolutional Encoder of AVRC and RSC Encoder

Table 1: Performance analysis of Hybrid Encoder with AVRC and RSC for Virtex 4

Encoder types	Area (μm²)	Delay (ns)	Power (mW)
AVRC	59401	6.9	158.6
RSC	42572	4.6	167.8
Hybrid Encoder	10593	3.8	145.3

Table 2: Performance analysis of Hybrid Encoder with AVRC and RSC for Virtex 5

Encoder types	Area (μm²)	Delay (ns)	Power (mW)
AVRC	50801	7.6	187.3
RSC	40102	5.3	173.7
Hybrid Encoder	12345	4.6	166.4

Table 3: Performance analysis of Hybrid Encoder with AVRC and RSC for Spartan 6

Encoder types	Area (μm²)	Delay (ns)	Power (mW)
AVRC	49975	7.9	179.4
RSC	39472	5.6	157.9
Hybrid Encoder	13993	4.8	147.5

5. CONCLUSION

The proposed an adaptive Hybrid Variable Convolutional encoding technique uses the Recursive systematic Convolutional encoder and Variable Rate Convolutional Encoder. From the simulation results, it is inferred that it achieves better Bit Error Rate and Throughput by involving the serial and parallel connection of above-mentioned encoder techniques. At the receiver side, Viterbi decoding method is employed to improve the performance of the communication model. The implemented results shows that it requires very less power, processing time, lesser number of gates, LUT's and clock cycles compared with existing encoding techniques. The proposed system achieves better efficiency and QoS by introducing the interleaver block between the RSC and AVRC encoder techniques. In future, it may be improved by involving the different types of interleaver technique such as pseudo random interleaver, circular shifting interleaver, and semi random interleaver block in between the encoder to improve the system performance in terms of processing time, power consumption, throughput, Bit Error Rate, Signal to Noise Ratio and delay. Also, it may be improved by addressing the adaptive modulation techniques based on channel estimation, bandwidth availability and received signal strength.

REFERENCES

[1] X. Gao, S. Han and C. Luo, A Detection and Verification Model Based on SSD and Encoder-Decoder Network for Scene Text Detection, IEEE Access, vol. 7, pp. 71299-71310, May 2019, doi: 10.1109/ACCESS.2019.2919994.

[2] B. Sansoda and S. Choomchuay, "Performance evaluation of error correction code in MIMO scheme for WBAN channel," 2014 International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS), pp. 230-233, December 2014, doi: 10.1109/ISPACS.2014.7024458.

[3] T. Le and Y. Duan, REDN: A Recursive Encoder-Decoder Network for Edge Detection, IEEE Access, vol. 8, pp. 90153-90164, May 2020, doi: 10.1109/ACCESS.2020.2994160.

[4] Y. Cai, FPGA Investigation on Error-Flare Performance of a Concatenated Staircase and Hamming FEC Code for 400G Inter-Data Center Interconnect, Journal of Lightwave Technology, vol. 37, no. 1, pp. 188-195, 1 January 2019, doi: 10.1109/JLT.2018.2881924.

[5] L. Liu and S. Liao, Optical Binary Encoder and Decoder With Ultra-Low Power Consumption, IEEE Photonics Technology Letters, vol. 32, no. 17, pp. 1113-1116, September 2020, doi: 10.1109/LPT.2020.3013808.

[6] Luis-J. Saiz-Adalid, Joaquín Gracia-Morán, Daniel Gil-Tomás, J.-Carlos Baraza-Calvo and Pedro-J. Gil-Vicente, Ultrafast Codes for Multiple Adjacent Error Correction and Double Error Detection, IEEE Access, pp. 1-9, October 2019.

[7] F. Qi, C. Lin, G. Shi and H. Li, A Convolutional Encoder-Decoder Network With Skip Connections for Saliency Prediction, IEEE Access, vol. 7, pp. 60428-60438, May 2019, doi: 10.1109/ACCESS.2019.2915630.

International Journal of
Electrical and Electronics Research (IJEER)
Research Article | Volume 10, Issue 3 | Pages 523-528 | e-ISSN: 2347-470X

[8] P. Reviriego, S. Pontarelli and A. Ullah, Error Detection and Correction in SRAM Emulated TCAMs, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 27, no. 2, pp. 486-490, February 2019, doi: 10.1109/TVLSI.2018.2877131.

[9] Sufia Banu and Shweta Gupta (2022), Design and Leakage Power Optimization of 6T Static Random Access Memory Cell Using Cadence Virtuoso. IJEER 10(2), 341-346. DOI: 10.37391/IJEER.100246.

[10] EunHwa Kim (2022), Fan-Shaped Flooding in Wireless Sensor Networks. IJEER 10(2), 225-229. DOI: 10.37391/IJEER.100230.