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Digital Hysteresis Control Algorithm for Switched Inductor Quasi Z-Source Inverter with Constant Switching Frequency

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ABSTRACT- In this paper, a digital hysteresis current limit controller is developed for Switched Inductor Quasi Z-Source Inverter (SLQZSI). Traditional methods like hysteresis current fixed limit and adjustable hysteresis current limit techniques changes the hysteresis bandwidth in accordance to modulating frequency and gradient of reference current. The operating shifting frequency of typical approaches oscillates and crosses the intended steady shifting frequency under noise. It leads to undesirable heavy interference between the phases and more power loss. In the planned digital hysteresis current limit technique, the hysteresis current limit is calculated by resolving the optimization problem. In the proposed approach the operating shifting frequency is kept same or inferior to the intended steady shifting frequency even under noise. Hence the planned digital hysteresis current limit algorithm maintains the output current steady and power loss is minimized which is not promised by the conservative techniques. To compare different control strategies in terms of nature of operating switching frequency and harmonic performance simulations are built on the MATLAB/SIMULINK.

Keywords: Digital Control, Hysteresis Control, Optimization problem, SLQZSI**,** Switching frequency, Total Harmonic Distortion.

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1. INTRODUCTION

Now a days in most applications such as enabling wider propagation of non-conventional energy production, [1,2] the recognition of new grid ideas with elevated effectiveness [3,4], inverters and their controllers have been receiving increased attention. There are three major classes of current control techniques, for instance sinusoidal triangle Pulse Width Modulation (PWM), predictive dead beat, hysteresis current control are developed over last few decades. The asynchronous sinusoidal delta PWM procedure needs a Proportional Integrator (PI) regulator to vary the current mismatch and often causes inevitable delay. The deadbeat predictive control procedure is extremely reliant on the precision of the predictive model, but is very convoluted to execute on the contrary, Hysteresis current control is easier to apply and has rapid vibrant response. This technique does not involve any particulars regarding the system speed and accuracy, hence strength of the procedure is enhanced. Therefore, this hysteresis current control procedure meets applications in a wide range of switching inverters.

2. LITERATURE REVIEW

In Hysteresis current control approach, the switching pulse is obtained by analyzing the real current and reference current, hence current mistake lies inside the acceptance current limit. In symphonic hysteresis current controllers [5,6], the hysteresis current limit is preset to a definite rate. This creates the shifting frequency to fluctuate with the purpose of include the current wave inside the limit. In adaptive hysteresis current control approach the current limit is managed adaptively in every shifting modulation cycle.

In digital hysteresis current control, a suitably high sampling frequency is required to operate the inverter switches with exact shifting time. The ripple current is contrary comparative to production inductance and directly comparative to diversity among the DC and output voltages. So ripple current shifts fastly during every switching modulation. In the sampling time, the hysteresis current limit is not realized awaiting the appearance of subsequent data sample. A small sampling rate leads to a significant overrun of the hysteresis limit ripple current [8,9].

The elevated switching rate has numerous advantages such as lesser ripple current and quicker transient response, for example, if a motor is hastened starting idle to rated speed, and in order to have small current alteration the inverter switches [10,11] are made to operate at their highest possible switching

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components and are enforced to transform its on – off states at a frequency outside its border. Because of presence of noise, short circuit problem may arise and leading to damage of shifting devices. Hence utmost care should be taken to control properly the hysteresis current band, making the frequency of the switching mechanisms not to go beyond their peak achievable switching frequency [12,13].

The typical approach uses the estimated voltage on the moment while the switches begin a current modulation cycle. Especially with the noise, the traditional approach [14,15] is not guaranteed to go beyond the highest switching frequency limit. The study of all literature review does not reveal the digital hysteresis control limit technique for SLQZSI using optimization resolution. The present work illustrates a novel digital hysteresis current control approach which considers the feedback data from the proceeding modulation cycle in to account. This technique keeps the switching frequency stable and constantly under the peak possible switching frequency even noise is present.

In this research work, *Section 3* deals with classical hysteresis current fixed limit control approach, *Section 4* presents Typical Adjustable Hysteresis Current Control Technique, *Section 5* introduces Digital Hysteresis Current Control Technique, *Section 6* shows the simulation results and *Section 7* summarizes conclusions.

3. CLASSICAL HYSTERESIS STABLE LIMIT CURRENT CONTROL TECHNIQUE

Consider the switching devices S_1 and S_2 in one leg phase of SLQZS inverter circuit. As seen in *Figure 1*, the output is connected to the Induction Motor ac voltage V_m. The DC voltage is supplied by a DC source has the value of V_{dc}. The switching devices S_1 and S_2 controls inverter output current i_L to track the given reference current i_{ref} current ripple filter removes the ripple content of output current i_L and output current i_0 enters into motor without a ripple component. In *Table 1*, Inputs and Outputs of inverter are shown along with the state of the switches.

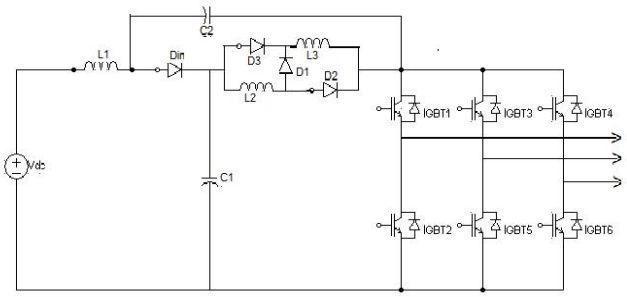

Figure 1: SL-QZSI Topology

Table 1: Switching States and their respective outputs

Half Period	S_1	S_2	V_{dc}	i_L
Positive	ON	OFF	V_{dc}	Rise
Negative	OFF	ON	-V_{dc}	Fall

The Tolerance current limit is set to a definite assessment Δi_b. No shifting occurs, if the output current i_L is among the higher and lesser boundary. The current begins to diminish when the switch S_1 is twisted off after that switch S_2 is twisted on, if the estimated output current passes over the upper limit of hysteresis band $(\Delta i_{ref} + \Delta i_b)$. The S_1 is turned ON, the switch S_2 is twisted OFF and current begins to rising if the calculated output current moves below the lesser boundary of hysteresis limit $(\Delta i_{ref} - \Delta i_b)$ as shown in *figure 2.*

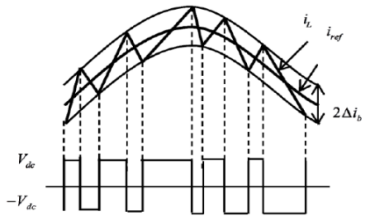

Figure 2: Stable band hysteresis current control

The hysteresis current limit is inversely proportional to shifting frequency and directly proportional to current ripple. As a result, increasing the hysteresis current limit value increases the current ripple, whereas decreasing the hysteresis current limit value increases the switching loss. In analogue regulators, the current swell is forever maintained inside the hysteresis group. Here digital controllers, the current limit must be selected to meet the criteria.

$$\Delta i_b > \max\left(\frac{di_{ref}}{dt}\right)\frac{1}{f_{sp}} \quad [1]$$

Where f_{sp} is the sampling frequency. The highest shifting frequency f_{sw_max} must be lesser compared to the partially the sampling frequency.

$$f_{sw\_max} \leq \frac{1}{2} f_{sp} \quad [2]$$

Stable limit hysteresis current Controller is very simple to implement, fast and stable response and is independent to changes in parameters of the load and power supply. The maximum peak current ripple is organized by any means the points on primary frequency signal by varying the switching frequency.

4. TYPICAL ADJUSTABLE HYSTERESIS CURRENT CONTROL TECHNIQUE

Symphonic hysteresis current technique introduces an undesirable heavy interference between phases in three-phase systems. So as to get better, an adjustable hysteresis current organized approach is implemented. In every switching modulation cycle, the current limit is not fixed but is controlled adaptively. Current limit is controlled based on the calculated output voltage values and the targeted switching constant frequency.

The current error $\Delta i(t)$ at time 't' is given by the expression

$$\Delta i(t) = i_L(t) - i_{ref}(t) \quad [3]$$

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Where $i_L(t)$ and $i_{ref}(t)$ are the inverter output and reference current at time instant‘t’.

The current error at time instant ‘t_0’is $\Delta i(t_0)$ as shown in *Figure 3*. Let at ‘t_0’ the output current i_L tends to pass over the lower hysteresis band, Switch S_1 is closed during $[t_0, t_1)$ intervals and open during $[t_1, t_2]$ intervals. Positive turn on and negative turn off durations are the terms for these intervals.

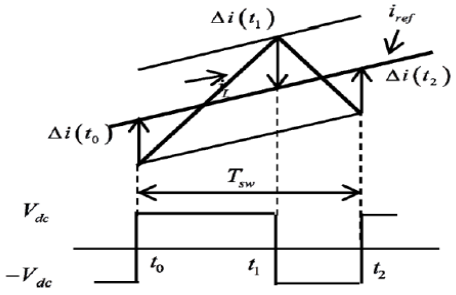

Figure 3: Typical adjustable hysteresis current control

The dynamic formula for output current can be expressed as:

$$\frac{di_L(t)}{dt} = \frac{v_{dc}(t) - v_m(t)}{L} \quad [4]$$

$$v_{dc}(t) = \begin{cases} v_{dc} & if\ S_1 is\ ON \\ -v_{dc} & if\ S_1\ is\ OFF \end{cases} \quad [5]$$

The output current gradients in the ON and OFF phases are defined as I_{ON} and I_{OFF} respectively.

Now during the switching modulation period $[t_0, t_2]$, output voltage is slowly varying. Hence the output current gradients (4) be able to be stated like

$$\dot{I}_{ON} = \frac{di_L(t)}{dt} = \frac{v_{dc} - v_m(t_0)}{L} \quad \text{for t} \in [t_0, t_1) \quad [6]$$

$$\dot{I}_{OFF} \triangleq \frac{di_L(t)}{dt} = \frac{-v_{dc} - v_m(t_0)}{L} \quad \text{for t} \in [t_1, t_2) \quad [7]$$

During the positive turn on and negative turn off cycles, the current mistakes are given by

$$\Delta i(t_1) = i_L(t_1) - i_{ref}(t_1) \quad [8]$$

$$= i_{ref}(t_0) + \Delta i(t_0) + \dot{I}_{ON}\, T_{ON} - i_{ref}(t_1) \quad [9]$$

$$\Delta i(t_2) = i_L(t_2) - i_{ref}(t_2) \quad [10]$$

$$= i_{ref}(t_0) + \Delta i(t_0) + \left(\dot{I}_{ON} T_{ON} + \dot{I}_{OFF} T_{OFF}\right) - i_{ref}(t_2) \quad [11]$$

For the switch S_1, T_{ON} and T_{OFF} are the on and off periods and they are expressed as

$$T_{ON} = t_1 - t_0 \quad [12]$$

$$T_{OFF} = t_2 - t_1 \quad [13]$$

During the modulation period the reference current slowly varies and it can be approximated as

$$i_{ref}(t_1) = i_{ref}(t_0) + \dot{I}_{ref}(t_0) T_{ON} \quad [14]$$

$$i_{ref}(t_2) = i_{ref}(t_0) + \dot{I}_{ref}(t_0)(T_{ON} + T_{OFF}) \quad [15]$$

$$\dot{I}_{ref}(t_0) = \left.\frac{di_{ref}(t)}{dt}\right|_{t=t_0} \quad [16]$$

The current errors can be determined by substituting equations [14] and [15] in [9] and [11]

$$\Delta i(t_1) = \Delta i(t_0) - \dot{I}_{ON}\, T_{ON} \quad [17]$$

$$\Delta i(t_2) == \Delta i(t_0) + \dot{I}_{ON}\, T_{ON} + \dot{I}_{OFF}\, T_{OFF} \quad [18]$$

Where $\dot{I}_{ON}$ and $\dot{I}_{OFF}$ are the current mistake gradient in positive turn on and negative turn off cycles and are represented as

$$\dot{I}_{ON} = \dot{I}_{ON} - \dot{I}_{ref}(t_0) = \frac{v_{dc} - v_m(t_0)}{L} - \dot{I}_{ref}(t_0) \quad [19]$$

$$\dot{I}_{OFF} = \dot{I}_{OFF} - \dot{I}_{ref}(t_0) = \frac{-v_{dc} - v_m(t_0)}{L} - \dot{I}_{ref}(t_0) \quad [20]$$

The targeted constant switching frequency is denoted as f_{sw}. In the typical adjustable hysteresis current control approach, the hysteresis current limit $\Delta i_b(t_0)$ is deduced by using the following conditions:

$$\Delta i(t_1) - \Delta i(t_0) = 2\Delta i_b(t_0) \quad [21]$$

$$\Delta i(t_2) - \Delta i(t_1) = -2\Delta i_b(t_0) \quad [22]$$

$$T_{ON} + T_{OFF} = T_{sw} \quad [23]$$

where $T_{sw} = \frac{1}{f_{sw}}$ is the targeted constant switching time. Inserting equations [21]–[23] into
Equations [17] and [18], the hysteresis current band is deduced as:

$$\Delta i_b(t_0) = \frac{1}{2} \frac{\dot{I}_{ON} \dot{I}_{OFF}}{\dot{I}_{OFF} - \dot{I}_{ON}} T_{sw} \quad [24]$$

By inserting equations [19] and [20] into Equation [24], the hysteresis limit in Equation [24]
also be drafted as:

$$\Delta i_b(t_0) = \frac{V_{dc} T_{sw}}{4L}\left(1 - m^2(t_0)\right) \quad [25]$$

$$m(t_0) = \frac{1}{V_{dc}}\left(v_m(t) + L\dot{I}_{ref}(t)\right) \quad [26]$$

while the inverter is working in the presence of noise, the negative half switching time T_{OFF_pre} in the earlier modulation shorter than the designed parameter, then working shifting frequency exceeds the highest possible shifting frequency.

5. DIGITAL HYSTERESIS CURRENT CONTROL TECHNIQUE

Figure 4 shows the arrangement of digital control technique. ADC measures and samples output voltage and current. These samples are applied for figuring ON/OFF pulses of switches S_1 and S_2.

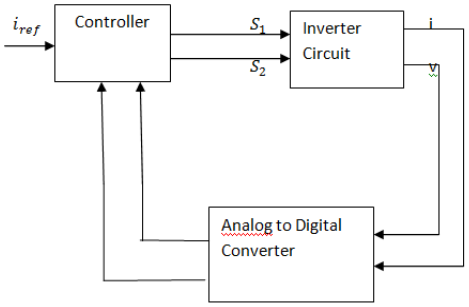

Figure 4: Arrangement of Digital Hysteresis Current Control Technique

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At instant t_0 if the output current crosses the lower band $(\Delta i_{ref} + \Delta i_b)$ and the switch S_1 is about to switch ON as depicted in *figure 5*. The negative turn off cycle of switch S_1 in the previous modulation time T_{OFF_pre}

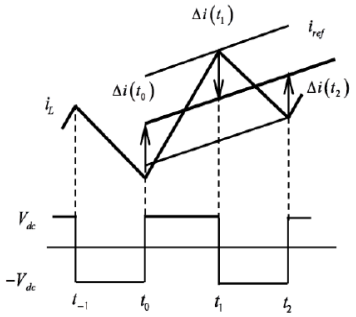

Figure 5: Digital hysteresis current control

This method provides an optimization problem fo computing hysteresis band as

$$T_{OFF\_pre} = t_0 - t_{-1} \quad [27]$$
$$(i) T_{OFF\_pre} + T_{ON} \geq T_{sw} \quad [28]$$
$$(ii) T_{ON} + T_{OFF} = T_{sw} \quad [29]$$
$$(iii) \Delta i_b = \Delta i(t_1) = -\Delta i(t_2) \quad [30]$$
$$(iv) \Delta i_b \geq \Delta i_{conv} \quad [31]$$
$$\text{Minimise J} = \left(\Delta i(t_1)\right)^2 + \left(\Delta i(t_2)\right)^2 \quad [32]$$

where Δi_{conv} is the hysteresis current limit estimated with the typical approach while in equation [24], and objective function is denoted as J.

Limitation constraints *(i)* and *(ii)* justify the working shifting frequency to exist identical otherwise lesser than targeted moment shifting frequency. Condition *(iii)* sets the mean magnitude of output current similar to the mention current through the shifting modulation cycle. Constraint *(iv)* prevents the amount produced current as of diverging as of the reference current. In every shifting modulation cycle, the power loss from the inverter is represented by the objective function J. The hysteresis limit is estimated to minimize energy loss J.

Equations [17] and [18] may be drafted like

$$T_{ON} = \frac{1}{\dot{I}_{ON}}\left(\Delta i(t_1) - \Delta i(t_0)\right) \quad [33]$$
$$T_{OFF} = \frac{1}{\dot{I}_{OFF}}\left(\Delta i(t_2) - \Delta i(t_1)\right) \quad [34]$$

Inserting equations [33] and [34] into equation [27]-[32], the optimization problem can be drafted as:

$$(i)\ \Delta i(t_1) \geq \dot{I}_{ON}\left(T_{sw} - T_{OFF\_pre}\right) + \Delta i(t_0) \quad [35]$$
$$(ii)\left(1 - \frac{\dot{I}_{ON}}{\dot{I}_{OFF}}\right)\Delta i(t_1) + \frac{\dot{I}_{ON}}{\dot{I}_{OFF}}\Delta i(t_2) \geq \dot{I}_{ON} T_{sw} + \Delta i(t_0) \quad [36]$$
$$(iii)\ \Delta i(t_1) = -\Delta i(t_2) = \Delta i \quad [37]$$
$$(iv)\ \Delta i_b \geq \Delta i_{conv} \quad [38]$$
$$\text{Minimise J} = \left(\Delta i(t_1)\right)^2 + \left(\Delta i(t_2)\right)^2 \quad [39]$$

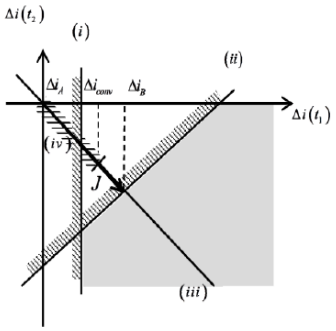

Figure 6: Hysteresis current band domain and optimal solution

The constraints make the optimization problem linear. Using Graphical method, the constraints are solved. The restriction *conditions (i)-(iv)* are depicted in *figure 6* as a black patch in the phase plane $(\Delta i(t_1), \Delta i(t_2))$ indicating the viable region. The separation from the initial stage –plane to point $(\Delta i(t_1), \Delta i(t_2))$ gives the objective function J. Hence from the graph the optimal solution is the point $(\Delta i(t_1)s, \Delta i(t_2)s)$ on the viable region, close near the initial value. The optimal result be able to determine like

$$\Delta i_{opt} = max\left(\Delta i_{conv}, \Delta i_{A,} \Delta i_B\right) \quad [40]$$

Where Δi_{conv}, $\Delta i_{A,}$ Δi_B be the points which fulfill combine limitation constraints (i, iii), (ii, *iii*), (*iv*, *iii*), correspondingly, and are known as

$$\Delta i_A = \dot{I}_{ON}\left(T_{sw} - T_{OFF\_pre}\right) + \Delta i(t_0) \quad [41]$$
$$\Delta i_B = \frac{\dot{I}_{ON} T_{sw} + \Delta i(t_0)}{1 - 2\frac{\dot{I}_{ON}}{\dot{I}_{OFF}}} \quad [42]$$
$$\Delta i_{conv} = \frac{1}{2}\frac{\dot{I}_{ON}\dot{I}_{OFF}}{\dot{I}_{OFF} - \dot{I}_{ON}} T_{sw} \quad [43]$$

When the optimal solution is at Δi_A, negative turn off cycle T_{OFF_pre} is the previous switching modulation was lesser than normal value. To satisfy the *condition (i)*, hysteresis current band is to be broadened. When the optimal solution is at Δi_B, average output current deviated from reference current. To satisfy the *condition (ii)*, hysteresis current band is to be broadened. Whenever the most favourable resolution is at Δi_{conv} it signifies to *condition (i)* along with *(ii)* have been met, and the hysteresis current limit ought to be elicited to relentless position as in typical approach.

6. RESULTS AND DISCUSSION

To judge the performance of planned approach and to compare with the typical approach, simulations have been carried out using MATLAB. The transistors available in inverter circuit were represented by IGBT. The output inductance L=1mH and filter capacitor of C=10μF.The inverter was powered by dc voltage of v_{dc} =100V and an ac voltage of V_m =15 $\sqrt{2}$ $\sin(100\pi t)$. i_{ref} =10 $\sin(100\pi t)$ were used as reference current, f_{sp} =2MHz was the sampling frequency of analog to digital converter.

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Noise is assumed as White noise with Variance of 0.01A. This can arise from a current sensor or an analog to digital Converter. *Figure 7* displays simulation diagram of SLQZSI with digital Hysteresis control. *Figure 8* displays gate pulses for IGBT switches generated by planned technique. In *Figure 9* Current Vs time curve shows the hysteresis current limit response for intended shifting frequency at 40KHZ. The switching frequency Vs time curve displays the nature of operating shifting frequency among planned and traditional approach. It is noticed that the response of operating frequency crosses the intended steady switching frequency of 40 kHz for typical method and it lies below the intended steady switching frequency for planned method.

In *Figure 10* Current Vs time curve shows the hysteresis current limit response for intended shifting frequency at 20KHZ. The switching frequency Vs time curve displays the nature of operating shifting frequency among planned and traditional approach. It is noticed that the response of operating frequency crosses the intended steady switching frequency of 20 kHz for typical method and it lies below the intended steady switching frequency for planned method.

In *Figure 11* Current Vs time curve shows the hysteresis current limit response for intended shifting frequency at 10KHZ. It is observed that the output current is similar to reference current. The switching frequency Vs time curve displays the nature of operating shifting frequency among planned and traditional approach. It is noticed that the response of operating frequency crosses the intended steady switching frequency of 10 kHz for typical method and it lies below the intended steady switching frequency for planned method.

Figure 12 displays FFT analysis of Phase current for digital hysteresis current limit approach. It is observed that digital hysteresis current limit approach for SLQZSI reduces THD in phase current to 4.16% and it is lesser than the typical approaches. *Table 2* depicts Performance comparison of Hysteresis current fixed limit, Adjustable hysteresis current limit, and digital hysteresis current limit approach for SLQZSI. *Table 2* illustrates the superior performance of digital hysteresis current limit approach compared with hysteresis current fixed limit approach and adjustable hysteresis current limit approach in terms of THD reduction and nature of operating shifting frequency.

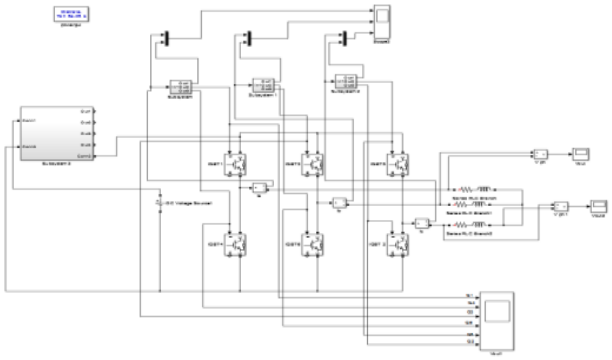

Figure 7: Schematic diagram of SLQZSI with Digital hysteresis control

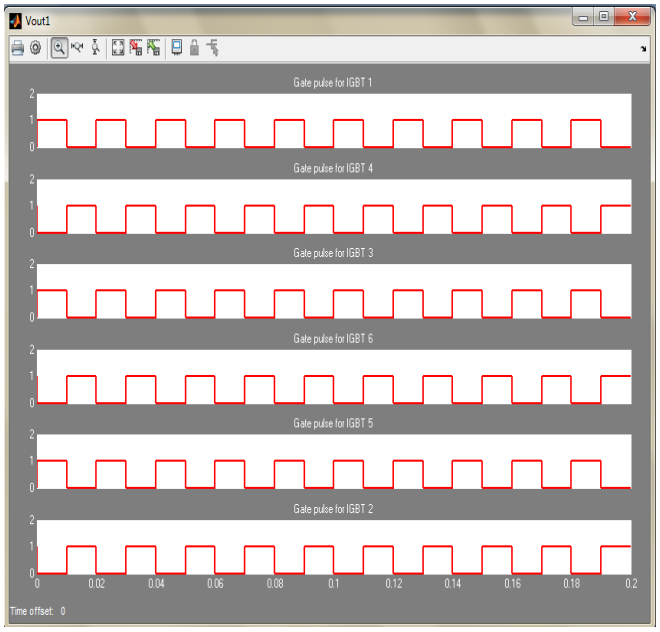

Figure 8: Gate pulses for the IGBT switches

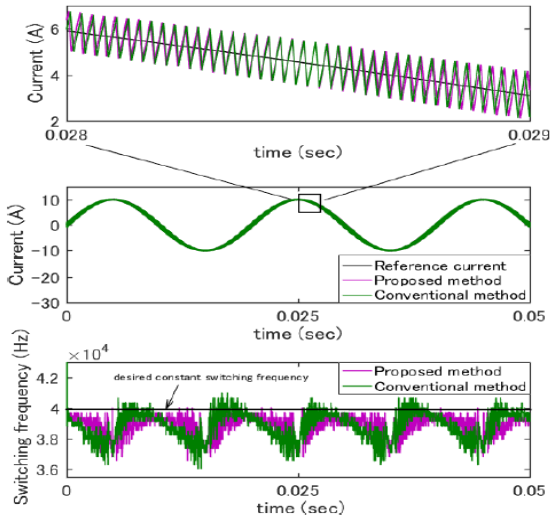

Figure 9: Current waveform and shifting frequency waveform for the intended shifting frequency at 40KHZ

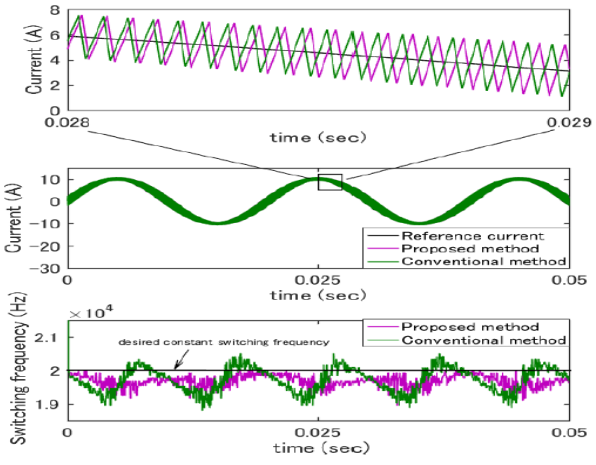

Figure 10: Current waveform and shifting frequency waveform for the intended shifting frequency at 20KHZ

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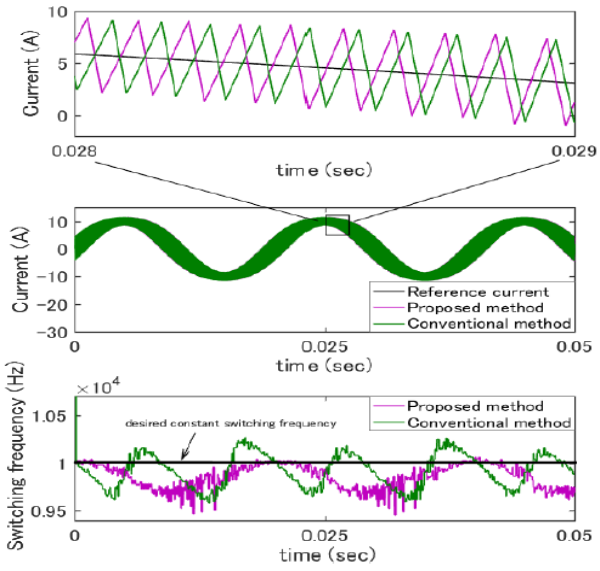

Figure 11: Current waveform and shifting frequency waveform for the intended shifting frequency at 10KHZ

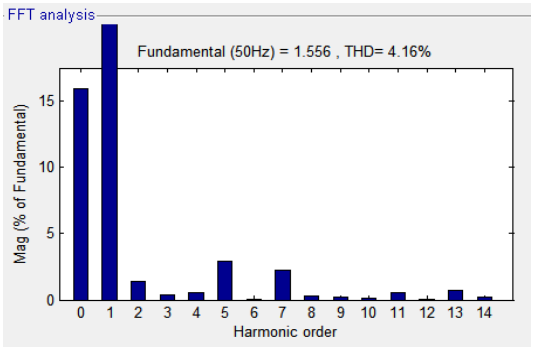

Figure 12: FFT analysis of Phase current for digital hysteresis current limit approach

Table 2: W Performance comparison of three approaches for SLQZSI

Algorithm	THD	Intended Shifting Frequency		
		40KHZ	20KHZ	10KHZ
Hysteresis current fixed limit approach	29.00%	Operating Switching Frequency crosses at 4HZ	Operating Switching Frequency crosses at 2HZ	Operating Switching Frequency crosses at 1HZ
Adjustable hysteresis current limit approach	7.75%	Operating Switching Frequency crosses at 4HZ	Operating Switching Frequency crosses at 2HZ	Operating Switching Frequency crosses at 1HZ
Digital hysteresis current limit approach	4.16%	Operating Switching Frequency lies below 4HZ	Operating Switching Frequency lies below 2HZ	Operating Switching Frequency lies below 1HZ

7. CONCLUSION

A digital hysteresis current limit controlled SLQZSI has been modeled and simulated successfully using MATLAB Simulink. The simulation result of planned algorithm indicates the THD in phase current is reduced to 4.16% and optimization solution is chosen such that the following setbacks are satisfied. (i) Shifting frequency is steady and for all time kept at identical or lesser than preferred stable switching frequency (ii) The produced current is steady about the suggestion current (iii) Power loss is minimal. The hypothetical mathematical and simulation outcomes illustrate good performance of planned algorithm over the traditional methods. The planned algorithm may be implemented in future with high-speed Field Programmable Gate array circuit.

8. ACKNOWLEDGMENT

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