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Optimization of Harmonics in Novel Multilevel Inverter using Black Wolf and Whale Optimization algorithms

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ABSTRACT- High-quality electrical energy is the most needed thing for standard living. We use power electronics converters for the conversion of different forms of electrical energy and we use them for producing quality power output. We use semiconductor devices as switches in the process of conversion of DC-DC, AC-DC, AC-AC, and DC-AC according to the requirement of the system. In this paper, an attempt is made to analyze the quality of output power from a multilevel inverter which is used in the conversion of DC supply to AC output voltage. Production of quality power by optimizing the multilevel inverter switching using Whale Optimization Algorithm helps the proposed inverter topology to perform well. The suggested topology and the optimization technique will help in harvesting multiple renewable energy sources with improved quality of power. Different DC sources of different voltage levels could be connected in input and the resultant AC output has less ripple content as per the IEEE standard. A detailed comparison has been made to show the superiority of the proposed algorithm.

Keywords: Power Quality, Multilevel inverter, Cascaded H-bridge, Optimization technique, Whale Optimization Algorithm, Black Widow Optimization Algorithm.

1. INTRODUCTION

The presence of harmonics in the electrical power system leads to voltage distortion and that may affect the equipment and loads connected to it. Maintaining high-quality power is important in systems. To achieve this, multilevel inverter receives more attention due to increasing utilization in the power industry for getting quality power. The need for an inverter of multilevel is to provide power output from voltage sources of medium size. Also, this multilevel inverter plays a vital role in harvesting solar energy. This manuscript describes an approach to obtaining good quality power using a multilevel inverter that receives input supply from different sources like batteries, solar panels, and fuel cells. An innovative symmetric multilevel inverter topology is described in this study, and its performance is evaluated using the MATLAB-SIMULINK software. In our paper, we used soft computing techniques for the elimination of harmonics which is considered an optimization task in the process of obtaining good quality of power.

A careful and comprehensive literature survey was made for designing a new optimum multilevel inverter topology and working out the best switching policy to minimize the harmonic distortion. The diode clamped multilevel inverter, the multilevel inverter based on flying capacitor, as well as the cascaded topology of multilevel inverter with different DC sources are explored [1].Controlling the harmonics existing in the output voltage of inverter is examined using modulation methods such sinusoidal pulse width modulation, selectively removing harmonic, and space vector modulation. Analyzing the use of these converters, such as conveyor belts and unified power flow controllers, attracts special emphasis. In [2,] a detailed proposal for high voltage and high power applications, such as hybrid electric vehicle (HEV) motor drives, is offered using a transformer less multilevel inverter. MLI can generate nearly sinusoidal output voltage with a fundamental switching frequency. In a cascaded multilevel inverter, several separate DC voltage sources are used, which can be from batteries, ultra-capacitors, or fuel cells. As a consequence, cascaded MLI is acceptable for larger hybrid electric vehicle drives. The simulation and practical findings demonstrated how to use this inverter for hybrid electric vehicle applications. In [3,] a cascaded multilevel inverter topology was created using only a single DC power supply and capacitors. For (2n+1) output voltage levels, the basic cascaded multilevel inverter structure requires n number of different DC sources. However, a single DC power supply with (n-1) capacitors is used to create a recommended topology in this proposed study. The capacitors' DC voltage levels were maintained in this system, and a fundamental switching frequency pattern was used to generate a nearly sinusoidal output voltage. To avoid harmonics in the output voltage, the turn on angles were chosen. An efficient PWM switching task for modified multilevel inverter based on H-bridge is available in [4]. The output voltage THD is minimized by adding PWM switching schemes with modified H-bridge MLI. The key disadvantage of this symmetric arrangement is that the size of the inverter grows linearly in proportion to the level. As a result, conduction losses grow, and

switches conducting at lower levels must also conduct for all levels. As a result, these switches are under a great deal of stress. This design does not allow for the use of asymmetric source configurations to further minimize the number of switches. [5] demonstrated a two-source topology. The structure appears to be simple, yet the control strategy is complicated. This architecture does not appear to support symmetrical source arrangements. The selective harmonic elimination PWM methodology is commonly used on multilayer series-connected voltage source PWM inverters. Optimization techniques are used to implement the procedure. A phase-shift harmonic suppression strategy is used to reach the optimization starting point.

Higher frequency switching modulation approaches minimize the filter size but increase losses occurring due to switching. Step modulation uses a lower switching frequency and potentially lower losses, at the same time it necessitates a larger filter size. The level number of the inverter is raised to minimize the filter size; however, this boosts the system's cost. [5] developed a fresh modulation method in which supplementary notches in the multilevel output voltage are introduced. Such notches remove harmonics of the order low and shift them to a higher order, enabling the filter design size to be minimized without worsening the system's switching loss or cost. The suggested modulation approach is validated in practice with a prototype of five level diode clamped inverter, as well as through simulation.

[6] presents an innovative modulation technique for multilevel inverters called carrier-transposed multicarrier modulation, which combines the benefits of phase-shifted multicarrier modulation technique's equal switching frequency in addition to even power distribution with best harmonic performance of level-shifted multicarrier modulation technique. The performance of four distinct sequential switching hybrid-modulation techniques for multilevel inverters of cascaded nature was examined and compared in [7]. To prove the feasibility of hybrid modulations, the author employed spectrum analysis, power loss analysis, modelling, and experimental data.

Multi-carrier Sinusoidal Pulse Width Modulation (SPWM) approaches are commonly employed for different multilevel inverter topologies among the many modulation techniques for multilevel inverters mentioned in [8]. As an attempt to use soft computing to such an optimization problem, [9] offered a new approach for selecting optimal switching angles established on the Firefly algorithm. The results illustrate that the suggested firefly algorithm can remove specific harmonics in a multilevel inverter's output voltage. To reduce THD in the inverter, [10,12] recommended a particle swarm optimization strategy and [11,12] suggested a Genetic Algorithm approach. Soft computing strategies have been shown to be successful in lowering the THD of a multilayer inverter in Teaching Learning-based optimization [13].

From the literature survey, it is understood that the multilevel concept with selective harmonic elimination using soft computing algorithm is a research domain where many attempts are being made.

2. PROBLEM STATEMENT

The goal of this manuscript is to recommend new multilevel inverter architecture with fewer switching devices, as well as to discover appropriate soft computing strategies to accomplish high-quality power. In this line, this paper presented recent soft computing algorithms like Whale Optimization Algorithm and Black Widow Optimization Algorithm for finding a better solution for such problems and identifying the best-suited one. A MATLAB-Simulink environment is used to model the suggested multilevel inverter with lowered switches, and the aforementioned soft computing approaches are used to get the lowest THD. Hardware verification of such a multilevel inverter is also carried out.
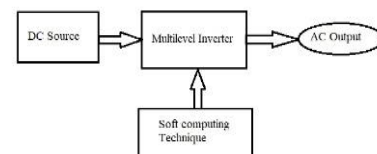
3. BLOCK DIAGRAM

Figure 1: Block diagram of the proposed system

The recommended system is simulated as a 21-level multilevel inverter whose triggering is derived from a soft computing algorithm. Ten DC sources are required for a 21-level inverter. Since this is a symmetric topology an equal voltage of 25 V is given to each DC source. Soft computing techniques have been used to optimize the harmonics in multilevel inverter. Using Whale Optimization Algorithm (WOA) and Wolf Optimization techniques, the best combination of switching angles is found and given to multilevel inverter so that AC output with minimum Total Harmonic Distortion can be obtained.

4. MULTILEVEL INVERTER

A multilevel inverter is a wise option for medium and high-voltage applications because it can create a suitable voltage output from a variety of input DC voltages. The first major goal of this study is to establish a new topology followed by the use of soft computing power for obtaining quality power. Aside from the traditional topologies, various customized topologies for both symmetric multilevel inverters with lower device count have been introduced in the earlier literature. The fundamental Cascaded H-Bridge (CHB) architecture is used to create several topologies.
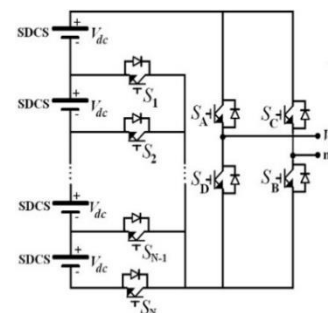

Figure 2: Topology for N level Multilevel Inverter

For a single phase, *figure 2* shows the suggested symmetric multilayer inverter. Separate sources of DC nature (N), primary

switches (N), and a single H-bridge cell make up this inverter. The magnitude of the separate DC sources (SDCS) used in the proposed topology is equal to V_{dc}. An H-bridge is used in each half cycle to shift the polarity of the voltage output and generate a zero voltage level. Different levels of the output voltage are created depending on the states of the switches. Switches S_A, S_B, and S_1 are turned on to gain $+V_{dc}$, while switches S_C, S_D, and S_1 are used to obtain $-V_{dc}$. S_A, S_B, and S_2 switches are activated to obtain $+2V_{dc}$, while switches including S_C, S_D, and S_2 are used to obtain $-2V_{dc}$. AC voltage for each level may be calculated in the same way. Turning on S_A and S_C or S_B and S_D result in a zero level. The major switches (S_1, S_2, S_3,.....S_N) create AC output voltage levels ranging from V_{dc} to NV_{dc}. A proposed N-level multilevel inverter's output phase voltage waveform is derived by

$$V_{an}(\omega t) = V_{a1}(\omega t) + V_{a2}(\omega t) + \ldots + V_a(N-1)(\omega t) + V_{aN}(\omega t) \quad V_a(\omega t) \frac{4V_{dc}}{\pi} \sum_{n=1,3,5} [\cos n\,\theta_1 + \cos n\,\theta_2 + \cos n\,\theta_3 + \ldots \cos n\,\theta_N] \frac{\sin n\omega t}{n}$$

The number of distinct DC sources (N) in a symmetrical multilevel converter can be connected to the functional number of output phase voltages levels (N-level) by:

$$N_{level} = 2N+1$$

$$N_{switch} = N+4$$

When it comes to the number of different DC sources(N), the suggested symmetric multilayer inverter's maximum output voltage ($V_{o.Max}$) is

$$V_{o.Max} = NV_{dc}$$

In the suggested structure of symmetrical multilevel inverter, the condition of the switches at various voltage levels is shown in *Table 1*. For Asymmetric multilevel the topology should have been modified.

Table 1. Different output voltage levels and corresponding state of the switches

Output V_{an}	Switch State							
	S_1	S_2	S_3	…	S_{N-1}	S_N	S_A S_B	S_C S_D
NV_{dc}	0	0	0	…	0	1	1	0
$(N-1)V_{dc}$	0	0	0	…	1	0	1	0
. . .	. . .	. . .	. . .	…	. . .	. . .	. . .	. . .
$3V_{dc}$	0	0	1	…	0	0	1	0
$2V_{dc}$	0	1	0	…	0	0	1	0
V_{dc}	1	0	0	…	0	0	1	0
0	0	0	0	…	0	0	1	1
$-V_{dc}$	1	0	0	…	0	0	0	1
$-2V_{dc}$	0	1	0	…	0	0	0	1
$-3V_{dc}$	0	0	1	…	0	0	0	1
. . .	. . .	. . .	. . .	…	. . .	. . .	. . .	. . .
$-(N-1)V_{dc}$	0	0	0	…	1	0	0	1
$-NV_{dc}$	0	0	0	…	0	1	0	1

Harmonics which are caused during the conversions that occur in multilevel inverters affect the effective functioning of the operating equipment. Harmonics are produced during the usage of non-linear power electronic devices in the system which produces non-sinusoidal output voltage. The effects of harmonics are overheating, electromagnetic interference, electric losses, distorted voltage and current, etc which may cause damage to the power system. So it is necessary to eliminate these harmonics. These harmonics are eliminated using optimization techniques to produce better results. Nearly sinusoidal output voltage waveform can be obtained by using high-level MLI with optimization techniques applied to it. To delete harmonics of a specific order, the selective Harmonic Removal method is utilized. So the optimum switching angles on which the SHE technique is highly dependent can be obtained from the Newton Raphson method.
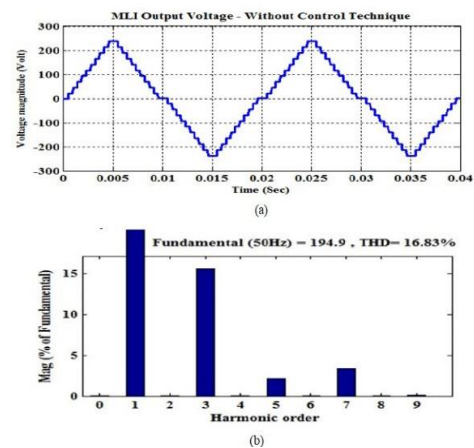

Figure 3: (a) Output voltage waveform (b) FFT Analysis without Control Techniques

The proposed model for 21-level MLI is done with MATLAB-SIMULINK software. Separate DC sources, such as battery packs, fuel cells, and solar, are used. The simulation for the proposed symmetric MLI that generates an output voltage of 250 voltage having separate dc voltages of 26v each is done. A 10-ohm resistive load is selected here.

This is an MLI output voltage waveform without a control technique for a 21-level proposed symmetric multilevel inverter. The MLI output voltage waveform without control technique for a 21-level proposed symmetric multilevel inverter is given below. *Figure 3* shows the output voltage waveform and THD without any control technique implemented.

Table 2. Comparison of parameters between Cascaded Symmetric and Proposed Symmetric

Inverter configuration Parameters	Cascaded symmetric H-Bridge	Proposed Symmetric Inverter
DC Sources	N	N
Voltage Level	2N + 1	2N + 1
$V_{o\,max}$	NV_{dc}	NV_{dc}
Main switching Devices	4N	N+4

Tables 2 highlight the comparison study between the usual cascaded architecture in symmetric as well as the proposed topology.

5. HARMONIC ELIMINATION

The ratio of the sum of the power of individual harmonic components to the power of fundamental harmonic components is known as total harmonic distortion. To improve the suggested inverter's performance, the recommended symmetric topology discussed in the previous chapter is used as the optimized topology, and the elimination of selective harmonic pulse width modulation (SHE-PWM) approach is used. The basic purpose of SHE-PWM is to remove specified harmonic order from the intended output voltage waveform.

Harmonic elimination is treated as an optimization problem that may be solved using a variety of evolutionary techniques [9-13] such as Genetic algorithms (GA), Particle swarm optimization (PSO), and Teaching-Learning based optimization (TLBO). But still, we authors find scope for improvement in the power quality. Hence recently developed soft computing optimization algorithms like Whale Optimization algorithm (WO), and Black Widow algorithm (BWA) were attempted to solve this problem. Simulation of proposed symmetric topology with optimum switching angle derived from Whale Optimization algorithm (WO) and Black Widow Algorithm(BWA) is carried out by using MATLAB – SIMULINK software.

6. BLACK WIDOW OPTIMIZATION ALGORITHM

The Black Widow spider is a poisonous spider that exists in Western Canada to Southern Mexico. A chemical called potent neurotoxin active is present in the venom of female black widow which is the most dangerous poison for humans as it can even lead to death even by one bite. The black widow optimization algorithm was designed based on the mating behaviors of the spider. The life cycle of the Blackwidow spider comprises three stages namely

1. Matting process of black widow spider,

2. Reproduction Style and Cannibalism,

3. Sibling Cannibalism. So here, each spider represents a solution in the initial population. In the process of cannibalism, the female spider will eat the male spider whereas in sibling cannibalism strong spiders will eat the weaker spiders. This process will be carried out followed by mutation, convergence, and parameter settings thus completing the optimization. *Figure 4* shows the pictorial description of the algorithm.

The solution to the harmonic reduction problem for 21 level inverter is ten switching angles α1, α2, α3, α4, α5, α6, α7, α8, α9 and α10.

Minimize the THD value in the fitness function of S variables α1, α2, α3,….. αn.

$$THD\_MLI = \frac{1}{V_{01}}\left(\sum_{n=2,3}^{DC} V_{on}^2\right)^{1/2}$$

Subject to $0 \le \alpha_1 < \alpha_2 < \ldots \alpha_n \le \frac{\pi}{2}$(bound) and magnitude of output voltage should satisfy the required output voltage. Von is the output voltage of an Nlevel(m) suggested symmetric multilevel inverter.
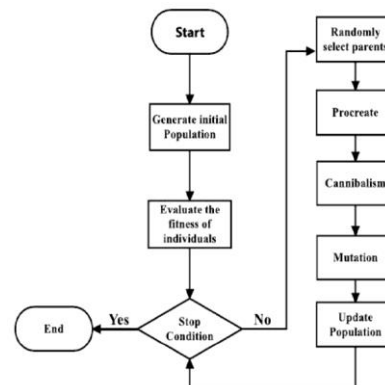

Figure 4. Flow chart for Black Widow Algorithm

$$V_a(\omega t)\frac{4V_{dc}}{\pi}\sum_{n=1,3,5}[\cos n\,\theta_1 + \cos n\,\theta_2 + \cos n\,\theta_3 + \ldots \cos n\,\theta_N]\frac{\sin n\,\omega t}{n}$$

The ratio of the sum of the power of individual harmonic components to the power of fundamental harmonic.

7. SIMULATION RESULT

The Black Widow Algorithm (BWA) was developed with the help of the MATLAB .m file. The recommended 21-level symmetric multilevel inverter's performance is assessed using the BWO methodology. During the simulation investigations, distinct DC sources were used. MATLAB –SIMULINK software is used to model the suggested symmetric 21 level MLI using these ideal switching angles. Figures 5 demonstrate the output voltage waveform and FFT analysis of the recommended multilevel inverter using the BWO approach. By doing FFT analysis, the THD is obtained with the value of 4.06% which is also less than 5% which is an effective output THD that to be obtained as a result of applying optimization techniques.

8. WHALE OPTIMIZATION ALGORITHM

Whales are considered the largest mammals in the world. There are many types of the whales like humpback, finback, blue whales, etc. These whales, according to Hof and Van Der Gucht, have specific cells called spindle cells that are responsible for their intelligence. Humpback whales (Megapteranovaeangliae), one of the largest whales, have a unique hunting style. The bubble net feeding method is the type of foraging technique. Whales can create distinctive bubbles or 9 shaped paths along a circle. This behavior is investigated using a tag sensor by GoldBogen et al. Upward spirals and down loops are two maneuvers. In upward spirals, the humpback whales jump 12 meters down around the prey and jump upward towards the ground. In the latter, coral loop, lob tail and capture loop are three stages. Some applications are neural network training, breast cancer diagnosis, economic dispatch, unit commitment problem solution, optimal power flow, etc. The mathematical model of WOA is divided into 3 types encircling

of prey, bubble-net attacking, and searching the prey. Pictorial description of the algorithm is presented in *figure 6*.
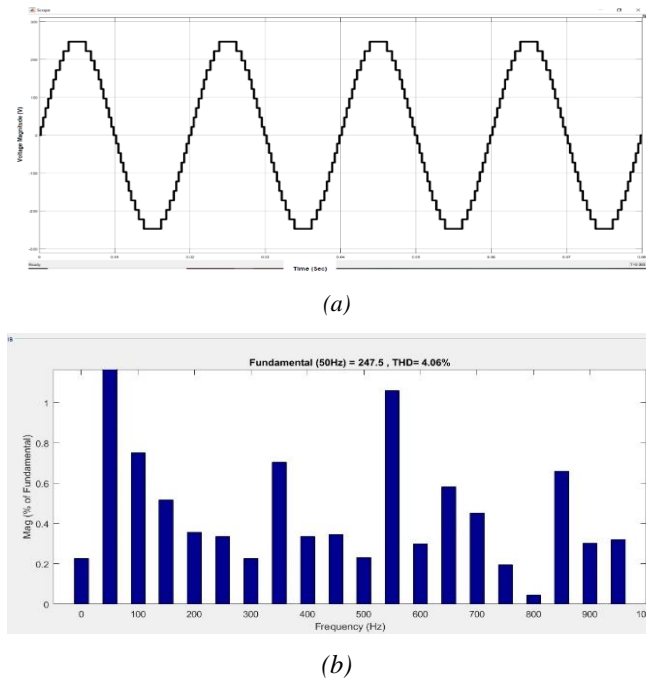

(a)

(b)

Figure 5: (a) Output voltage waveform (b) FFT Analysis using Black Widow Algorithm

9. SIMULATION OUTCOME

After optimization harmonics have been reduced to 3.96% which is suitable for all applications where AC input sources are given. The Output waveform and THD value is depicted in *figure 7*. Thus Whale Optimization algorithm gives better output than Black Widow Optimization Algorithm by giving less THD and more sinusoidal output waveform.

10. IMPLEMENTATION STRATEGY

The proposed symmetric multilevel inverter hardware as depicted in *figure 8* was built and tested in 21 level mode to ensure that the inverter's performance reliable with the THD minimization concept. The framework comprises of an FPGA controller, an isolation circuit, and a driver circuit. Each inverter switch has its own distinct driver circuit. An opto-coupler in the control circuit gives this isolation. The proposed soft computing based switching approach is used to create Pulse Width Modulation (PWM) control signals utilizing an FPGA controller.

These PWM signals drive the switching devices in the intended multilevel inverter circuit. The converter is made up of ten distinct 12 volt dc voltage sources and a single H-bridge. A R load with 1.2A current was used to establish the experimental configuration. MOSFET IRF840 switching devices and MOSFET driver IC TLP250 were used to build this prototype inverter. The FPGA controller generates the gating pulses (Xilinx ISE). Implementation is shown in *figure 9*. Hardware implementation output shown in *figure 10* favors the Whale Optimization Technique.
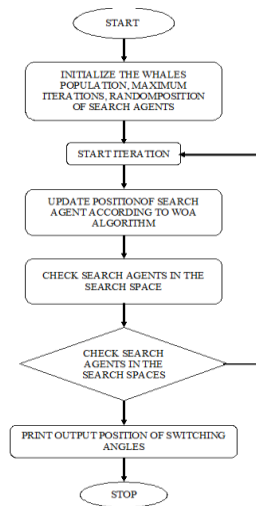

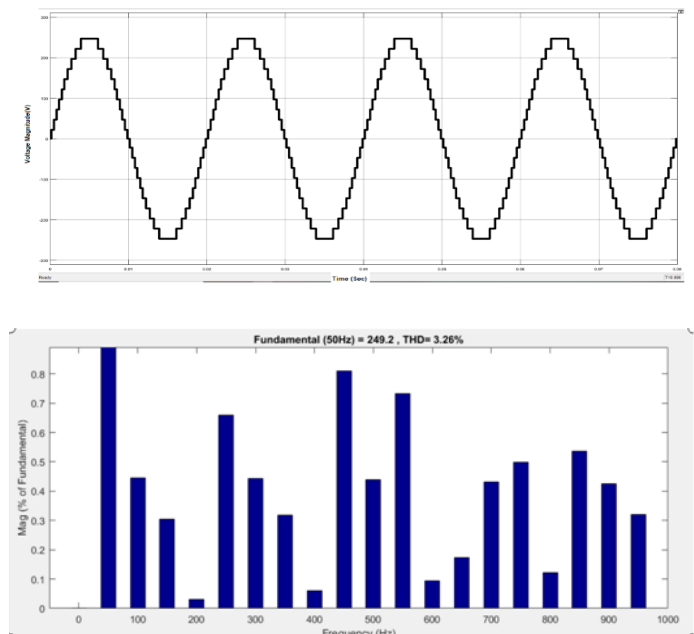**Figure 6:** Flow chart for Whale Optimization Algorithm

Figure 7: (a) Output AC waveform (b) FFT Analysis while using Whale Optimization Algorithm
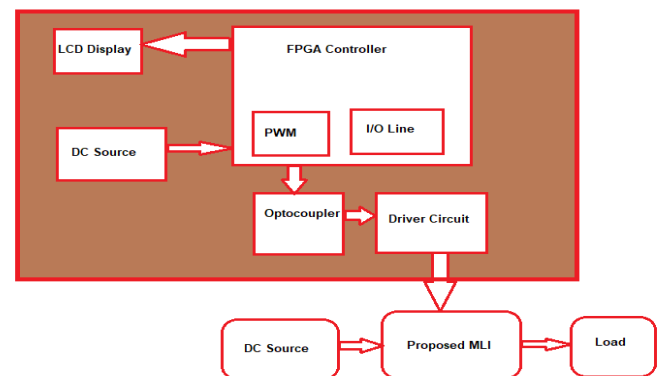

Figure 8: Proposed MLI control signal generation

11. CONCLUSION

This paper aims in developing a novel topology of a multilevel inverter whose power quality is improved using the power of the latest soft computing algorithms. The following are the key benefits of the suggested symmetric multilevel inverter:
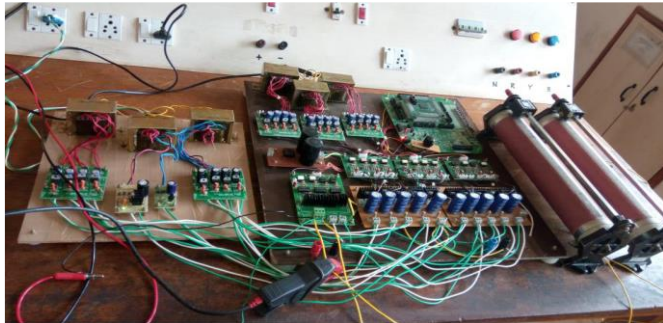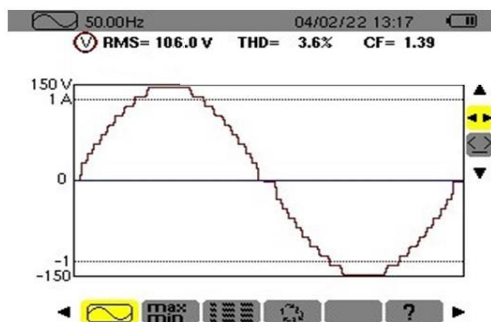

Figure 9: Experimental setup of proposed MLI

Figure 10: Output voltage waveform and THD of the proposed symmetric multilayer inverter using Whale Optimization Technique (experimental results)

Table 3. Comparison of percentage THD

Optimization Algorithms	WOA		BWOA	GA [12]	PSO [12]	TLBO [13]	Conventional
	Simulation	Hardware					
THD (%)	3.26	3.6	4.06	4.07	3.96	3.89	4.23

There are fewer components in the proposed method than diode-clamped, flying capacitors, and cascaded inverters to achieve the same amount of voltage levels. Because each level only requires one SDCS and one switch, and no additional clamping diodes or no voltage balancing capacitors, it is feasible to optimize circuit layout and packaging. The fabrication process will be easier, faster, and less expensive as a result of this. To improve the power quality, here, Whale Optimization Algorithm (WOA) and Black Widow Optimization Algorithm (BWOA) are tested. The obtained results are judged against the already published results obtained using other well-known soft computing algorithms. Table 3 provides such a comparison. From the table, it is inferred that Whale Optimization Algorithm acts as the best technique for THD minimization when compared to Black Widow Optimization Algorithm (BWOA) and other known algorithms.

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