

Performance Analysis of Various Fin Patterns of Hybrid Tunnel FET

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ABSTRACT- High speed and low power dissipation devices are expected from future generation technology of Nano-electronic devices. Tunnel field effect transistor (TFET) technology is unique to the prominent devices in low power applications. To minimize leakage currents, the tunnel switching technology of TFETs is superior to conventional MOS FETs. The gate coverage area of different fin shape hybrid tunnel field-effect transistors is more impacted on electric characteristics of drive current, leakage current and subthreshold slope. In this paper design various fin patterns of hybrid TFET devices and shows on better performance as compared with other fin shape hybrid tunnel FET. The TCAD simulation tool is used to determine the characteristics of different fin shape tunnel FET.

General Terms: MOSFET device, Nano technology, TFET, subthreshold slope.

Keywords: Tunnel FET, band to band tunneling, fin shape TFET, drive current, leakage current, subthreshold slope.

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1. INTRODUCTION

Due to rapid advancements in nanotechnology, device structures are shrinking beyond their limitations, resulting in inadequate gate control over the channel at typical room temperature (i.e., 300 K), and a progressive rise in short channel effects. The sub-threshold slope (SS) of conventional MOSFET device is bound to be greater than 60mV/decade because of the thermal diffusion mechanism.

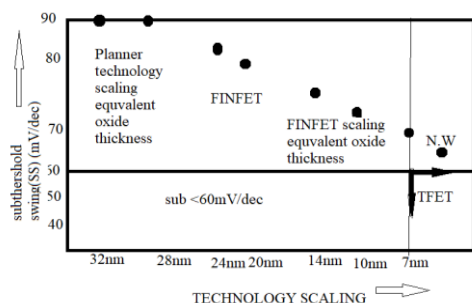


Figure 1: The relationship between Nano-scale device and sub-threshold swing

One of the most well-known solutions is the use of TFET [1]. The band-to-band tunneling (BTBT) [2] mechanism is used in Tunnel FET to overcome the physical limitations of SS value in MOSFET. Figure 1 shows the Nano-scale devices trend. At ambient temperature, SS in TFETs may be reduced to below 60mV/decade [3], indicating that important technical barriers have been overcome and that there is less off current.

2. LITERATURE SURVEY

In simple TFETs, source and drain terminals are doped with opposites of each other. As shown in figure 2(a), the TFET is a reversed biased P-I-N diode [4] with gate-varying tunneling probabilities. In this case, source carriers are injected via the BTBT mechanism. The standard TFET device features a p-type source and n-type drain and also works to different gate biases.

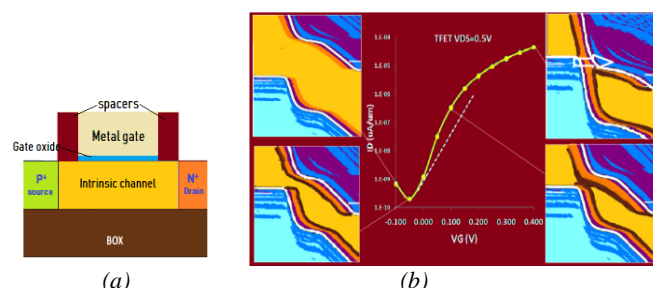


Figure 2: (a) Schematic diagram (b) Bands vary at different switching conditions of TFET

The extremely doped with p+ region near the source, moderately doped n-type channel and also extremely doped n-type drain. In General, TFET involves a number of parameters like as I_{GEN} , I_{BTBT} and I_s . ' I_{GEN} ' is a generation current in reverse-biased voltage that is reliant on the formation of holes

and electrons at the depletion regions. Similarly, ' I_{BTBT} ' is a BTB tunneling current that relies on tunneling of this carrier from the occupied band to the empty band of the destination. ' I_s ' really diffusion based reverse saturation current. Figure 2 (b) shows, band diagram of TFET.

The reducing supply voltage in nano electronic circuits is a viable technique to reduce power dissipation. However, inside MOSFETs [5], the basic lower limit of SS is a key impediment to other expanding the operation voltage without degrading the ON/OFF ratio in contemporary IC's.

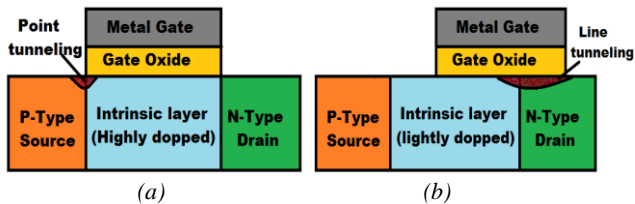


Figure 3: Based on gate alignment in TFET (a) point tunneling (b) Line tunneling

Nano device and Nanotechnology [6] unveiled innumerable devices with tremendous research. TFET is one of the capable devices for the SCEs [7] which results due to the continuous device scaling in traditional transistors. TFET unique construction and working principles keep it another side to the conventional devices [8]. The essential building of Tunnel FET has P-I-N construction.

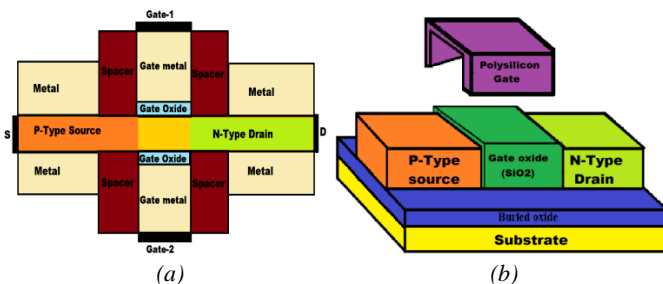


Figure 4: Schematic diagram of (a) Double gate tunnel FET (b) Tri gate tunnel FET

The different tunneling mechanism based on gate alignment described by Matthias Schmidt et al., figure 3(a) shown the low charge carrier BTBT generation rate occur in less tunneling area [9] of the source-channel junction is called "point tunneling". Figure 3(b) shown in this device the gate is overlapping the source, that effects higher charge carriers BTBT generation rate occurs in large tunneling area [10] of the gate overlap source-channel junction is called "line tunneling". Based number of gates are used they classified double and tri gate TFET's are shown in figure 4 (a) and 4(b).

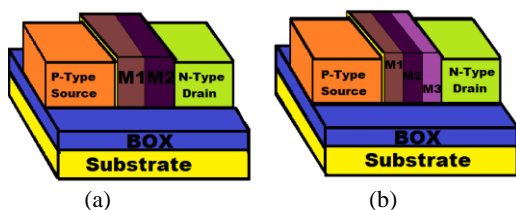


Figure 5: Based on number of metals used in fin gate TFET (a) Two metal gate (b) Three metal gate

Sneh Saurabhet al., [11] describe strained double gate TFET (SDGTFET). Single-layer strained-silicon-on-insulator (SSOI) technology is used in the design consider parameter. The on-current strengthen by in the order of two magnitudes for a Ge mole fraction of 0.5 and also meet the ITRS necessities. Based numbers of metals are used in the gate it classified double and triple metal gate TFET's are shown in figure 5 (a) and 5(b). Jang Hyun Kim et al. [12] suggested TFET comes with a SiGe channel, a fin arrangement along with a raised drain to boost its electrical operation. It reveals ON-state present (I_{ON}) is amplified by 24 times greater than that of Si control set and also by 6 times additionally of SiGe management team. The ambipolar current (I_{AMB}) can be diminished by up to 900 times compared with the SiGe control group.

Kaishen Ou et al. [13] demonstrated structure for p-type Ge-Fin TFET with a wrapped around epitaxial layer. The design consideration parameters are Fin width, gate source overlap length, drain doping, and equivalent oxide (HfO_2) thickness (EOT). The limitations are too large gate-source overlap can compromise drive current due to increased series resistance in the larger undoped epitaxial layer beneath the gate. Low temperature ($330 \sim 400^\circ C$) growth of Ge is preferred. The influence of the height (H_{fin}) and width (W_{fin}) of a Si fin on the Epitaxial layer TFETs [14]. Because the EL is formed on the top and sidewall of a fin, the vertical BTBT cross-sectional area is proportional to H_{fin} . Therefore, the increase of H_{fin} leads to Ion boosting in the case of EL TFETs.

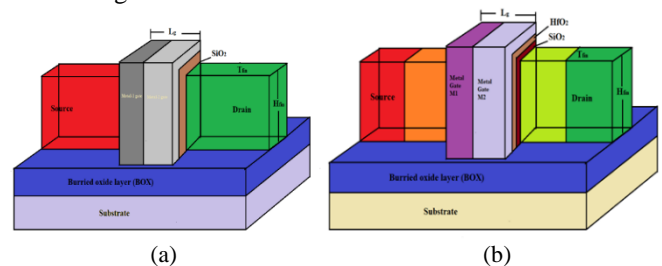


Figure 6: Based on models' double metal Fin TFET (a) Single gate oxide (b) Dual gate oxide

Priyanka Saha et al.,[15] explained that Dual Metallic Tri-gate TFET (DM TG-TFET) will be It's been proven to research tunneling barrier tuning from the station area by double fabric gate electrode with different values of work functions of M1 and M2 that the BTB carrier tunneling at the origin into the station region enriches the BTB provider tunneling out of The origin to the station area with significant advancement in I_{on}/I_{off} that the ratio will be 10^2 , the low V_{th} is 0.8V, steeper DMTG Silicon On Nothing (SON) TFET using SiO_2/HfO_2 piled gate oxide to obtain the double benefits of gate material and dielectric engineering methods [16]is shown in figure 6 (a) and 6(b).

3. PROPOSED DEVICE DESIGN STRUCTURE

Fin shape tunnel FET has better electrostatic control of gate over the entire semiconductor channel, which enhances conduction current and decrease leakage current. Figure 7

shows the proposed device structures of different fin pattern tunnel FETs.

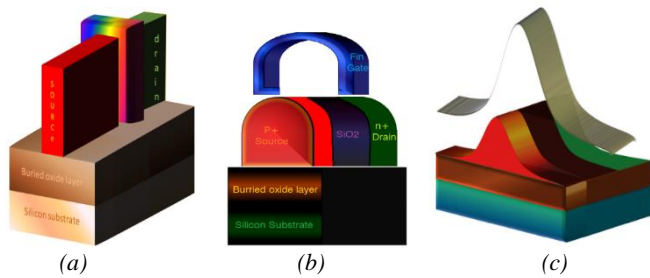


Figure 7: Based on Fin shapes TFETs are (a) Rectangular (b) Trapezoidal (c) Triangular

Fin shape tunnel FET has better electrostatic control of gate over the entire semiconductor channel, which enhances conduction current and decrease leakage current. *Figure 7* shows the proposed device structures of different fin pattern tunnel FETs. In rectangular cross-section fin shape device has on –current is high but line edge roughness and random doping fluctuation are affected on improved leakage current. The triangular fin shape tunnel FET offers low leakage current and the conduction current is slightly less as compared with the other two fin shape TFET's. Because the gate coverage area of the channel is less as compared to other fin shapes TFET's. The trapezoidal fin shape TFET has better performance as compared with triangular fin and rectangular fin pattern tunnel field transistor's because of tunneling current is high and soft corners are rectifying the problem of leakage current. I_{on}/I_{off} ratio is high in trapezoidal fin shape TFET.

4. SIMULATION RESULTS AND DISCUSSION

In this section, we have investigated an overall performance of proposed devices of different fin pattern hybrid tunnel FET based on Centaurs TCAD simulation results. The triangular, rectangular and Trapezoidal fin pattern hybrid TFETs are designed using the following specifications: Thickness of buried oxide (t_{box})=50nm; channel length (L_{ch})= 20nm; gate oxide thickness (t_{ox}) =1nm; doping concentration of source, drain and channel regions are $N_D=10^{20} \text{ cm}^{-3}$, $N_A=10^{19} \text{ cm}^{-3}$ and $N_A=10^{17} \text{ cm}^{-3}$; Height of the fin (H_{fin})=20nm and width of fin (W_{fin}) varied based fin pattern i.e., Triangular fin width top and bottom are 0.001nm and 15nm; Rectangular fin width top and bottom is 15nm and Trapezoidal fin width top and bottom are 15nm and 10nm respectively.

Based on specification 3D view of complex fin patterns which represents three different (Triangular, rectangular and Trapezoidal) fin shape hybrid tunnel FET models were designed using a sentaurus TCAD simulation tool is shown in *figure 8(a), 8(b) and 8(c)*. Kane's, Auger and SRH recombination, and band gap narrowing prototype were supported in this simulator.

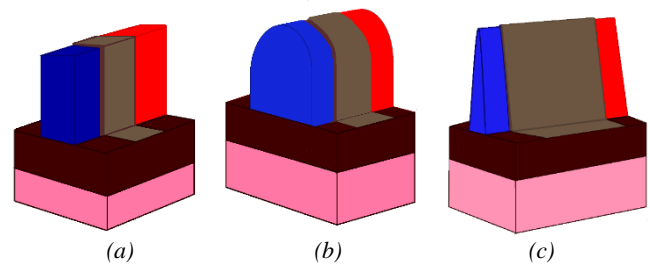


Figure 8: Simulation results of Fin shapes TFETs are (a) Rectangular (b) Trapezoidal (c) Triangular

Figure 9 exhibits the energy band diagram of soft corner different fin shapes hybrid tunnel FETs in the off-state, in which there is no tunnel path exists in between source and channel. When low drain bias causes the energy band shift upwards at drain end. The leakage current does not appear in between source-channel junction of tunnel path. The gate pulls up the channel's energy band in the on-state, creating an overlap appear between conduction band of source and valence band of channel. This path can be tunneled through by carriers and reached drain end. At result high on-state current, average steeper slope also acquired are an incredibly low off-state current and an excellent I_{on}/I_{off} .

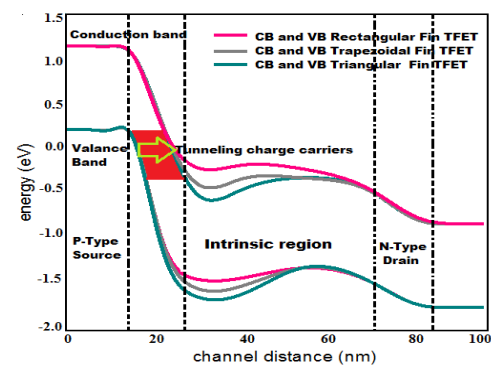


Figure 9: Energy bands variations in different fin pattern tunnel FET's

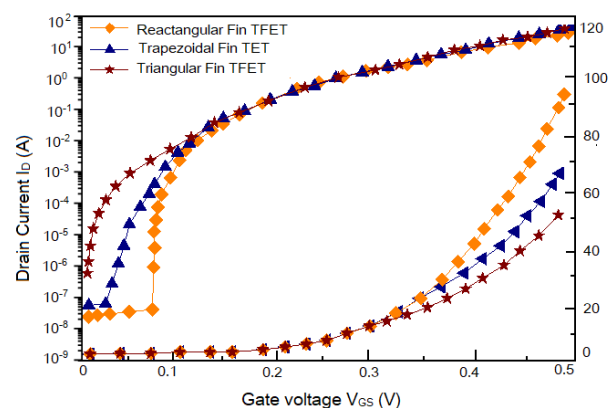


Figure 10: $I_d - V_{GS}$ characteristics of different (Rectangular, Trapezoidal and triangular) Fin shape TFET

The major impact on cross section area of the fin pattern on I_D - V_{GS} characteristics is shown in *figure 10*. Tunneling area of the source and the channel region, line-edge roughness (LER) and corner effect result in and develop a better performance in terms of the differences between SS, I_{amb} , and I_{ON} current as compared with the different fin patterns of the TFET devices. The more trapezoidal cross section area of fin TFET has better on-state current, less ambipolar current and subthreshold slope. In rectangular fin shape has high drive current but, raises the ambipolar current because of corner effects. As compared with other fin pattern TFETs, the triangular fin TFET has lower on-state and ambipolar currents.

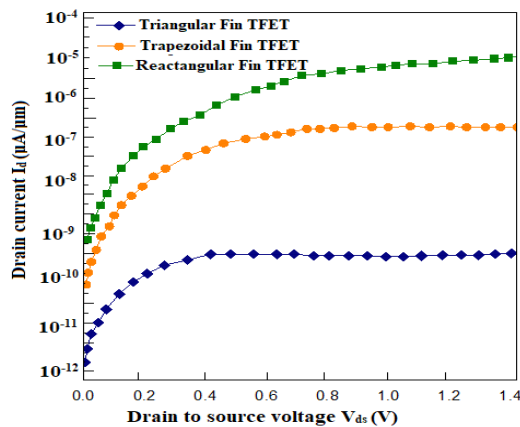


Figure 11: $I_d - V_{ds}$ characteristics of different (Rectangular, Trapezoidal and triangular) Fin shape TFET

The output characteristics for different Rectangular, Trapezoidal and triangular Fin TFET at $V_{gs}=0.4v$ is shown in *figure 11*. A higher drain current will result in a higher gate to source voltage. More electrons enter the drain region when the voltage gradient increases, and the barrier height decreases. Results from TCAD simulation show that Trapezoidal Fin TFET achieves better performance than triangular and rectangular Fin TFET. *Figure 12* exhibits that SS and I_d are different characteristics of depending on Fin pattern TFET. As a result, considerable, improve of subthreshold swing (SS) correlation with triangular, Trapezoidal and Rectangular Fin TFET.

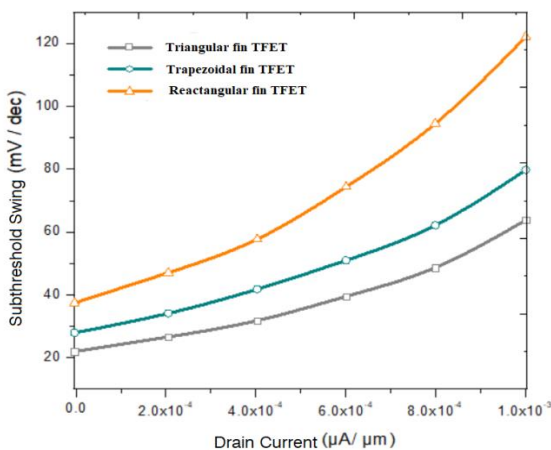


Figure 12: Comparison of SS- I_d characteristics of different Fin pattern TFET

5. CONCLUSION

This paper proposes various fin patterns of hybrid TFET. In this, analysis of various fin patterns are influences on the I_{ON} parameter of 20nm Rectangular, Trapezoidal, and Triangular Fin TFETs is shown in *table 1*. In this the rectangular fin shape has the largest top and bottom fin widths of 15nm, it has the highest I_{ON} current i.e., $18 \mu A/\mu m$ as compared with remaining two fin shape designs. Triangular fins, on the other hand, have the lowest I_{OFF} current i.e., $10^{-5} \mu A/\mu m$ because of reduce corner effects of the fin. In trapezoidal fin shape TFET has better SS 18.2mV/decade as compare with other two fin patterns of device.

Table 1: Parameters comparison in Triangular, trapezoidal and Rectangular Fin TFET

| Device Parameters (units) | | | | |
|---------------------------|-------------|-----------------------|------------------------|------------------|
| Model | SS (mV/dec) | $I_{ON}(\mu A/\mu m)$ | $I_{OFF}(\mu A/\mu m)$ | I_{ON}/I_{OFF} |
| Triangular Fin TFET | 32 | 14 | 10^{-5} | 10^5 |
| Trapezoidal Fin TFET | 18.2 | 16 | 10^{-15} | 10^9 |
| Rectangular Fin TFET | 25 | 18 | 10^{-8} | 10^{10} |

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