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Non-Volatile Logic Design Considerations for Energy Efficient Tolerant Variation

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ABSTRACT- Systems design for the non-volatile application must work on less energy or power. The spin-transfer torque-magnetic tunnel junction (STT-MTJ) devices added to the flip-flops which are regarded as non-volatile storage devices. Those are addresses to save the energy of that system stated by the nonvolatile logic. The changes during the production of STT-MTJ and CMOS transistors decrease the yield, which leads to overdesign as well as more energy consumption. The total processes of driver circuitry design for the tradeoffs for backup and restore performance. A new method called the novel method is introduced for flawless energy drivers for given results. The design for the backup time determination and to reduce the energy wastage are mentioned. To get an efficient output of 98% this approach needs to dissipate 5 times more energy than initially required. This method can dissipate the energy up to 26%. It also contains the nonvolatile flip-flop (NVFF) which has energy consumption more when it is used in the functional blocks.

Keywords: Nonvolatile logic, NVFF, STT-MTJ, Nonvolatile test, Scan mechanism.

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1. INTRODUCTION

A microelectronic circuit consumes the power from an ambient power source like solar. Thermoelectric, airflow, vibration, and piezoelectric are projected to become very important to grow or develop quickly in the research area of the Internet of Things (IoT). Even though the power density varies depending on mW to uW. These variations are distributed energy time. It is the irregular character of energy delivery by advanced encryption standard (AES). These pose a difficult dispute for the micro-electronic system [1-5]. But these are commonly made for operation in the continuous path. It is critical for predicting quickly an imminent power disturbance and reduction the non-volatile storage for the entire population. But it can be easy for the simplest devices. The CMOS well-matched non-volatile memory (NVM) skills from the precedent decade are used in the method for the architecture of novel circuits for energy-efficient holdup and retrieval [6-9].

NVM for backup can be used in any one of the two ways. One is NVMA (Non-volatile Memory Array) which can register all the data serially before the power failure and can be retrieved serially. The other way is to have each register be NVFF in the standard method. It has been added the capacity to save its current state before a power failure in a local non-volatile mechanism. The power leakage of CMOS devices becoming a major problem by the advancement of technology [10-12]. Therefore, NV magnetic memories by implementing Spintronic technologies are becoming more and more popular. This popularity occurs because of many features for example high survival soaring density, soft fault protection, CMOS compatibility, *etc.* [13-15]. To reduce the power loss by NVM architectures, a new concept called a non-volatile processor (NVP) is introduced. It is a set of NVFF which are used to restore the regular contents. NVP can back up the information in every NVFF in parallel so it has the capability for reduction of sleep and wake-up time into nanoseconds. Hence NVP is more useful in every harvesting system and management of power. Some of the ways to reduce the leakage power are clock and power gates, transistor stacking, adaptive body biasing, etc. [5, 16, 17].

2. RELATED WORK

A chip was developed in 2010, based on Fe-RAM to overcome difficulties of power reduction techniques in SRAM. An NVFF that contains Fe-RAM and the circuits for power gates is used as configuration memory [6]. The NVFF automatically transfers data between a flip flop and Fe-RAM when the power is turned on or off. The hibernation time is very less i.e., employs a style routing architecture [3, 7]. A fabricated NVP is introduced based on a ferroelectric flip-flop. These are used for the maintenance of the system state without any power supply [13]. During power failure for automatic backup a voltage detector system is designed. This Ferroelectric NVP can operate even under power failure. For backup, it takes very little time up to 7µs, and for restoration 3µs. Power consumption during this backup is also very less up to nW [4, 8].

In 2014, a drawback was found by STT-MRAM. STT-MRAM is shown potential memory. It can become the worldwide memory technology because it has many advantages such as high density, non-volatile, scalability and high endurance, *etc.*

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But the major disadvantage, it is read disturb. Read disturb means a bit flip-flop occurs while the read operation is going on because the write and read operations are in the identical path [9, 10]. As interpret to write down existing ratio is decreasing this major issue is growing with the technology. For this drawback, they proposed a circuit that detects the read disturb fault along with a machine that tests its behavior [12]. The read operation always flips from the configuration in its accomplishment. Another circuit called conditional circuit is also used to make active the detector route only for the AP pattern. Finally, this circuit can detect the real concern with low power and area overhead [1, 11].

An NV logic-based 32-Bits microcontroller SOC is introduced which can back up its processing state with zero leakage in the sleep model within very less it can be restored *i.e.*, < 400 ns. This SOC would help to enable systems like energy scavenging, wireless Microsystems [6, 14]. In 2015, a detailed description is given on the threshold logic gate (TLG). Threshold Logic gates can reduce the complexity by the absorption of Boolean logic. These TLG-1, ETLG-1 are more noise resilient and faster in comparison with SAFF and D-MS. Multi-input TLG's are low power consumption and higher performance when compared to CMOS counterparts [7, 15]. An NVFF with zero leakage power is introduced based on a ferroelectric flip flop. The flip flop stores data in its resistive memory when the power is off and restore when the power is on. The technology used in resistive memory is Programmable Metallization Cell (PMC). This model is used to estimate the energy consumption and reliability of reading operations in any regimes [5, 16].

Another drawback for STT-MRAM is founded *i.e.*, write latency and high write power. It has basically occurred for two reasons, one is bit-cell implementation is asymmetric. This means one write path is slower than another one. The second one is stochastic switch performance for fragment cell provides a manager to reach the particular write error rate (WER). To overcome this drawback there is a stationary and active route level technique. Which, are used to decrease the write latency [16]. The static method means by increasing the write current for slow writes then the write asymmetry gets reduces. The Dynamic technique is the increase in current write dynamically in stair sensible to reduce the unconstructive contact for the stochastic switch performance to reach the write margin. Thus, the dynamical technique reduces the overall write latency to upto71% by holding the same WER [2, 5].

3. LOGIC DESIGN CONSIDERATION

A backup driver is one of the non-volatile devices which is a common component to store and restore the data. By knowing the brief description of STT-MTJ, we can explain the backup driver design and its optimization shown in *figure 1*.

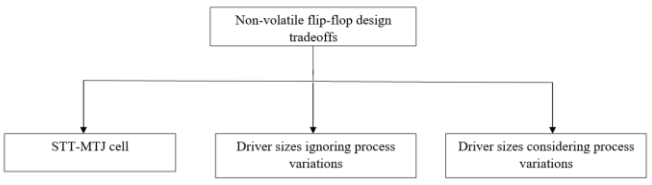

Figure 1: Logic Design considerations method

STT-MTJ has two ferromagnetic layers alienated by a layer by usually MgO as shown in the *figure* above. MTJ resistance depends on the magnetic orientation of MTJ with parallel (P) and anti-parallel (AP) states. By monitoring the magnetic field, the switching can be operated. This method can be used to switch the state by allowing the lower current through MTJ [6]. Driver sizes ignoring process variations: In this method, the backup drive can be designed without considering the variations in the process (variation in length, width, thickness).

Driver sizes considering process variations: In this method, the driver backup can be designed by considering all the variations in the process such as a change in length, width, and oxide thickness.

3.1 Non-volatile Flip Flops with Scan

To get the higher yield there must be a higher energy expenditure. By boosting up the voltage we can reduce the backup energy. The various methods used to improve the efficiency of energy and with balancing the backup time in NVM are not used for NVFF. Therefore, the other method for high energy consumption is to improve the write margin with the increase of drive size along with backup time. By the procedure of E_{OPT} results, the backup time with high probability which gives y% of the cube will give successful output in the encouragement of '1' and '0'. Therefore, the conventional preference of backup time gives wasted energy foremost dice. Therefore, an adaptive method for determination of support time on a per chip origin. The NVFF with scan method is introduced which is allow for adjusting the backup time with minimization of energy shown in *figure 2*.

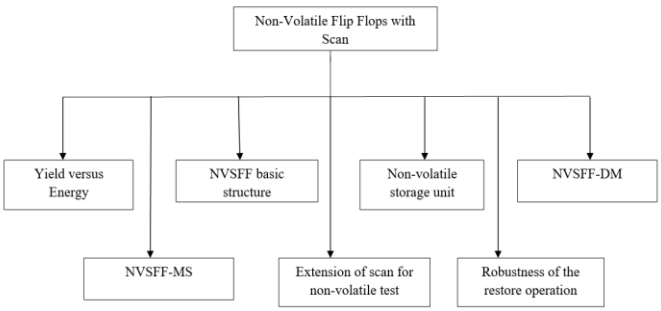

Figure 2: Structure design of non-volatile flip flops with scan

NVSFF basic structure: In this structure, there are 5 types of modes are there. They are normal mode, backup mode, restore mode, scan mode that doesn't use any battery power, backup, restore mode. The operational mode is mainly to perform non-volatile device tests and to backup time determination.

3.2 Non-volatile Storage Unit (NVSU)

The schematic diagram [8] of NVSU is as shown in the above *figure*. In this, there are two differential signals with inputs 'IN1' and 'IN2', and that results in their output as the degree of different outputs as N1 and N2. The SAV and RES help to manage the process mode. Therefore, the two are in NVSU in STT-MTJ devices. These are used one for STT data store up condition throughout support method and the other is STT-

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refused for the situation while in the restore mode. The schematic diagram of NVSU is revealed in *figure 3*.

3.3 Non-volatile Scan Differential Flip Flop (NVSFF-DM)

NVSFF-DM is termed as Non-volatile scan differential flip flop. When we observe in NVSU, it takes two degrees of different inputs in the backup mode and a couple of output in restore mode. When the flip flop interface with NVSU it results in NVSFF-DM. This NVSFF-DM contains the sense amplifiers with outputs as N1 and N2 which are the SR latch and the NVSU are connected. In this, there are two feedback loops used to delete the potential floating nodes which include the conventional Flip Flops is shown in flow chart *figure 4*.

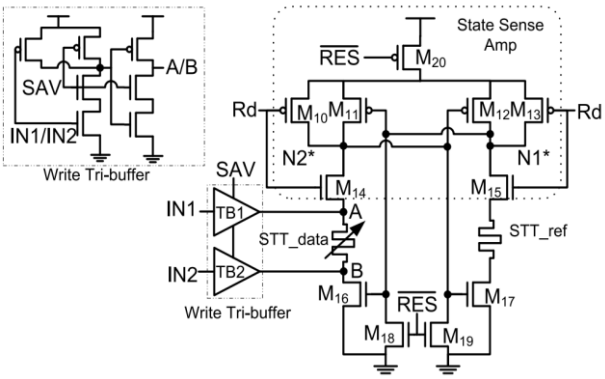

Figure 3: Schematic diagram of NVSU

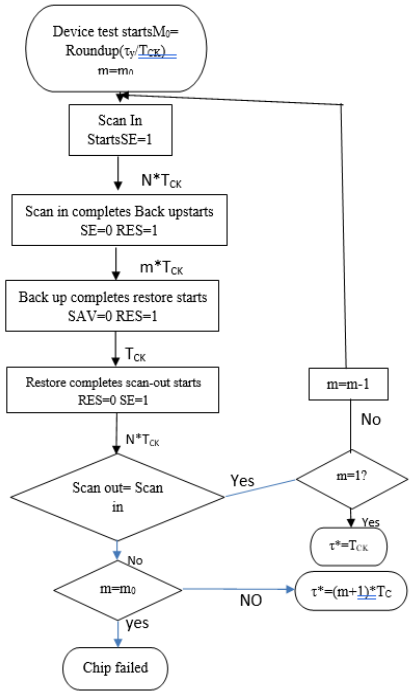

Figure 4: Scan of non-volatile materials

NVSFF-MS: NVSFF-MS is termed as a flip-flop of a Non-volatile master-slave. When NVSU contains the master-slave flipflop it results in NVSFF-MS. The scan mechanism in this circuit is the same as the D flip-flop mechanism. The NVSU needs to take the inputs from the slave key throughout the backing mode and need to send them back to the same node throughout the refurbish mode. During this the transmit gate must be turned off to obstruct the signal which results in commencing the master latch, it must be proficient to control the information when the clock goes to '0'. The conservative scan method is used to test the non-volatile procedure in NVFF. The following flowchart shows how the test is done to determine the authentic or chip detailed backup time that would do following the production. The main theme is power efficiency and the strength of note down or support procedure. To read the NVFF state the data must be sensitive and compare with the situation. Therefore, the technique used to get better toughness of NVFF read process would be done by appliance limitation optimization or by redundancy which would honestly applicable to the NVFF plan.

4. RESULT ANALYSIS AND DISCUSSION

In this section came to know about the evaluation for the proposed NVFF circuit and the result on a larger design incorporated with NVSFF. Generally, the circuit was considered using a design kit for the 40 nm GP procedure. Therefore, the power and interruption standards are obtained by use HSPICE.

Table1: MTJ-STT Parameters

Parameters	Value
MgO thickness(μ)	0.8nm,0.85nm
Free layer thickness	1.3nm
Area	40nm*40nm
Resistance area product	5Ω.μm^2
TMR at bias with Zero	140%
Variation of STD (σ)	2.3%, 5.6%, 11% [19]
Monte Carlo case	10020

4.1 STT-MTJ Cell

The t_{ox} is the majority important feature for energy utilization. To shorten the examination the t_{ox} perturbations are unspecified as Gaussian. 10000 Monte Carlo simulations are done to study the resistance variations in t_{ox} by mean $\mu_{tox}$and σ_{tox} of t_{ox} which are set to 0.8nm and 10%mean. If a particular control provides is used in NVSFF devise then the highest power fall across MTJ could not go beyond the V_{dd} (0.9V) in 40nm technology. The resistances can be calculated as:

$R_{H\ max}$=32.4 KΩ (1)

$R_{L\ max}$=11.43 KΩ (2)

Table 2: Standard deviation and mean of t_{ox} versus MTJ-STT resistances

μ_{tox} (nm)	σ_{tox} (%)	μ_{RH} (KΩ)	σ_{RH} (KΩ)	μ_{RL} (KΩ)	σ_{RL} (KΩ)
0.85	10%	9.59	6.91	3.84	2.76
	5%	8.23	2.74	3.29	1.09
	3%	7.96	1.57	3.18	0.62
0.8	10%	6.39	4.33	2.56	1.73
	5%	5.57	1.75	2.23	0.70
	3%	5.41	1.01	2.16	0.40

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Above *table 2* has shown the standard deviation and mean of resistance for two dissimilar mean value of 't_{ox}'. A small 't_{ox}' is favored for the '$3\sigma'$ of 'R_H' and 'R_L' are under the highest resistances by dictate to the power supply.

4.2. Performance estimation of planned NVSFFs

The below *table 3* has been shown the impediment and power interruption merchandise of two NVSFF and volatile flip flop designs for the master-slave scan. The system time for NVSFF is negative in contrast with NVSFF-MS. NVSFF-overall DM's delay is smaller than NVSFF-total MS's delay. The energy consumption is higher in NVSFF-DM than NVSFF-MS.

Table 3: Performance estimation of planned NVSFFs

Design Method	T_{C2Q} (ps)	T_{setup} (ps)	T_{total} (ps)	Energy (fJ/cyc)	EDP (fJ.ps)
MS-NVSFF	59.59	5.36	71.20	5.02	312.89
DM-NVSFF	46.99	-2.99	45.48	6.89	278.45
MS- SFF	40.18	21.69	56.08	2.47	141.23

5. CONCLUSION

The flip-flops that make up the majority of an NVL are the components that are in charge of conveying the current state of the system at any given moment. The flip-flops can be raised to a higher level by employing the storage space that is offered by NV. This is the way that is the most effective for restoring and backing up the state. The fundamental relevance of the process modification is the primary objective of the driving path, which is to put away the situation in an NV mechanism. This has primary significance for the efficiency of the energy and strength provided by the process modification. A new and more advanced technique has been established for power most favorable drawing for support driver and for equivalent support subject matter determination in order to satisfy the acquiesce restriction. Following the completion of the work, the length of time spent backing up the data on each chip's origin was altered in an original manner in order to cut down on the quantity of energy that was frittered away. This method cuts down on the amount of energy that is spent during the process of backing up data as compared to employing a single backup time for all of the chips. The concept of NVFFs was implemented into the scanning mechanism, which permits post-fabrication adjustments to be made to the amount of time the backup takes. As a consequence of this, this technique is applied in order to change the design of the ASIC to one that is nonvolatile.

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