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# Performance Evaluation of Low Power Hybrid Combinational Circuits using Memristor

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**ABSTRACT-** Recently, extending the use of memristor technology from memory to computing has received a lot of attention. Memristor-based logic design is a new concept that aims to make computing systems more efficient. Several logic families have emerged, each with its own set of characteristics. In this paper, CMOS-based hybrid memristor-based combinational circuits are designed. Many computational devices require combinational circuits. All of the proposed designs were analysed for power, latency, and transistor count. Cadence Virtuoso is used for simulation of circuits. In this study, we used the VTEAM model to describe the simulated memristor because it is easy to understand and gives accurate results.

**General Terms:** Digital Electronics, Combinational Circuits, Low Power Design
**Keywords:** Memristor, Combinational Logic, Decoder, Encoder, Multiplexer.

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## 1. INTRODUCTION

Nowadays, the VLSI industry is investing more in nanomaterial research, and nano-scale devices with good electrical properties are sought for logic block design. In this study, we present a unique nano-scale device termed a memristor [1]. The name stems from the memory resistor's capacity to remember previous resistance levels. It is very descriptive, but if you are unfamiliar with the concept of resistance, then that doesn't actually mean anything. The change in resistance in the memristor is caused by the behavior of the voltage and current directions [2, 3]. It refers to a wide range of resistance-changing devices. The disadvantages of memristor logic alone are endurance, reliability, and signal restoration. So here we propose a hybrid memristor [4] and CMOS logic in which the memristor's benefits can be added [5] with CMOS signal restoration and reliability.

This study presents a digital design logic block that includes a Decoder, Encoder and Multiplexer. There are a number of factors to be considered while designing complex circuits, for efficiency of the circuits. Portable multimedia applications such as mobile devices and PCs are a major factor in the need for low-power, rapid, and efficient digital logic design. In CMOS digital circuitry, there is both dynamic and static power dissipation. The switching component of power dissipation is primarily determined by the load capacitor, clock frequency, power activity factor, and short circuit current. Leakage current due to subthreshold effects and other factors causes static power dissipation. As explained in [6], there are numerous design methodologies and hierarchy levels. Voltage scaling and reduced voltage swing are a few of them; others are clock frequency reduction and switching capacitance reduction. All of these methods, however, have some flaws. Dynamic power dissipation is reduced when the supply voltage is dropped, but there is a delay penalty. When the threshold voltage is reduced, the latency is reduced, but there is an exponential rise in sub-threshold leakage current. In addition, numerous approaches for reducing switching capacitance have been proposed. The capacitance is strongly affected by the logic style chosen. There are many more techniques to reduce power dissipation, such as reducing the number of devices or scaling the transistor size. In terms of combinational circuits, there are mainly two design strategies. First is to take the core CMOS design concept and apply it to multiple technologies. The second design technique is based on CMOS VLSI logic design concepts, using two memristors with opposing orientations, complementary logic can be created. There are already many designs few of them are discussed here. The memristor is a three-terminal device in this case, and the design has a sneak path problem [7]. The encoder circuit is constructed using a NAND gate. It is built on domain-specific logic and incorporates two-step calculations in this design philosophy [8]. The use of core conceptual logic to develop combinational circuits at the gate level is another design method that can be employed. An extension of this concept is presented in the current study, in which the memristor is seen as a two-dimensional device and a new NAND gate design is detailed. This gate is used to construct combinational designs that take advantage of the benefits of

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hybrid CMOS-memristor technology. The proposed architecture conceptualizes one-stage computation logic, as opposed to stateful logic, which requires two stages of computation. The simulation is carried out in Cadence Virtuoso, and the outcomes are compared to CMOS designs. The following is how the paper is structured: *Section 2* provides an introduction to the nano-device memristor, which is a viable candidate for circuit design, as well as information on the designing and evaluation processes. *Section 3* describes the memristor gates that were used to produce the unique combinational circuits that were demonstrated. The results and performance evaluation are provided in *Section 4*. *Section 5* of the paper brings the paper to an end.

## 2. MEMRISTOR

A memristor is a non-linear circuit element that works on the basis of a nonlinear voltage-current relationship. Because this element's electrical resistance is proportional to its prior current, it's called a memristor [1]. Image processing, simulation of biological systems, and electrical and neural networks have all been successfully implemented using memristor-based circuits and systems [9]. Chua [1] defined the memristor as a previously undefined relationship between flux and charge q, providing a memristor's current–voltage (I–V) characteristic is shaped like a pinched hysteresis loop, as shown in *figure 1(a).*

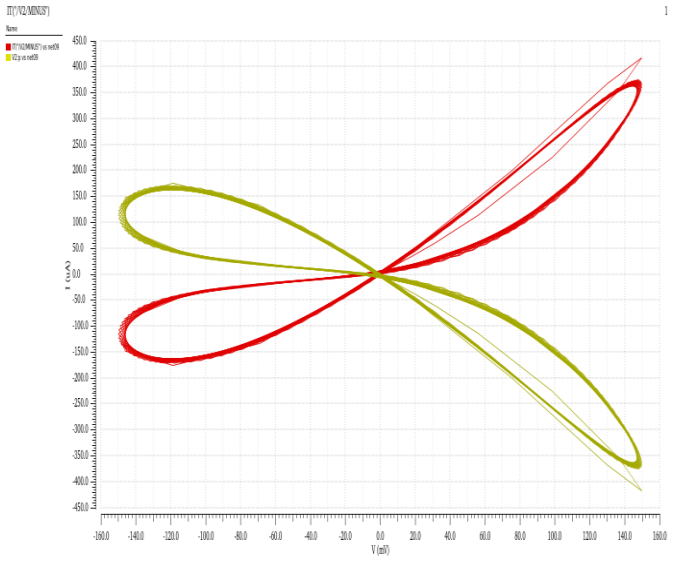

**Figure 1(a)**: Pinched Hysteresis Loop of Memristor

$$M(q) = \frac{d\emptyset}{dq} \qquad (1)$$

A memristor's current–voltage (I–V) characteristic is shaped like a pinched hysteresis loop, as shown in *figure 1(a)*. The hysteresis effect suggests that memristor resistance can be switched between two states: $R_{ON}$ and $R_{OFF}$. *Figure 1(b)* displays the memristor device's 3D structure, whereas Figure 1 (c) depicts the commonly used symbol for a single memristor. *Figure 1(d)* shows the physical model of a memristor, which consists of two layers of TiO2 sandwiched between platinum contacts [9], as described by HP Labs.

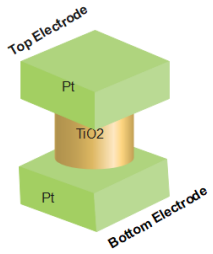


**Figure 1(b)**: Structure of Memristor

**Figure 1(c)**: Symbol of Memristor

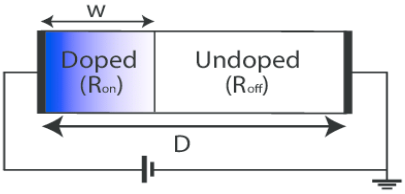


**Figure 1(d)**: Model of Memristor

One layer of TiO2 is doped with oxygen vacancies, while the other remains undoped. As a result, the doped region acts like a semiconductor, whereas the undoped part acts like an insulator. According to the amount and direction of the electric charges *q(t)* travelling across the memristor, the width of the doped area w(t) changes between zero and a memristor length of *D*. As a result, introducing a bias to the memristor causes current to flow, which affects the value of *w(t)*. As a result, the virtual boundary between the doped and undoped areas moves, which changes the memristor's total resistance, as shown in Equation (2) [10].

$$R_{MEM}(x) = R_{OFF}(1 - x) + R_{ON}(x) \quad (2)$$

Where x= w/D $\epsilon$[0,1] and $R_{ON}$ and $R_{OFF}$ are the limiting values of memristor resistance for w = D and w = 0, respectively. The drift velocity is the rate at which the boundary moves between the two ends, and it is represented by the state equation [2].

$$\frac{dx}{dt} = k.i(t) \ \ for\ k = \mu_v \frac{R_{ON}}{D^2} \qquad (3)$$

*Equation (3)* assumes that the drift velocity is constant, yielding a linear memristor drift model. The studies provided in [11,12] reveal that the implemented memristor's behaviour is non-linear. Several models have been developed in the literature to deal with the problem of nonlinearity. The authors suggested a non-linear dopant drift model as a relationship between the memristor's current and voltage (I-V) in [13]. To simulate the non-linearity, the drift velocity was expressed using a window function f(w) in [14]. In this study, the VTEAM model [15] was employed, and it was found to be superior to the other models tested. In the literature, three basic design styles for using memristors in logic design may be discovered. Only memristors are used for logic implementation in the first two design

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approaches, IMPLY [16,17] and MAGIC [18]. MRL [19,20] is the third design style, which uses a combination of CMOS and memristor components.

This section gives a quick view of these design styles. IMPLY Gates Material Implications: The logical state variables (0, 1) are represented by the memristor states ($R_{OFF}$, $R_{ON}$) in IMPLY. The gate is made up of the two memristors as well as the resistor. The input to the gate is represented by the initial memristances, while the output is written into the memristor after applying VCOND and VSET concurrently. As a result, the computation necessitates a series of steps. Several ways of executing combinational logic with IMPLY have been proposed in the literature [21,22]. To complete the goal computations, all feasible designs require multiple time steps. When compared to alternative logic implementation strategies, this fact results in a temporal delay. Logic using Memristors MAGIC is a logic design paradigm that uses only memristors and supports Boolean functions [23]. Unlike IMPLY, this logic family uses two memristors to store the input and output bits and a third memristor to store the output bit. The resistance recorded in the used memristors represents the logic state in the MAGIC implementation, where $R_{OFF}$ and $R_{ON}$ represent logic "0" and "1," respectively. In [24, 25] MAGIC NOR is employed as a foundation for performing logic computations inside the memory, hence increasing processing capabilities. To put it another way, each processing work is broken down into a series of MAGIC NOR operations that are carried out one after the other, employing memory cells as computation elements. Memristor Ratioed Logic (MRL) [26] is the third design style of memristor-based logic. The programmable resistance of memristors is used in the computation of the Boolean AND and OR operations in this typical hybrid CMOS–memristor logic architecture. In a similar fashion to CMOS-based devices, MRL uses voltage as the state variable, allowing the calculation to be completed in a single step. This criterion avoids the disadvantages of IMPLY logic devices' sequential process.

## 3. HYBRID MEMRISTOR COMBINATIONAL CIRCUITS

The new design aims to reduce the number of transistors necessary to build the circuit while preserving performance. As a viable technology for realizing these circuits, the memristor, a nanotechnology device compatible with ordinary CMOS technology, could be investigated as an option. In order to generate more than two states without the usage of additional hardware, memristors can be employed in combinational circuits [27], and this ability can be exploited to develop more efficient combinational circuits. Each of the combination circuits has a specific operation described by a set of Boolean logic that may be accomplished using gates and the connections between the gates. As a result of using memristor-based gates to build the combinational digital circuits outlined above, it has been discovered that the design is both faster and provides better performance than CMOS logic circuits. This is due to the fact that the designs do not make use of PMOS transistors and have a relatively low number of transistors. Due to the fact that the electron mobility is almost twice that of holes, the resistance of an n-channel device must be half that of an equal p-channel device to function properly. As a result, the level of complexity for n-channel devices is lower. A lower junction capacitance is achieved by shrinking the n-channel junction size to a smaller size. The variable resistance of the memristor is utilized to remove the PMOS transistor from the CMOS architecture [28]. As a result, the performance of this design paradigm is superior to that of MRL-based hybrid CMOS systems in every regard. Because of the lower dimension of the memristor and the low transistor count, the designs use less chip area and operate at higher speeds as a result. In addition to saving a significant amount of power due to the fact that a memristor does not conduct when no power is supplied and does not generate leakage current, the unique designs have other advantages over CMOS digital circuits.

### 3.1 Priority Encoder

The encoder outputs an x-bit binary that corresponds to the y-bit input signal code provided by the user. An encoder with a priority system is one where the input with the top priority supersedes over the other inputs while two or more inputs are provided at the same time. The output of the encoder reflects the binary equivalent of the ordinal number based on the most significant bit of input that was made available by the encoder (*Figure 2, Table 1*). The equation for the encoder can be represented in the following way.

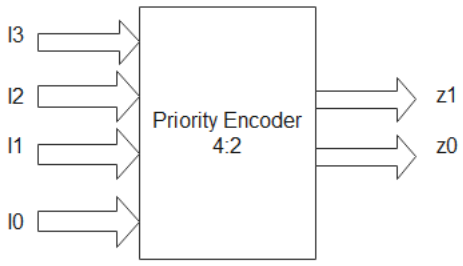


**Figure 2**: Block diagram of 4:2 Priority Encoder

$$Z1 = I2 + I3 \qquad (4)$$

$$Z0 = I3 + \acute{I}2\, I1 \qquad (5)$$

**Table 1. Truth Table of Priority Encoder**

| Input | | | | Output | |
|---|---|---|---|---|---|
| **I3** | **I2** | **I1** | **I0** | **Z1** | **Z0** |
| 1 | X | X | X | 1 | 1 |
| 0 | 1 | X | X | 1 | 0 |
| 0 | 0 | 1 | X | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 |

In accordance with the schematic in *figure 3*, the design is entirely implemented with memristors and NMOS transistors. The encoder's inputs are labelled I0, I1, I2, and I3, while its outputs are labelled Z0 and Z1, respectively. For the Boolean logic in (7) and (8), logic gates are employed to implement their meanings. Inputs I2 and I3 are applied to transistors 1 and 2, respectively, and input I1 is applied to the d-memristor. Input I1 is applied to the d-memristor. It is necessary to invert the output (I3 + I2) in order to obtain the result Z1, which is equivalent to (I3 + I2). In a similar manner, the output of Z0 is

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obtained. As can be observed, the transistors have been reduced to seven from the previous nine. Since the same logic is performed in CMOS logic style, the number of transistors is reduced to 16. This resulted in a more straightforward architecture when compared to the CMOS circuit.

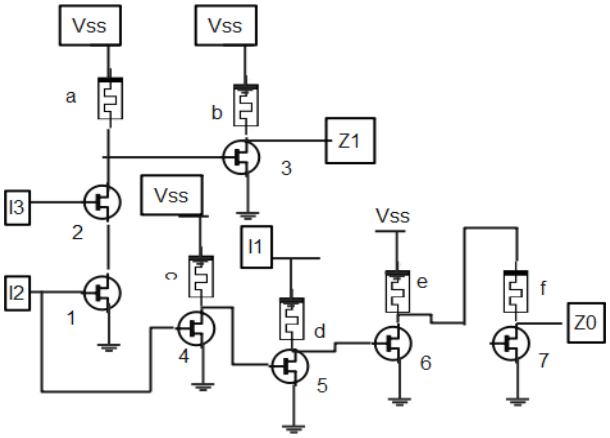


**Figure 3:** Proposed Design of hybrid memristor based priority Encoder

## 3.2 Decoder

A decoder converts binary data from x input lines to up to 2x distinct output lines [14]. It acts as a converter, changing the x-input into 2x different output lines. *Figure 4* shows the block diagram for it. The output expression can be written as using the *truth table 2* as a guide.

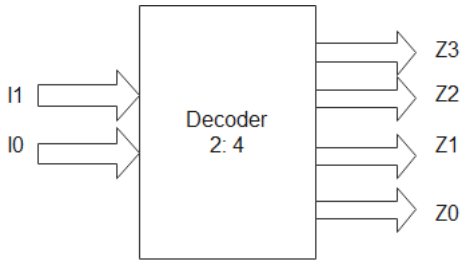


**Figure 4:** Proposed Design of hybrid memristor based priority Encoder

$$Z3 = I1I0 \quad (6)$$

$$Z2 = I1\acute{I}0 \quad (7)$$

$$Z1 = \acute{I}1I0 \quad (8)$$

$$Z0 = \acute{I}1\acute{I}0 \quad (9)$$

**Table 2. Truth Table of Decoder**

| Input | | Output | | | |
|---|---|---|---|---|---|
| **I1** | **I0** | **Z3** | **Z2** | **Z1** | **Z0** |
| 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 |

*Figure 5* displays the proposed design of the 2:4 Decoder, which was accomplished through the use of simple logic gate components. Before taking the Z3 output, the inputs I1 and I0 are first inverted. Z1 and Z0 are also achieved by circuit design in a similar way. The transistors have been reduced to just eight for this design. When using CMOS logic to make the same logic, twenty transistors are needed instead of ten.

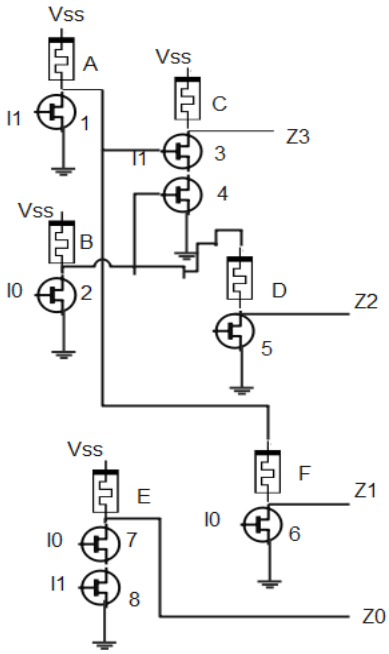


**Figure 5:** Proposed Design of hybrid memristor based Decoder

## 3.3 Multiplexer

In computing, a digital multiplex is a circuit that selects binary data or information from many input lines and transmits it to a single output line. The user is prevented from choosing the exact input line by a cluster of selection lines. 2X1 multiplexers are depicted in block diagram form in *figure 6*.

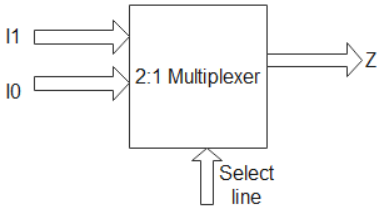


**Figure 6:** Block Diagram of 2:1 Multiplexer

When one of the two input AND gates' inputs is applied to I(0) or I(1), it is referred to as a 0 or 1. The selection lines choose (0) decode in order to select the exact input. When the value of the select line is zero, the value of the output line is I0. I1 will be used as the output if a select line contains only one value. Due to the fact that it selects one of several inputs and routes binary data to the input line, a Mux is also known as a Data Selector. It is composed of AND gates that are coupled to CMOS logic, which is followed by the author, and its waveform is observed. This device has two inputs and a single output. This

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led us to design and build what is shown in *Figures 6 and 7*: the necessary MUX.

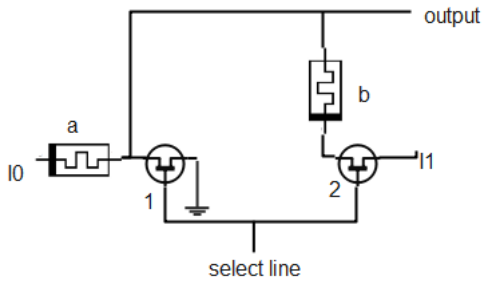


**Figure 7:** Proposed Design of hybrid memristor based multiplexer

Following this equation, 2X1 Mux can be defined as

$$Z = \acute{S}I0 + SI1 \qquad (10)$$

**Table 3. Truth Table of Multiplexer**

| Select Line | Output |
|---|---|
| 0 | I0 |
| 1 | I1 |

## 4. RESULTS

Cadence Virtuoso is used to simulate and analyse all of the proposed circuits. To simulate NMOS and PMOS, the parameters used are L = 1.8u, W = 28u, and L = 9u, W = 64u, respectively. $R_{ON}$ is 0.8 K in the memristor model [28], $R_{OFF}$ is 10,000 K, and $R_{init}$ is 8000 K in the memristor model [28]. All potential input combinations are tested and determined to be in agreement with the *truth table*. A comparison of all of the digital circuits under consideration is made using CMOS logic designs. Power dissipation, latency, and transistor count are some of the metrics utilized in the comparison of the two devices. Based on the simulation findings, the proposed approach is capable of achieving the intended circuitry with the least amount of power and the smallest number of transistors. As may be seen in Figure 8, the transient response of the encoder is significant. The encoder receives data from voltage nodes V(0), V (1), V (2), and V (3), which represent I0, I1, I2, and I3, respectively. The encoder outputs voltage nodes V (4) and V (5), which correspond to Z1 and Z0, respectively. When the input I3 is high, independent of I2 or I1, the outputs Z1 and Z0 are also high. This proves the encoder's truth table, which is shown in the simulation results. Using the *truth table*, the results can be double-checked for any alternative input values. Circuit delays of picoseconds are quite short compared to those of nanoseconds, which are created by the CMOS circuit.

In *figure 9*, the transient response of the decoder is significant there are two voltage nodes connected to I1 and I0 of the decoder, which are labelled V (1) and V (2). There are voltage nodes V (3, 4, 5, and 6) for each of the four outputs Z0, Z1, Z2 and Z3. I1 and I0 are applied sequentially, and the output truth table is checked. To make sure that the output X2 is always high, the circuit is tested by simulating and verifying every possible combination of the two inputs, namely I1 and I0. Figure 9 shows the transitory reaction.

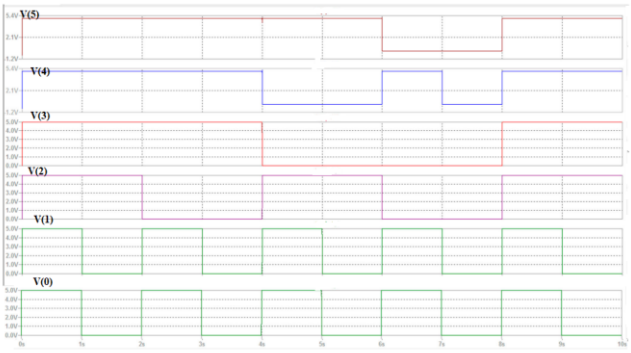


**Figure 8:** Transient response of Encoder Circuit

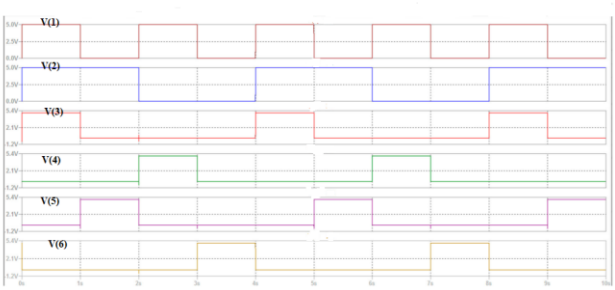


**Figure 9:** Transient response of Decoder Circuit

From the table, it's evident that memristor decoding consumes less power than CMOS decoding. Additionally, reducing the number of transistors to eight leads to a simpler design and a smaller chip (*Table 5*). When it comes to logic design, the CMOS-based approach is based on the mobility of holes and electrons, whereas the memristor approach is based on the motion of the boundary between the undoped and doped areas. This is further examined. When comparing electron and hole mobility with other components constant, the speed of border movement between the doped and un-doped regions increases by a factor of 104. Because of this, the switching time of memristive devices is significantly lower than that of CMOS systems. Nano-dimensional devices and increased mobility of the boundary between a doped and an undoped region mean that dopants can move with less energy, which in turn means that less power is required to demonstrate switching features [17]. The memristor also has virtually little leakage power consumption, reducing the overall power consumption and eliminating the need for any static power use. Scaling the length of a memristor can also increase the voltage required for it to switch. The bias voltage decreases considerably when the memristor device length approaches the nanoscale range, which minimizes power consumption. The above-mentioned facts are corroborated by the simulated outcomes.

**Table 4. Comparative Analysis of Proposed Encoder with CMOS Encoder**

| Parameters | CMOS based Encoder Design [29] | Proposed Design |
|---|---|---|
| **No. of Transistor** | 16 | 7T+6M = 13 |
| **Latency** | 5.027ns | 82.68ps |
| **Power Consumption** | 25.07uW | 8.86uW |

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**Table 5. Comparative Analysis of Proposed Decoder with CMOS Decoder**

| Parameters | CMOS based Decoder Design [29] | Proposed Design |
|---|---|---|
| **No. of Transistor** | 20 | 8T+6M = 14 |
| **Latency** | 3.98ns | 61.54ps |
| **Power Consumption** | 18.607 | 5.26uW |

# 5. CONCLUSION

Combinational circuit designs based on memristors are suggested in this paper. The results are then compared to the CMOS-based design using Cadence Virtuoso. According to the circuit design, latency and power consumption is reduced. A wide range of digital circuit designs can be benefited from these circuits. It's difficult to integrate memristor-based design with CMOS technology because of driver circuits for dynamic loads and varying operating voltages. Stacking memristors may cause problems with stealth mode. In order to remedy the problem, larger chip areas or materials with considerable non-linearity in the ON state can be employed instead, although this negates the goal of device scaling. Adding memristors on top of normal silicon transistors, which feed power into the system, could be a difficulty because it introduces extra masks and could have an adverse influence on outputs because of the chances of mistakes growing.

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