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Design and Speed Analysis of Low Power Single and Double Edge Triggered Flip Flop with Pulse Signal Feed-Through Scheme

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ABSTRACT- Flip flop is a fundamental electrical design component. Most electrical designs incorporate memory and their corresponding designs. The consumer electronics or end users need mobility and extended battery backup to enhance design performance. The focus on any parameter in the system is to maximize the performance of the design. Here the task is to reduce the energy use of flip flop. Due to the increased frequency clock delivered to the networks within the design, the edge or level triggered by a flip flop will contribute to power consumption. Due to the short circuit power consumption between ground and V_{dd}, the static design of the flip flop will increase power consumption. The flip flop is dynamically designed and implemented, leading to higher leakage power. Dynamic clock implementation helps for short-circuit power avoidance. It also provides greater download channel to the ground from output. The clocking system also demands more power. With the TSPC technology and output feedback, the suggested mechanic will increase the performance of the flip flop and establish the Pull-up network. The PMOS that contains the output node X value. The use of an additional NMOS transistor to draw the output value down to the ground, regardless of the input, so that the input runs on the discharge path that improves power, however the pulsed clock which has a smaller width than normal clock as well about 15% high.

Keywords: True Single-Phase Clock, Static conditional discharge Flip Flop, Low Power, Edge Triggered.

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1. INTRODUCTION

Flip-Flop is an electrical circuit that holds a logical state of 1 or many input signals for a clock pulse. Flip flops are frequently used in machine circuits for continuous clock intervals in elite sequences to get and keep information decent for a limited time for different circuits at intervals in a system to provide more methodical understanding. The flip-flop is a fundamental storage component that is utilized in numerous types of digital circuits. The use of Master-slave flip-flops is common in earlier designs. A pulse-triggered flip-flop can be used in its stead, which only needs a single latch and reduces chip size and overall power consumption. This decreases the circuit's degree of complexity. Implicit and explicit pulse triggered flip-flops are two types of pulse triggered devices. Flip-flop with a trigger, in an implicitly pulse-triggered flip-flop pulse generator, latch structure logic is built in. However, it has an issue with longer discharge paths. When a flip-flop is explicitly pulse-triggered, the pulse generation Design of the latch structure is distinct. Explicit kind uses more energy as a result of the independent pulse generator. The information keeps an excessively large number of flip flops on the market at each raising or lowering rim of the clock signal, so that it may be applied as input to combinational or sequential electronic equipment. Once technology scales down, total power dissipation can decrease and at identical time delay

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varies depends upon offer voltage, threshold voltage, ratio, compound thickness, load capacitance. CMOS devices have scaled downward sharply in every technology generation to realize higher integration density and performance. But with scaling technology, the download power has increased dramatically and is a major contributor to the entire IC power. A technique to build integrated circuits might be a complementary metal-oxide-semiconductor (CMOS).

In microprocessor systems, microcontrollers, static RAMs and various digital logic circuits CMOS technology is used. That double edge clocking can be used to save half of the power in the clock distribution network. Dynamic or switching power dissipation and leakage power depends on supply voltage. Since Dynamic power is proportional to the square of the supply voltage it is the highest power consumption among the three. Hence the major step to be taken is to reduce the dynamic power. By reducing the supply voltage dynamic power can be reduced. This may affect the speed of the circuit. Reduction in clock frequency is another alternative to reduce the dynamic power. By using Double edge clocking, clock frequency can be reduced. In this approach same data throughput can be achieved with half of the clock frequency as compared to SETFF. Single edge triggered flip flop takes many cycles to pass the data whereas dual edge triggered flip flop takes only few cycles to sample the data [1].

2. BACKGROUND

The advent of the high-class material inside the CMOS technique, as proclaimed by IBM and Intel at the 45 nanometer node and at the far side, resulted in a return of various metal gates. "CMOS" refers to each form of digital electronic device selected and so usually implements that electronic device on an integrated circuit (chips) [2] Electronic CMOS systems expend less power than resistive bulk logic families. Given the need for CMOS processes and variations, the vast bulk of current production of micro circuits is in processes with regard to CMOS.

2.1 Power Consumption in CMOS

The increased importance of mobile systems and, consequently, the energy consumption (and consequently thermal dissipation) in dense ULSI chips should be limited to quick, creative low-power advancements in recent years. The main factors for these advances are mobile appliances that require a low energy dissipation and a high output, such as laptops, [3] mobile devices and private digital assistants (PDAs). In most situations, the requirements for low power consumption should be fulfilled with equally tighter objectives of high chip density and high output. Thus, low power digital style.

The limited battery duration generally puts extremely stringent requirements on the general energy usage of the moving system. While new kinds of reversible battery such as binary nickel-metal composites (NiMH), with larger energy capacity than the traditional Nickel cadmium batteries, are being developed, there is no provision for a revolutionary rise in energy capacity in the near future. The energy density supplied by modern battery technologies (*i.e.* NiMH) refers to 30 DH/lb which remains low visible to growing applications of mobile systems. Reduce the dissipation of the integrated system.

Accordingly, a further key aspect of reliability added flavor is a reduction in energy usage. The methods used for square metering are large-scale, from the device technique level to the level of control with low energy consumption in digital systems. Device features (*e.g.* threshold voltage), geometry of the unit, and square interconnections assess key variables for reducing installation consumption. Measurements of circuit level, such as the right selection of circuit type designs, voltage swing reduction and continuance procedures may be accommodated at the level of the semiconductor back energy dissipation. [4] Incorporate specific the measurements of the circuit or transistor level that may be used to reduce the dissipation of digital integrated circuits. Numerous energy consumption sources are well discussed and techniques for reducing waste from the plant have been presented. System level problems such as pipeline replication and hardware (parallel processing), and the effect of such measures on power supply will be investigated.

2.2 Switching Power Dissipation

This component is an installation which is dissipated when a switching event, that is, after a logical transition is made to the power node voltage of CMOS gate [5]. The switching power is wasted in digital CMOS circuits, once energy is taken from the facility offering to power the output node. The power node voltage generally transfers from zero to VDD throughout this load-up portion and simply dissipates the energy derived from the factory offer as heat within the conductive PMOS transistors.

The power disconnection of the switch is also a linear operation of the clock frequency, although the general system performance would be significantly reduced only by lowering the frequency. Therefore, reducing the clock frequency would only be practical when different indications imply the overall outturn of the system. One of the most often utilized measurements for low power is the drop in power supply voltage [6]. While this is generally terribly successful, a great many important problems should be solved by themselves in order to avoid sacrificing system performance.

2.3 Short-Circuit Power Dissipation

The dissipation of the switch power discussed above is purely due to the energy needed to activate parasitic capacity in the circuit, and hence the switch power is independent of the increases and decreases in the input signals. If, however, each NMOS and indeed the PMOS transistors inside the circuit are operated by input voltage waveforms at finite times, each of the NMOSs can simultaneously lead for a short amount of your time throughout the switch, thus forming an immediate current path between the facility offer and thus the present part passing through the earth.,[7] The whole switch does not charge the capacity in the circuit and is consequently considered to as the current section of the short circuit If the

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output charge capability is small, and/or if the sign increases and decreases squarely.

2.4 Leakage Power Dissipation

The transistors used in NMOS and PMOS in a CMOS door often have non-zero reverse outputs and sub-thresholds. CMOS VLSI chip with a very large number of transistors contributes even when transistors are not subject to any switch event to the general power consumption [8].

3. DESIGNING WITH CMOS LOGIC

3.1Static CMOS Logic

Static logical circuits provide that basic CMOS designs flexibly incorporate static or steady-state supporting logical operations. A typical static gate delivers power supply to its output levels. An outsized range of transistors may nonetheless be required to get a performance and there should be a big delay. The example of 2-input gates is why the static CMOS logic is performing fundamentally. The path between the output nodes is run such that the floor offers a high-value logic to measure the V_A and V_B input voltage [10].

3.2 Dynamic CMOS Logic (Pre Charge - Evaluate Logic)

Dynamic CMOS Circuit Technologies that decreases the number of transistors needed for any logic in the USA substantially. The operation of the circuit is based on the initial preload for the output node and the output level is then evaluated according to the inputs applied. Each designed square measuring for a one-clock signal that powers a single NMOS and an electronic PMOS transistor in each dynamic step. Dynamic F = (AI A2 A3 + BB2) implementation of a CMOS gate. The PMOS electronic transistor MP pre-charge is conducted although the clock signal is low (pre-charge) and the NMOS transistor is comparable to that of the US. Logically high V_{OID} = VDD level is charged for the parasitic power output of such a circuit by the PMOS electronic transistor [11].

The output node voltage can now be at a high level of logic or a low level of logic with input voltage levels. The output capacitation can be discharged into VOL = zero V when the input signal provides the path from the output node to the floor. It is rather straightforward to operate the single stage dynamic CMOS gate. However, the dynamic CMOS gate has a major disadvantage for sensitive multi-stage applications. Consider the two-stage cascaded arrangement illustrated in the following image to see this basic constraint In this case, one input from the second dynamic CMOS stage is supposed to be an input gate for simplicity, the output from the primary dynamic CMOs stage. Each V_{out1} and V_{out2} square output voltages indicate strength in the pre-charge section by different pre-charge devices of PMOS.

In addition, the measurement for external inputs was applied in all areas [12].Throughout the analytical portion, you can download the input variable for the primary step square measurement that supposes the output V0outj to logical "0." On the other hand, a "one" logic is considered to be the external input of the second-stage NAND2 gate. Each output voltages V_{outl} and V_{out2} square measure the logic-high measurement once the analysis portion starts. When an accurate time delay is established, the output of the primary step (Vocal) decreases to the right logic level.

Nevertheless, when this analysis is done concurrently at the commencement of its analysis section, starting with a high value of V_{outl}, the V_{out2} output tension in the end of the analysis section will be incorrectly small. Although the primary output assumes the proper output value once the retain charge is exhausted [13], it is not possible to adjust the second stage output. This example demonstrates that dynamic CMOS logic levels controlled by a clock signal equivalent cannot be cascaded directly. This extreme constraint undermines all the contrary benefits of dynamic CMOS, such as low-power dissipations, enormous noise margins.

The circuit enabled preliminary pre-charging and evaluation of the output level according to the applied inputs of the output node. The pre-load portion sets the circuit to a starting status preset while the individual logic response is specified mostly in analysis section. Nevertheless, Static CMOS delivers intelligent performance in terms of propagation latency and cannot continue dynamic logic architectures. In order to increase power dissipation it is mostly necessary to list brief delays.

3.3 True Single-Phase Clock (TSPC) Dynamic CMOS

The following dynamic circuit technology is dissimilar from either the NORA CMOS circuit design, where just a 1-clock signal is used that is not inversed. Since I'm not using the inverted clock signal mostly in system, there is no disadvantage of the clock. Therefore, for dynamic pipeline operation, higher clock frequencies will be achieved. The circuit comprises of alternate phases, known as *n*-blocks and p-blocks, and the same clock signal *p* drives each block. A Nursing *N*-Block is formed through the cascade of a dynamic NMOS stage and a dynamic latch, whereas a dynamic PMOS phase and a dynamic latch is formed through cascade. When the clock signal is down, a PMOS electronic transistor pre-loads the output n-block to the V_{DD}. The output is measured and the output latch consequently provides a genuine output level when the clock signal changes from low to high. On the contrary, the p-block is preloaded after a high clock and evaluated once a low clock has been lowered. This means that the cascade coupling of the N-block and P-block alternating circuits can allow a single clock signal to operate the pipeline. We require 2 more transistors per stage compared to NORA CMOS [13].

3.4 Pulse Triggered Flip Flop

Owing to their one-lace design, Pulse-triggered FF (P-FF) is much frequent in high-speed applications as the classic transmission gate (TG) and master slave-based mainly FFs. In addition to its speed benefit, its simplicity reduces the clock tree system's easy usage. A PFF includes a stroboscope signal generator and an information systems security latch. If

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somehow the square pulse is thin enough, the latch functions as a triggered FF. Because just 1 lock, as hostile 2 is necessary within the normal master slave arrangement, P-FF reliability is easy.PF-FFs would be implicitly or definitely described in terms of pulse generation as Associate in nursing. The pulse generator is an integral component of the lock style in nursing implicit kind P-FF, and no explicit pulsing signal quadrant is created. In a certain P-FF type the generator of heart beat and therefore the latch square measurement separate while not generating pulse signals, implicit sorting P-FFs square typically measures a lot of energy-efficient [14]. They suffer nevertheless from a prolonged release route, which leads to lower time arrangements. Accelerated pulse production, on the alternative, generates a lot of electricity consumption, while the logical dissociation of the latch type gives the FF style a unique speed benefit. It effectively reduces its power consumption and therefore circuit quality if one generator shares a gaggle of FFs; we thus shall specialize on explicit type P-FF styles just during this brief period. To compare the current P-FF styles, a traditional P-FF style, termed data near to output (ep-DCO), is shown on the top of the examined square measurements. It comprises a NAND-logic-based generator and just a latch type constructed in semi-dynamic single phase clock (TSPC) [15].

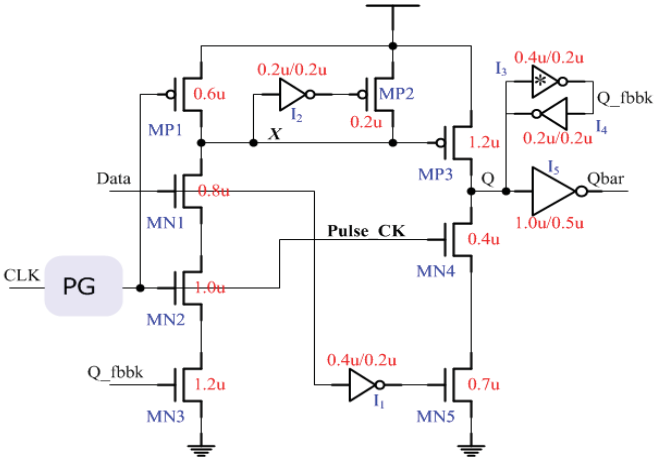

Figure 1: ep-dco flip flop

Upon top including its schematic, an extra NMOS electronic transistor MN3 controlled by the Q fdbk output is used for a conditionally discharged method (CD), so that no discharge takes place when "1" persist in the input file. Further, the defender logic for the internal X node in the nursing system is simplified Associate consisting just of a PMOS transistor and an electric converter. *Figure 1* shows the ep-dco flip flop.

The diagram above illustrates a similar P-FF, Static Conditional Discharge Flip Flop (SCDFF) style using static conditional unloading. In using the static latch structure, the style of the CDFF varies. Accordingly, Node X is free from periodic pre-requirements. The delay is longer than the CDFF style from D-to-Q. A download path made of 3 stacked transistors, *i.e.* MN1-MN3, leads to a worse latency in every style.

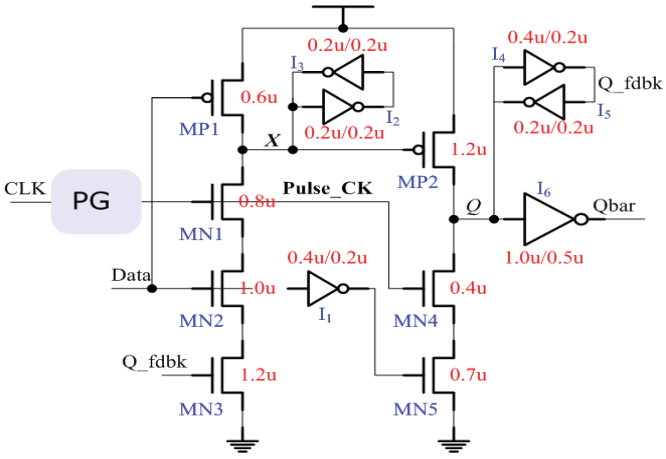

Figure 2: Cd-flip flop

Pull-down electronic equipment is essential to resolve considerable delay, which offers ample lay-out area and power consumption. The hybrid latch flip flop employs a fixed latch cooperatively and is deleted with node X keeping logic. Figure 2 depicted Cd-flip flop structure. The size of the x node is maintained when letter 0 is kept by a weak electronic transistor MP1 controlled by output letter. 2 inconveniences, X-node is not pre-downloaded, prolonged zero is predicted to be extended by one delay.

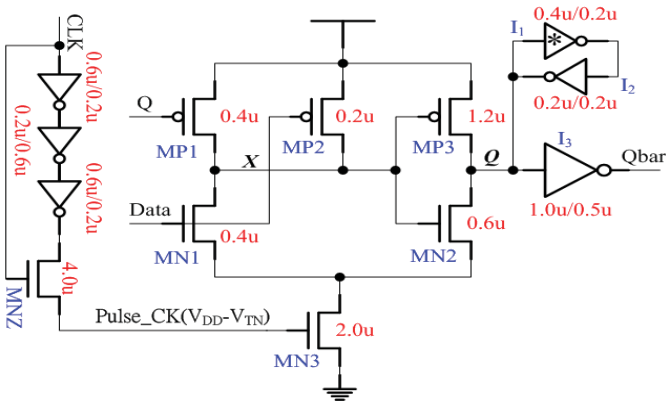

Figure 3: SCd-flip flop

Figure 3 shows the SCd-flip flop model. As a consequence of a level deteriorated clock pulse, the delay deteriorated more as the MN3 node X discharge electronic transistor floats, and its value might influence the drift inflicting additional dc power.

4. PROPOSED MODULE DESCRIPTION

The Flip flips we saw in current style are affected by the problems that all of them face a time schemes of zero to one control and data in an analogous worst scenario. In order to increase this latency the planned style uses a proof-feed approach. Like the style of the SCDFF, the proposed style combines a static latch structure with a conditional discharge theme to minimize needless node shifts. There are nevertheless three important differences, each of which results in a unique

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TSPC latch structure, creating a different projected style from the preceding one.

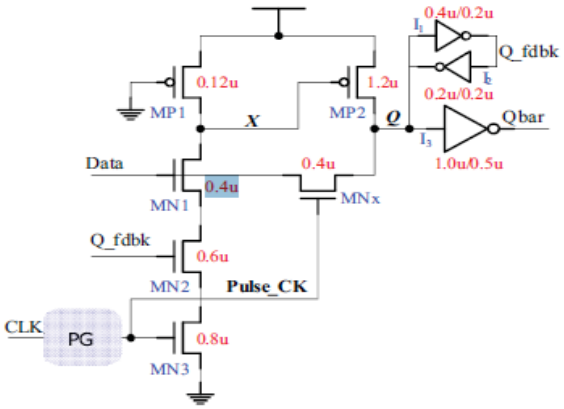

Figure 4: Proposed flip flop

The initial phase of a TSPC lock uses a weak electrical MP1 pull-up with a gate linked to the bottom. The load keeping circuit for the internal node X will be saved, which gives the pseudo-NMOS logic trend. This method decreases the load capacity of node X together to simplify the circuit. Secondly, an electronically controlled pass transistor MNx is included so that the latch node letter is directly driven by the input file. This further transmitter allows the auxiliary signal from the input supply to the letter node together with the pull-up of the electronic transistor MP2, at the second stage of the TSPC latch electrical converter. The level of the node is forced to reduce the transition time of information rapidly. Thirdly, the second-stage electric converter pull-down network is completely eliminated. The newly used electronic transistor MNx offers a download route. Thus, the role life of MNx is twice as important, that is, over zero to one transitions, the additional driving to node letter and the unloading of node letters via "1" to "0" transitions. The planned-type load keeper (two inverters), a pull-down network and electrical converter are the circuit savings of the projected style compared to the loop structure used in the SCDF-type.The proposed model Shown in *figure 4*.

Once the "I" to "0" transition of knowledge takes place, the SCDFF also activates the clock pulse on the electrical transistor MNx and the input step discharges the node letter through this route. The input supply does not carry the only actual discharge duty, like the case of "0" to "1." The loading result for the input supply isn't relevant as MNx is enabled for under a brief time. In particular, this discharge does not correlate to the fundamental route delay and does not require a tweak to strengthen the speed of the electronic transistor. Moreover, because the keeper logic is positioned on the node letter, the release duty of the supply is elevated as soon as the maintainer logic status is reversed.

4.1 Double Edge Triggered Flip Flop

At the rising and falling edges of the clock the flip-flop input is transferred to the output. The consumption of the facility is lowered when the electronic transistor is used. At each perimeter at the same moment, the information will be activated, thereby reducing clock power. The distribution of the clock power is important disadvantage, and hence the most prevalent technology is. In comparison to single edge triggering, this technique delivers greater turnout. For two-edge triggers, the frequency needed is 0.5 in comparison with the single-edge triggering. The dual edge causes the flip flop, thereby decreasing the delay to greater operating speed. It conjointly reduces space by triggering each positive and negative edge at the same time. It decreases space by simultaneously activating every positive and negative edge. Together, the pulse noise sensitivity is reduced. The measurement square of the inverters used in the double edge caused a flip flop and not a NAND door. The NMOS is provided on both sides and the clock is added. When the entry is supplied, the info on each edge is activated by the electrical converter. Therefore, when a clock is supplied, the information transfer is faster. Thanks to the gate, the current style occupies plenty of room. The anticipated style because space is reduced by just electrical converter. In order to prevent switching at an internal node, the design also uses a static latch structure and a conditional discharge technique. This system uses a standard explicit type pulse-triggered flip-flop to solve the lengthy discharge route problem. There is no data transition when a clock pulse appears. Table1 illustrated the Power Comparisons.

Table1: Power Comparisons

Parameter	Power (Watts) at Time 1.8328e-007	Power (Watts) at Time 1.8328e-007
Average power consumed	->1.87526e-003	1.0948176e-004
Max power	8.117876e-003	6.543203e-003
Min power	1.054530e-003	6.658484e-007

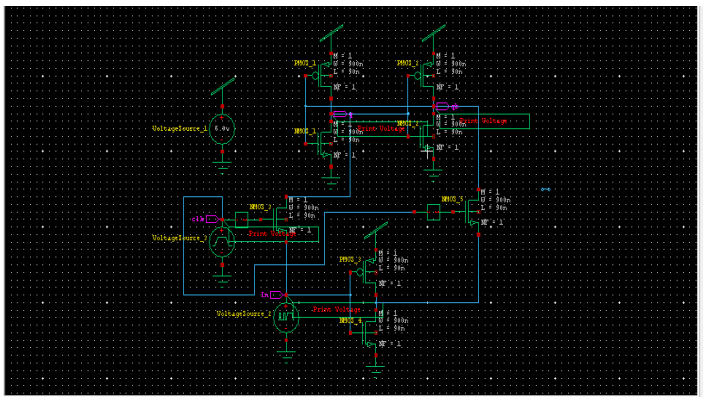

Figure 5: Schematic results of proposed scheme

The information activates either on a positive or a negative edge in single edge triggered flip flop. To convey the information it takes several cycles. The existing style of each generating gate is used. When the info is sent from zero to one with one to zero, the inverters cut down the dump path. *Figure 5* shows the Schematic results of proposed scheme.

5. SIMULATION RESULTS

The analyzed flip flop triggering pulse circuit extensively can be used in low power applications. It has been developed with

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EDA tanner toolsv13.0 for simulation. S-Edit is the key schematic designer. The circuit for Pulse generation in this first one and then generated, then, in the whole existing design, the same circuit is utilized and tested their performance and power, delay findings as given below. Compared with Ep-Dco and MHL FF, the suggested signal edge pulse triggered flop flip flop consume less power; the other two are CDFF and SCDFF, too. The following diagrams depict the resulting wave shapes. *Figure 6* showing the Schematic results of proposed scheme.

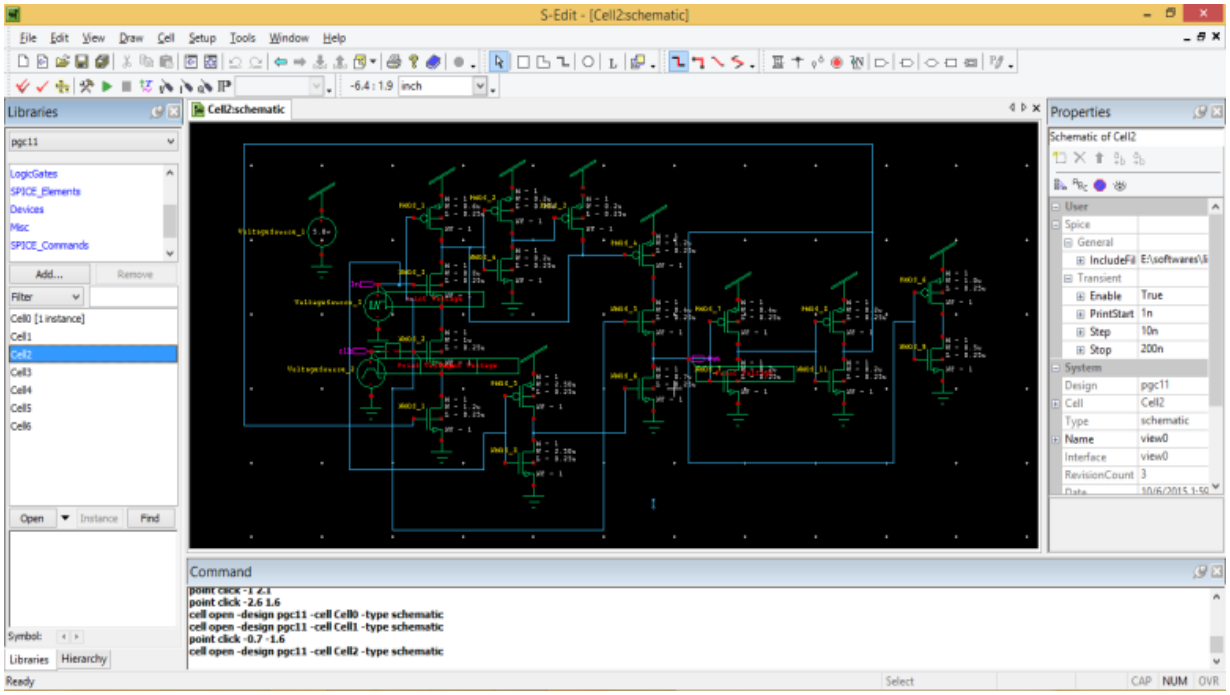

Figure 6: Schematic results of proposed scheme

Node Q and the input data are on the same level. Based on a signal feed-through system, low power P-FF architecture. By feeding the input signal straight to a latch design internal node, the design is able to reduce the delay and quicken the data transition.

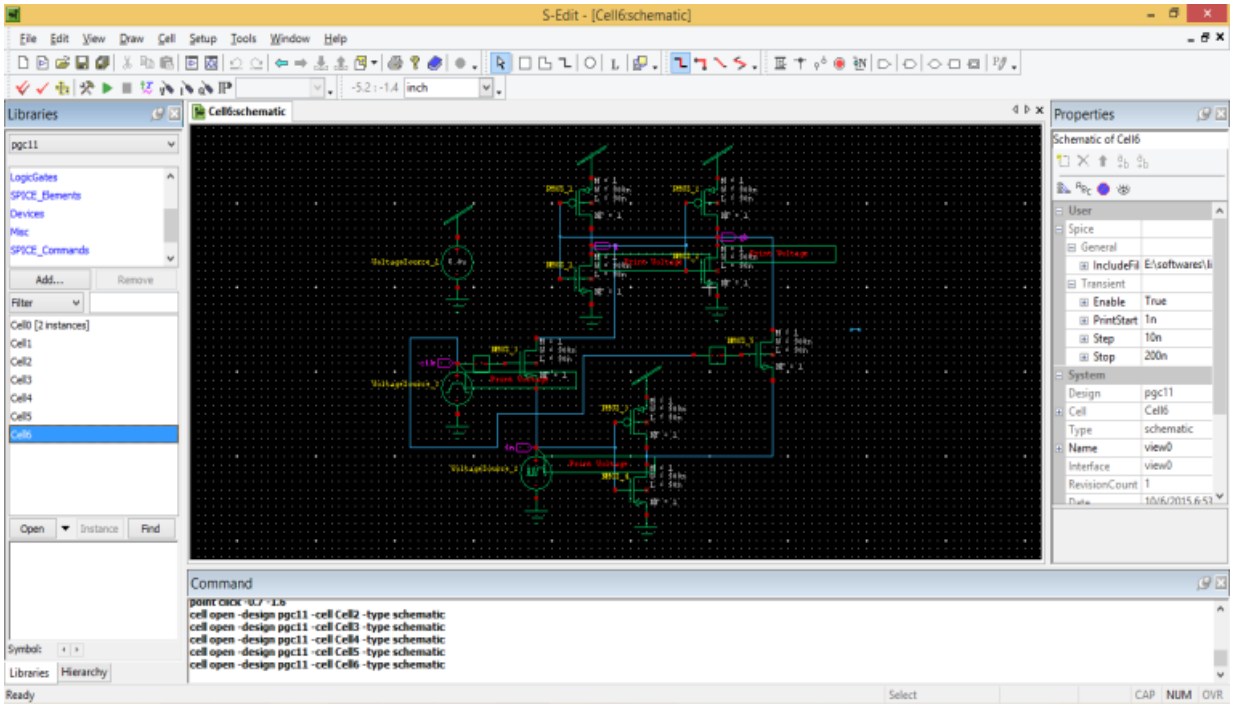

Figure 7: Schematic results of proposed scheme

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It results in a novel P-FF design with improved speed and power delay product (PDP) characteristics when paired with the pulse generation circuitry. *Figure 7* shows the Schematic results of proposed scheme.

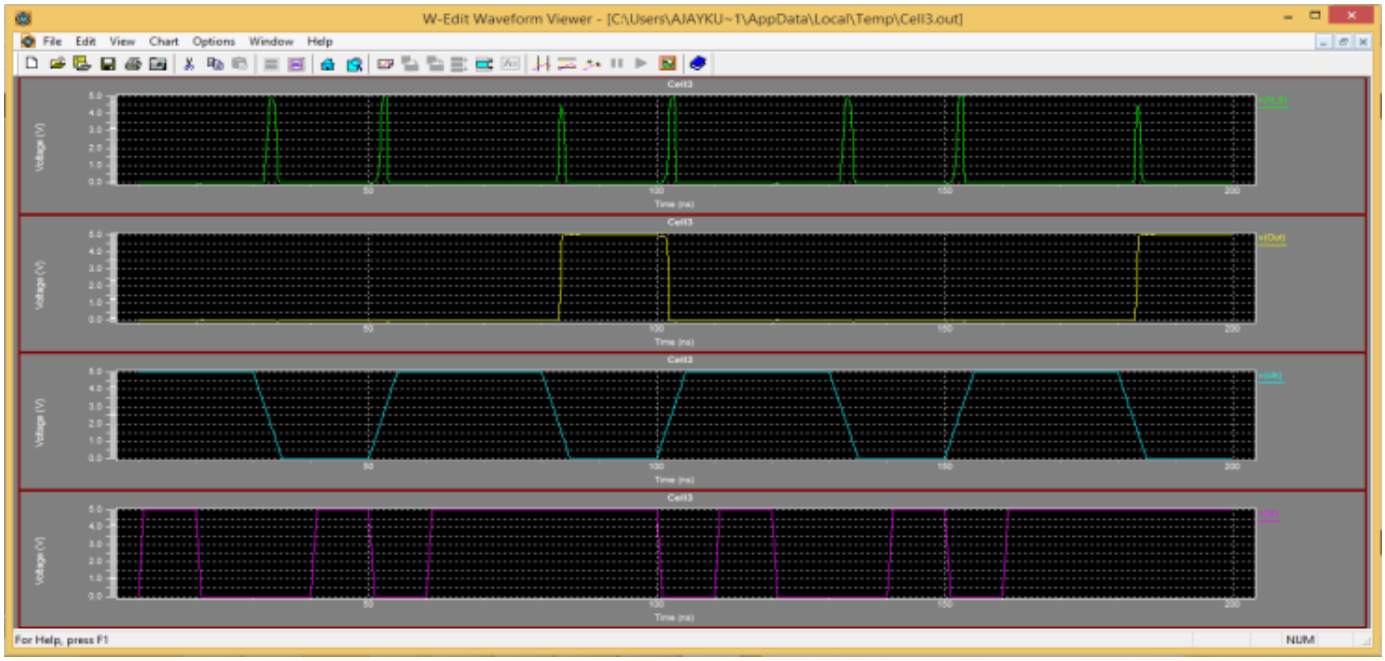

Figure 8: Simulation results of proposed scheme

The internal node(x) receives the input signal, which accelerates the data transition. An explicit type pulse-triggered structure and a modified true single phase clock latch based on a signal feed-through method are featured in a low power flip-flop design that is shown. The long discharge route issue in conventional explicit type Pulse- Triggered FF (P-FF) designs is successfully resolved by the proposed design, which also provides higher speed and power performance. *Figure 8* describes the Simulation results of proposed scheme.

Table2. Power comparisons at different time

Parameter	Power (Watts)
Average power consumed	-> 2.902832e-004
Max power	1.433808e-002
Min power	4.514772e-007

There are two sorts of pulse-triggered flip-flop designs: implicit type and explicit type. The logic for creating the clock has a latch built in. The clock generation and latch are distinct in an explicit type. Implicitly induced pulses Flip-flops are thought to use less energy than explicitly typed pulse triggered pulses. *Table 2* shows the Power comparisons at different time.

6. CONCLUSION

The single edge triggered true one-stage flip flop and double edge triggered flip flop with pulsing feed system are designed and analyzed with low power and speed. During this period we also built circuits based on existing literature such as Ep-DCO, CDFF, S-CDFF and MHLFF. This design is also implemented by using the double edge clocked technique. Substantial power savings in the clock distribution network can be achieved by reducing the clock frequency by one half. Hence it is concluded that this design achieves low power consumption. Shift registers has been constructed to show how the power will decrease as the sharing of a single pulse generator among multiple flip- flops is increased can be extended for the future work.

REFERENCES

[1] Kawaguchi, H.; Sakurai, T.A Reduced Clock-Swing Flip-Flop (RCSFF) for 63% Power Reduction. I.E.E.E. J. Solid State Circuits May1998, 33 (5), 807–811. DOI: 10.1109/4.668997
[2] S.Ravi Chand, K.V.Ganesh, M.Sailaja On-Chip Generation of Accumulator Based 3- Weighted Test Pattern Generation for Synchronous VLSI Circuits" IJAER, Vol 2015, ISSN: 0973-4562, 10 (1), online ISSN 1087-1090
[3] Chen, K.A 77% Energy saving 22-Transistor Single Phase Clocking D flip- Flop with Adoptive – Coupling Configuration in 40 nm CMOS. In Proceedings of the IEEE Interface Solid-State Circuits Conference, November 2019, pp 338–339.
[4] Consoli, E.; Alioto, M.; Palumbo, G.; Rabaey, J.Conditional Push pull pulsed Latch with 726 f Jops Energy Delay Product in 65 nm CMOS. In Proceedings of the IEEE Interface Solid-State Circuits Conference, February 2020, pp 482–483.
[5] S. RaviChand, Dr.M.Sailaja, Dr.T.Madhu, Fault Tolerant Multicore Architecture with Hardware Reconfigurable Unit" published in SYLWAN JOURNAL, Poland 2017 ISSN: 0039-7660, 161 (8).
[6] S.Ravi Chand, Dr.M.Sailaja, Dr.T.Madhu. SRAM Based Fault Tolerant Technique for Detection of Transient Errors in Processors through P T Logic" published in International Journal of Computer Applications (IJCA) USA, October2017, IJCA**,** Volume 176 ISSN: 0975–8887-No.3.
[7] S tojanovic, V.; O klobdzija, V. G. Comparative Analysis of Master slave latches and Flip-Flops for High-Performance and Low-Power Systems. I.E.E.E. J. Solid State CircuitsApril1999, 34 (4), 536–548. DOI: 10.1109/4.753687
[8] S. Ravi Chand, Dr.M.Sailaja, Dr.T.Madhu. Design and Analysis of Transient Fault Tolerance in SRAM with Different NT Techniques" IJCA; October 2016,Volume 151 – No.3, ISSN: 0975 – 8887

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[9] S. Ravi Chand, Dr.M.Sailaja, Dr.T.Madhu. Fault Diagnosis for Using Tpg Low Power Dissipation and High Fault Coverage, I.E.E.E. Conference Publications Pages; Vols. 1–5, p 978-1-4244-5967-4/10/$26.00 ©2010 IEEE. DOI: 10.1109/ICCIC.2010.5705884
[10] Alioto, M.; Consoli, E.; Palumbo, G. General Strategies to Design Nanometer Flip-Flops in the Energy-Delay Space. IEEE Trans. Circuits Syst. IJuly2010, 57 (7), 1583–1596. DOI: 10.1109/TCSI.2009.2033538
[11] Alioto, M.; Consoli, E.; Palumbo, G. Flip-Flop Energy/Performance versus Clock Slope and Impact on the Clock Network Design. IEEE Trans. Circuits Syst. IJune2010, 57 (6), 1273–1286. DOI: 10.1109/TCSI.2009.2030113
[12] Alioto, M.; Consoli, E.; Palumbo, G. Analysis and Comparison in the Energy-Delay-Area Domain of Nanometer CMOS Flip-Flops: Part I - Methodology and Design Strategies. I.E.E.E. Trans. Very Large Scale Integr. (VLSI) Syst.May2011, 19 (5), 725–736.
[13] Alioto, M.; Consoli, E.; Palumbo, G. Analysis and Comparison in the Energy-Delay-Area Domain of Nanometer CMOS Flip-Flops: Part II - Results and Figures of Merit. I.E.E.E. Trans. Very Large Scale Integr. (VLSI)Syst.May2011, 19 (5), 737–750
[14] Bai-Sun Kong; Sam-Soo Kim; Young-Hyun Jun. Conditional- Capture Flip-Flop for Statistical Power Reduction. I.E.E.E. J. Solid State CircuitsAugust2001, 36 (8), 1263–1271. DOI: 10.1109/4.938376
[15] Shilpa K.C, Lakshminarayana C, "Optimized Low Power Dual Edge Triggered Flip-flop with Speed Enhancement", International Journal of Image, Graphics and Signal Processing (IJIGSP), Vol.14, No.1, pp. 50-63, 2022.DOI: 10.5815/ijigsp.2022.01.05
[16] Dasari Ramanna and V. Ganesan (2022), Low-Power VLSI Implementation of Novel Hybrid Adaptive Variable-Rate and Recursive Systematic Convolutional Encoder for Resource Constrained Wireless Communication Systems. IJEER 10(3), 523-528. DOI: 10.37391/IJEER.100320.
[17] Hyogeun An, Sudong Kang, Guard Kanda and Prof. Kwangki Ryoo (2022), 128-Bit LEA Block Encryption Architecture to Improve the Security of IoT Systems with Limited Resources and Area. IJEER 10(2), 245-249. DOI: 10.37391/IJEER.100232.
[18] B. Murali Krishna, Chella Santhosh, S.K. Khasimbee (2022), FPGA Implementation of High-Performance s-box Model and Bit-level Masking for AES Cryptosystem. IJEER 10(2), 171-176. DOI: 10.37391/IJEER.100221.