FOREX Publication
Open Access | Rapid and quality publishing

International Journal of
Electrical and Electronics Research (IJEER)
Research Article | Volume 10, Issue 4 | Pages 1115-1120 | e-ISSN: 2347-470X

Modelling and Analysis of Non-ideal Two stage Lift Luo Converter with Positive Output

T.S. Saravanan[1*], K. A. Indu Sailaja[2], P. Marish Kumar[3], G. Merlin Suba[4] and K. Palanivel Rajan[5]

[1]*Assistant Professor, Department of EEE, Rajalakshmi Engineering College, Thandalam, chennai, Tamil Nadu – 602105, Email: saravanan.ts@rajalakshmi.edu.in*

[2]*Assistant Professor, Department of EEE, Easwari Engineering College, Ramapuram, Chennai, Tamil Nadu – 600089, Email: sailaja.indu@gmail.com*

[3]*Associate Professor, Department of EEE, Easwari Engineering College, Ramapuram, Chennai, Tamil Nadu – 600089, Email: marishkumar.p@eec.srmrmp.edu.in*

[4]*Associate Professor, Department of Electrical and Electronics Engineering,Panimalar Engineering College Chennai, Tamil Nadu 600123 ,India, Email: merlinsubag@gmail.com*

[5]*Assistant Professor, Department of ECE, PSNA College of Engineering and Technology, Kothandaraman Nagar, Tamil Nadu 624 622, Email: kpvrajaneee@psnacet.edu.in*

***Correspondence:** T. S. Saravanan; Email: saravanan.ts@rajalakshmi.edu.in;

ABSTRACT- High power applications such as motor drive control requires a higher voltage level of the DC-DC power converter fed from low-level DC input sources. For increasing the output voltage, a gain of the converter is increased using the pump circuit consisting of inductors and capacitors connected in different forms. The effect of adding the energy storage elements includes the parasitic resistances in the converter and affects the performance. This research paper is intended to model and investigate the effects of non-idealities in two stages cascaded lift circuit type Luo converter with positive output voltage. To analyze the non-ideal effects, state-space averaging (SSA) technique is used to model the converter. The converter is modeled in the presence of equivalent series resistance (ESR) of inductances and capacitances to study the effect of parasitic resistances on the converter performances. The transient and frequency response of the converter is plotted using the MATLAB simulation and observed that the ringing in the transient response is damped and oscillation at corner frequency is mitigated. The effect of ESR reduces the voltage gain and improves the stability of the system by increasing the gain and phase margin. Step response and bode plot of the converter is plotted at ideal and non- ideal condition.

Keywords: Relift Luo Converter, state-space averaging, transfer function model, phase margin, gain margin.

ARTICLE INFORMATION

Author(s): T.S. Saravanan, K. A. Indu Sailaja, P. Marish Kumar, G. Merlin Suba and K. Palanivel Rajan;

Received: 02/09/22; **Accepted:** 03/11/22; **Published:** 15/12/2022;
E- ISSN: 2347-470X;
Paper Id: IJEER220751;
Citation: 10.37391/IJEER.100457
Webpage-link:
https://ijeer.forexjournal.co.in/archive/volume-10/ijeer-100457.html

Publisher's Note: FOREX Publication stays neutral with regard to jurisdictional claims in Published maps and institutional affiliations.

1. INTRODUCTION

It is essential to boost the input source with low magnitude into an output with high magnitude for applications like DC drive systems, electric vehicles, battery charging and distributed generation. There are so many non- isolated topologies discussed in the literature to boost the output voltage from low-level sources such as cascaded boost [1], in which the basic boost converter is connected in series to increase the gain. In split inductor type Luo converter the pump inductor L is split in stages to increase the gain [2], In split capacitor type Luo converter the pump capacitor C is split in stages to improve the gain [3] and in hybrid split inductor and capacitor both pump inductor and capacitor is split in stages to boost the gain [4]. Application of Half bridge multiport converters in CubeSat with multiple inputs to increase the DC bus voltage is discussed in [5]. Zeta converter applied to solar water pumping model with improved gain and analysis of the converter is discussed in [6]. LLC resonant converter realization with SiC MOSFET switch improves the voltage gain, power density and efficiency of the converter [7] One such high voltage gain converter is Luo converter [8], [9] with different stages such as elementary and additional series super-lift converter.

This paper focuses on the relift type Luo converter [10] with two lift circuits cascaded together to improve the gain of the converter. In two stage cascaded Luo converter type the voltage gain is increased in geometric progression from initial stage to n stage. Though the voltage gain increases, complexity of the converter design, control and realization is also increased with the stages. The advantages of super-lift Luo converter compared to other topology is requirement of only one switch for any stages of realization, this reduces the complexity in control and PWM generation.

In order to study the non-ideal effects, on the behavior of the cascaded two stage lift circuit type Luo converter at steady and transient state a mathematical model of the converter is

FOREX Publication
Open Access | Rapid and quality publishing
International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 10, Issue 4 | Pages 1115-1120 | e-ISSN: 2347-470X

required. A different modelling approach are discussed in the literature such as switching flow graph [11], state space averaging (SSA) [12], average PWM switch [13] and energy factor approach [14] to deduce the output to input voltage transfer function. Out of these methods, SSA method simplifies the task of achieving transfer functions with less time and complexity. This paper model the non- ideal cascaded two stage lift Luo converter (NI-CTSLLC) using SSA technique and the MATLAB simulation software is used to compute the coefficient matrices of the average model. Time and frequency responses are plotted to infer the transient, steady state and stability of the NI- CTSLLC. The responses of the NI- CTSLLC are compared with the ideal cascaded two stage lift Luo converter (I-CTSLLC). From the above survey, it is inferred that different topologies are available and in each topology the energy storage elements inductors and capacitors are connected in the different forms to increase the gain of the converter. But in these high gain converters discussed, the effects of parasitic of the energy storage elements on the performance of the converter is not dealt. Moreover, the transient, steady state response and stability of the converter are analyzed for ideal conditions.

Following this section, the paper is structured into different sections with *section 2* describing the operations of NI-CTSLLC and the state space modelling of the NI-CTSLLC are deduced in the *section 3*. *Section 4* elaborates the derivation of transfer function using SSA and computation of coefficient matrices. Time and frequency response comparison are discussed in the *section 5*. Finally, conclusion is drafted in the *section 6.*

2. OPERATION OF NI-CTSLLC

In this section, operation of cascaded two stage lift LUO converter (CTSLLC) with positive output is discussed, which is a sixth order system. The complete circuit of CTSLLC is shown in *fig 1*. The circuit operation is discussed with the assumption that the converter is operating in the continuous conduction mode CCM. CTSLLC consists of first stage lift circuit components pump inductor L_1, diodes D_1 and D_2, capacitors C_1, C_2. The second stage lift circuit components are inductor L_2, diodes D_3 and D_4, capacitors C_2, C_4 and switch S. The equivalent series resistance (ESR) of the first stage lift circuit inductor is r_1 and capacitors are r_2, r_3. In the same manner, ESR of the second stage lift circuit inductor is r_4 and capacitors are r_5, r_6.

NI-CTSLLC operation when switch S is closed is highlighted in *fig. 2*. At switch – ON mode time elapse, energy stored in the pump inductor L_1 is increased and the inductor voltage is equal to V_{in}. The Input supply voltage V_{in} forward biases the diode D_1 and the voltage across the capacitor C_2 equal to V_1 reverse biases the diode D_2. Pump inductor L_2 stores the energy and the voltage across the inductor L_2 is equal to the first stage lift circuit voltage V_1. Voltage V_{C4} across the capacitor C_4 reverse biases the diode D_4.

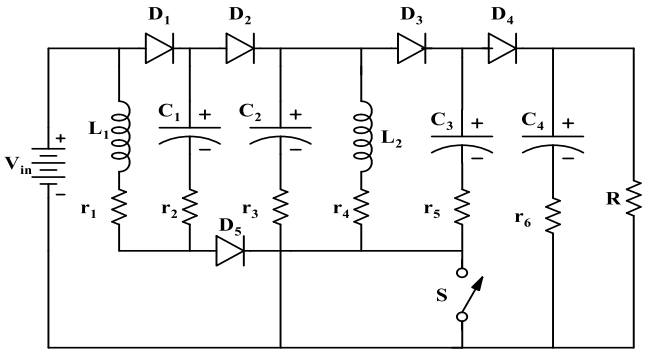

Figure 1: NI- CTSLLC circuit

Operation of NI-CTSLLC during switch-OFF condition is shown in *fig. 3*. Voltage across the capacitor C_1 reverse biases the diode D_1. Voltage on the input side, inductor V_{L1} and voltage across the capacitor C_1 forward biases the diode D_2 and charges the first stage lift circuit capacitor C_2 to V_1. First stage lift circuit voltage V_1 and voltage across inductor L_2 forward biases the diode D_4 and charges the capacitor C_4. Voltage across the capacitor C_3 reverse biases the diode D_3. In OFF- state Diode D_5 is reverse biased by the voltage across the inductor L_2, which is greater than the diode D_5 anode voltage.

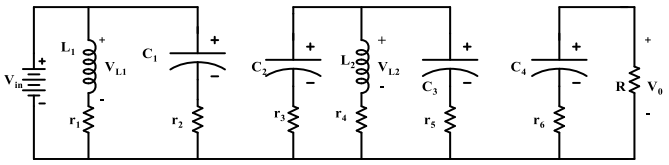

Figure 2: NI- CTSLLC t_{ON} equivalent circuit

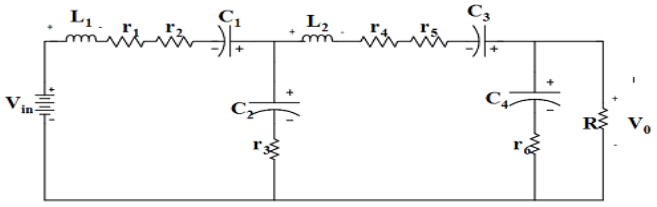

Figure 3: NI- CTSLLC t_{OFF} equivalent circuit

During t_{on} the voltage across the capacitor C_1 is charged to the supply voltage V_{in} and the voltage across the capacitor C_1 is equal to 10.02 V at the steady state condition as shown in the *fig 4*. During t_{off} state, the capacitor C_2 is charged to the voltage equal to $V_{in} + V_{L1}+V_{C1}$. As shown in *fig 4* the voltage across the capacitor C_2 at steady state is equal to 33.87V. Capacitor C_3 is charged to the first stage output voltage equal to the voltage across the capacitor C_2. From the *fig 4*, at steady state the voltage across the capacitor C_3 is equal to 32.43 V during t_{on}. During t_{off}, the energy stored in the inductor L_2 and C_3, charges the capacitor C_4 to $(V_1 + V_{L2}+ V_{C3})$. So the voltage across the capacitor C_4 is equal to 105.54V at steady state condition, which is also equal to the output voltage V_0. Ripple in the output voltage of CTSSLLC is shown in the *fig 5*. From the *fig 5*, it is inferred that the maximum peak to peak ripple voltage is equal to 10 mV and the ripple factor is equal to .0009% which is very

FOREX Publication
Open Access | Rapid and quality publishing
International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 10, Issue 4 | Pages 1115-1120 | e-ISSN: 2347-470X

much less than the standard value of 1%, so the output voltage is a stiffed DC voltage.

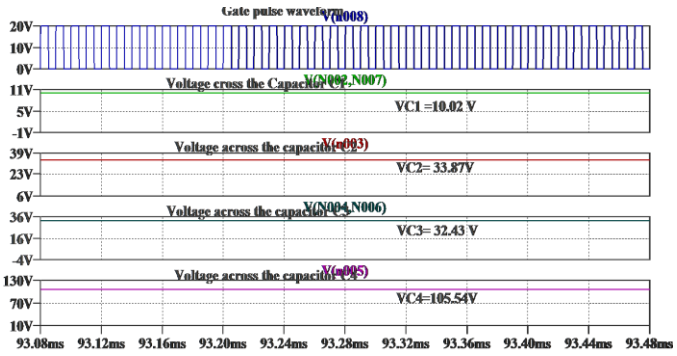

Figure 4: Voltage waveforms across the capacitors C1, C2, C3 and C4

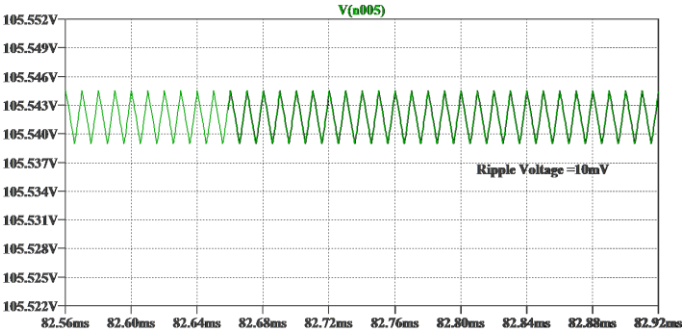

Figure 5: Ripple Voltage of CTSLLC

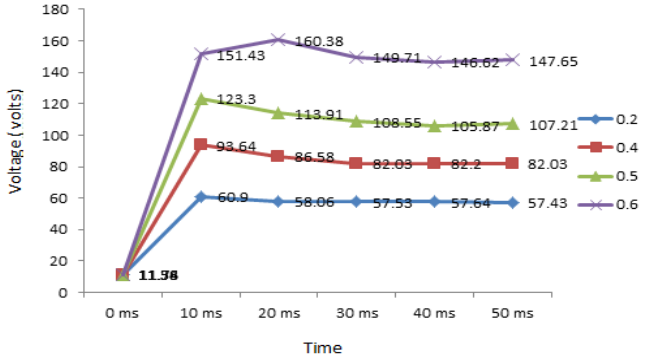

Figure 6: Output voltage of CTSLLC with variation in duty ratio

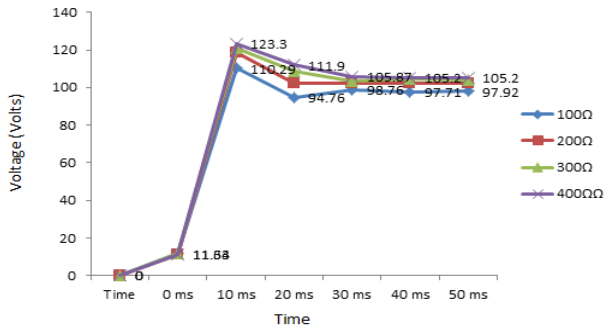

Figure 7: Output voltage of CTSLLC with variation in the load resistance

Output voltage variation with respect to change in the duty cycle is shown in the *fig 6*. It is inferred that CTSSLLC increases its output voltage with change in the duty ratio. For 0.6 duty ration the steady state output voltage is equal to 147.65 V. *Fig 7* shows the output voltage variation with respect to change in the load resistance with duty ratio fixed to 0.5 and input voltage equal to 12 V. It is observed from *fig 7* for 100Ω load the steady state output voltage is equal to 97.92 V and with 400 Ω load resistance the output voltage is increased to 105.2V. This increase in the output voltage is caused due to decrease in the input current drawn from the source and drop in the passive components.

3. STATE SPACE MODELLING OF NI-CTSLLC

Modelling of the converter is done to predict the transient and steady state response. This paper utilizes the SSA approach to model and infer the performance of the converter. Normally in any converters, state equations are written by choosing the state variables. State variables are equal to the energy storage elements in the converter. In NI- CTSLLC, six energy storage elements are used so six state variables such as x_1 equal to inductor current i_{L1}, x_2 equal to capacitor voltage v_{C1}, x_3 equal to capacitor voltage v_{C2}, x_4 equal to inductor current i_{L2}, x_5 equal to capacitor voltage v_{C3} and x_6 equal to capacitor voltage v_{C4} are chosen with u and y as input and output variable [15].

Turn-ON equivalent state equations for the first stage lift circuit are

$$\frac{di_{L1}}{dt} = \dot{x_1} = \frac{1}{L_1}u - \frac{r_1}{L_1}x_1 \quad (1)$$

$$\frac{dv_{c1}}{dt} = \dot{x_2} = \frac{1}{r_1 c_1}u - \frac{1}{r_1 c_1}x_2 \quad (2)$$

$$\frac{dv_{c2}}{dt} = \dot{x}_3 = \frac{1}{c_2(r_3+r_5)}x_5 - \frac{r_5}{c_2(r_3+r_5)}x_4 - \frac{1}{c_2(r_3+r_5)}x_3 \quad (3)$$

Turn-ON equivalent state equations for second stage lift circuit are

$$\frac{di_{L2}}{dt} = \dot{x}_4 = \frac{1}{L_2(1+r_3)}x_5 - \frac{r_4 - r_3 + r_3.r_4}{L_2(1+r_3)}x_4 + \frac{r_3}{r_5(1+r_3)}x_5 \quad (4)$$

$$\frac{dv_{c3}}{dt} = \dot{x_5} = \frac{1}{L_2(r_3+r_5)}x_3 - \frac{1}{c_3(r_3+r_5)}x_5 - \frac{r_3}{c_3(r_3+r_5)}x_4 \quad (5)$$

$$\frac{dv_{c4}}{dt} = \dot{x}_6 = \frac{1}{(R+r_6)c_4}x_6 \quad (6)$$

Output equation

$$Y(t) = \frac{R}{R+r_6}x_6 \quad (7)$$

Turn-OFF equivalent state equations for the first stage lift circuit are

$$\frac{di_{L1}}{dt} = \dot{x}_1 = \frac{1}{L_1}u_1 - \frac{(r_1+r_2+r_3)}{L_1}x_1 + \frac{1}{L_1}x_2 - \frac{1}{L_1}x_3 + \frac{r_3}{L_1}x_4 \quad (8)$$

$$\frac{dv_{c1}}{dt} = \dot{x}_2 = \frac{-1}{c_1}x_1 \quad (9)$$

$$\frac{dv_{c2}}{dt} = \dot{x}_3 = \frac{1}{c_2}x_1 - \frac{2}{r_3 c_2}x_3 + \frac{1}{r_3 c_2}x_5 - \frac{x_4}{c_2} \quad (10)$$

Turn- OFF equivalent state equations for the second stage lift circuit are

FOREX Publication
Open Access | Rapid and quality publishing
International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 10, Issue 4 | Pages 1115-1120 | e-ISSN: 2347-470X

$$\frac{di_{L2}}{dt} = \dot{x_4} = \frac{1}{L_2}x_3 + \frac{1}{L_2}x_5 - \frac{\left(1-\frac{r_6}{R+r_3}\right)}{L_2}x_6 + \frac{r_3}{L_2}x_1 - \left(\frac{r_3+r_4+r_5+\frac{R.r_6}{R+r_6}}{L_2}\right)x_4 \quad (11)$$

$$\frac{dv_{c3}}{dt} = \dot{x}_5 = \frac{-1}{c_3}x_4 \quad (12)$$

$$\frac{dv_{c4}}{dt} = \dot{x}_6 = \frac{R}{(R+r_6)C_4}x_4 - \frac{1}{(R+r_6)c_4}x_6 \quad (13)$$

Output equation

$$Y(t) = \frac{r_6 R}{R+r_6}x_4 + \frac{R}{R+r_6}x_6 \quad (14)$$

State equation matrix form at Turn- ON condition

$$\begin{bmatrix}\dot{x_1}\\ \dot{x_2}\\ \dot{x_3}\\ \dot{x_4}\\ \dot{x_5}\\ \dot{x_6}\end{bmatrix} = \begin{bmatrix}\frac{r_1}{L_1} & 0 & 0 & 0 & 0 & 0\\ 0 & \frac{-1}{r_1c_1} & 0 & 0 & 0 & 0\\ 0 & 0 & \frac{-1}{c_2(r_3+r_5)} & \frac{-r_5}{c_2(r_3+r_5)} & \frac{1}{c_2(r_3+r_5)} & 0\\ 0 & 0 & \frac{1}{L_2(1+r_3)} & \frac{-(r_4-r_3+r_3.r_4)}{L_2(1+r_3)} & \frac{r_3}{r_5(1+r_5)} & 0\\ 0 & 0 & \frac{1}{c_3(r_3+r_5)} & \frac{-r_3}{c_3(r_3+r_5)} & \frac{1}{c_3(r_3+r_5)} & 0\\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{(R+r_6)c_4}\end{bmatrix}\begin{bmatrix}x_1\\ x_2\\ x_3\\ x_4\\ x_5\\ x_6\end{bmatrix} + \begin{bmatrix}\frac{1}{L_1}\\ \frac{1}{r_1c_1}\\ 0\\ 0\\ 0\\ 0\end{bmatrix}[u] \quad (15)$$

Output voltage equation matrix form at Turn - ON condition

$$[Y] = \begin{bmatrix}0 & 0 & 0 & 0 & 0 & \frac{R}{R+r_6}\end{bmatrix}\begin{bmatrix}x_1\\ x_2\\ x_3\\ x_4\\ x_5\\ x_6\end{bmatrix} + [0][u] \quad (16)$$

State equation matrix form at Turn- OFF condition

$$\begin{bmatrix}\dot{x_1}\\ \dot{x_2}\\ \dot{x_3}\\ \dot{x_4}\\ \dot{x_5}\\ \dot{x_6}\end{bmatrix} = \begin{bmatrix}\frac{-(r_1+r_2+r_3)}{L_1} & \frac{1}{L_1} & \frac{-1}{L_1} & \frac{r_3}{L_1} & 0 & 0\\ \frac{-1}{c_1} & 0 & 0 & 0 & 0 & 0\\ \frac{(r_2+r_3)}{c_2r_3} & 0 & 0 & \frac{-1}{c_2} & 0 & 0\\ \frac{r_3}{L_2} & 0 & \frac{1}{L_2} & \frac{-(r_3+r_4+r_5+\left(\frac{Rr_6}{R+r_6}\right))}{L_2} & \frac{1}{L_2} & \frac{-(1-\frac{r_6}{R+r_3})}{L_2}\\ 0 & 0 & 0 & \frac{-1}{C_3} & 0 & 0\\ 0 & 0 & 0 & \frac{R}{(R+r_6)c_4} & 0 & \frac{-1}{(R+r_6)c_4}\end{bmatrix}\begin{bmatrix}x_1\\ x_2\\ x_3\\ x_4\\ x_5\\ x_6\end{bmatrix} + \begin{bmatrix}\frac{1}{L_1}\\ \frac{1}{r_1c_1}\\ 0\\ 0\\ 0\\ 0\end{bmatrix}[u] \quad (17)$$

Output voltage equation matrix form at Turn - OFF condition

$$[Y] = \begin{bmatrix}0 & 0 & 0 & \frac{r_4R}{(R+r_4)} & 0 & \frac{R}{R+r_6}\end{bmatrix}\begin{bmatrix}x_1\\ x_2\\ x_3\\ x_4\\ x_5\\ x_6\end{bmatrix} + [0][u] \quad (18)$$

4. TRANSFER FUNCTION DERIVATION OF NI-CTSLLC

In State space averaging (SSA) technique, weighted averaging of the equations from 15 to 18 yields the complete state space description of the NI- CTSLLC in one switching cycle. The state and output voltage averaged equations over one complete switching cycle is expressed by *equations 19 and 20*.

$$\dot{x} = Ax(t) + Bu(t) \quad (19)$$

$$y = C(x) + Du(t) \quad (20)$$

Where,

$$[A] = [A_1]K + [A_2](1-k)$$
$$[B] = [B_1]k + [B_2](1-k)$$
$$[C] = [C_1]k + [C_2](1-k)$$

Where, k and (1-k) are the turn- on and turn-off switching time instants.

The matrix A_1, B_1, C_1 during t_{ON} mode from *equations 15 and 16* is

$$A_1 = \begin{bmatrix}\frac{r_1}{L_1} & 0 & 0 & 0 & 0 & 0\\ 0 & \frac{-1}{r_1c_1} & 0 & 0 & 0 & 0\\ 0 & 0 & \frac{-1}{c_2(r_3+r_5)} & \frac{-r_5}{c_2(r_3+r_5)} & \frac{1}{c_2(r_3+r_5)} & 0\\ 0 & 0 & \frac{1}{L_2(1+r_3)} & \frac{-(r_4-r_3+r_3.r_4)}{L_2(1+r_3)} & \frac{r_3}{r_5(1+r_5)} & 0\\ 0 & 0 & \frac{1}{c_3(r_3+r_5)} & \frac{-r_3}{c_3(r_3+r_5)} & \frac{1}{c_3(r_3+r_5)} & 0\\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{(R+r_6)c_4}\end{bmatrix} \quad (21)$$

$$B_1 = \begin{bmatrix}\frac{k}{L_1}\\ \frac{k}{r_1c_1}\\ 0\\ 0\\ 0\\ 0\end{bmatrix} \qquad C_1 = \begin{bmatrix}0 & 0 & 0 & 0 & 0 & \frac{kR}{R+r_6}\end{bmatrix} \quad (22)$$

The matrix A_2, B_2, C_2 during t_{OFF} mode from *equations 17 and 18* is

$$B_1 = \begin{bmatrix}\frac{k}{L_1}\\ \frac{k}{r_1c_1}\\ 0\\ 0\\ 0\\ 0\end{bmatrix} \qquad C_1 = \begin{bmatrix}0 & 0 & 0 & 0 & 0 & \frac{kR}{R+r_6}\end{bmatrix} \quad (22)$$

The matrix A_2, B_2, C_2 during t_{OFF} mode from *equations 17 and 18* is

$$A_2 = \begin{bmatrix}\frac{-(1-k)(r_1+r_2+r_3)}{L_1} & \frac{(1-k)}{L_1} & \frac{-(1-k)}{L_1} & \frac{(1-k)r_3}{L_1} & 0 & 0\\ \frac{-(1-k)}{c_1} & 0 & 0 & 0 & 0 & 0\\ \frac{(1-k)(r_2+r_3)}{c_2r_3} & 0 & 0 & \frac{-(1-k)}{c_2} & 0 & 0\\ \frac{(1-k)r_3}{L_2} & 0 & \frac{(1-k)}{L_2} & \frac{-(1-k)(r_3+r_4+r_5+\left(\frac{Rr_6}{R+r_6}\right))}{L_2} & \frac{(1-k)}{L_2} & \frac{-(1-k)(1-\frac{r_6}{R+r_3})}{L_2}\\ 0 & 0 & 0 & \frac{-(1-k)}{c_3} & 0 & 0\\ 0 & 0 & 0 & \frac{(1-k)R}{(R+r_6)c_4} & 0 & \frac{-(1-k)}{(R+r_6)c_4}\end{bmatrix} \quad (23)$$

$$B_2 = \begin{bmatrix}\frac{(1-k)}{L_1}\\ \frac{(1-k)}{r_1c_1}\\ 0\\ 0\\ 0\\ 0\end{bmatrix} \qquad C_2 = \begin{bmatrix}0 & 0 & 0 & \frac{(1-k)r_4R}{(R+r_4)} & 0 & \frac{(1-k)R}{R+r_6}\end{bmatrix} \quad (24)$$

FOREX Publication
Open Access | Rapid and quality publishing
International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 10, Issue 4 | Pages 1115-1120 | e-ISSN: 2347-470X

Table 1 shows the simulation parameters of the NI- CTSLLC used in the *equations from 19 to 24* to compute the matrices A, B, C and D.

Table 1 Simulation Parameters of NI-CTSLLC

Parameters	Value
Input Voltage (V_{in})	12 V
Output Voltage (V_0)	108 V
Inductor (L_1)	10 mH
Inductor (L_2)	10 mH
Capacitor (C_1 to C_4)	220 µF
MOSFET operating frequency (f)	100 kHz
Resistive load (R)	470 Ω
Duty ratio (k)	0.5
Equivalent Series Resistances (ESR) r_1, r_2,r_3,r_4,r_5 and r_6	0.1Ω

$$A = 1X10^3\begin{bmatrix} 0 & 0 & -0.050 & 0 & 0 & 0 \\ -4.54 & 0 & 0 & 0 & 0 & 0 \\ 2.27 & 0 & 0 & -3.41 & 0 & 0 \\ 0 & 0 & 150 & 0 & 0 & -0.050 \\ 0 & 0 & 0 & -3.41 & 0 & 0 \\ 0 & 0 & 0 & 2.27 & 0 & -0.00967 \end{bmatrix}$$

$$B = 1X10^6\begin{bmatrix} 0.000150 \\ 2.2727 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

$$C = [0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 1]$$

$$D = [0]$$

The state space to transfer function conversion is done using A, B, C and D matrices in the MATLAB simulation tool. The obtained input to output voltage transfer function of the NI-PORSLLC is shown in the *equation 25*. From the transfer function, it is observed that the NI- CTSLLC has three zeros and six poles. Zeros of NI-CTSLLC are -169800 and -2100 ± j1800 and poles are -2291.9, -2140.5, -137.4 ± j 837.9 and -136.4 ± j 48.1. Using *equations 21 to 23*, transfer function of the ideal positive output relift type super-lift Luo converter I-CTSLLC is derived by letting the ESR's of inductance ($r_1 \approx 0$ and $r_2 = 0$) and ESR's of capacitances $r_3 = 0$, $r_4 = 0$, $r_5 \approx 0$ and $r_6 = 0$) with exception that ESR's r_1 and r_5 to be chosen close to zero. *Equation 26* shows the transfer function of the output to input voltage for the I-CTSLLC.

The six poles of I- CTSLLC are -4.18 ± j134, -0.659 ± j849, 0 and 0. Two Zeros of I- CTSLLC are $2.67x10^{-14}$ which is very close to zero.

$$\frac{V_0(s)}{V_i(s)} = \frac{24.94X10^2s^4 + 4.77X10^7S^3 + 2.57X10^{11}S^2 + 6.58X10^{14}S + 5.99X10^{17}}{S^6 + 4979.99S^5 + 8.1510^6S^4 + 6.51X10^9S^3 + 4.92X10^{12}S^2 + 1.06X10^{15}S + 7.40X10^{16}} \quad (25)$$

$$\frac{V_0(s)}{V_i(s)} = \frac{1.162X10^{11}S^2 - 1.99X10^{-5}S - 8.2157X10^{-17}}{S^6 + 9.6712S^5 + 7.38610^5S^4 + 6.044X10^6S^3 + 1.291X10^{10}S^2} \quad (26)$$

5. TIME AND FREQUENCY RESPONSE OF I-CTSLLC AND NI-CTSLLC

Equations 25 and 26 are used to plot the time and frequency response of NI-CTSLLC and I- CTSLLC. *Fig. 8* shows the step response comparison of NI- CTSLLC and I-CTSLLC. From the comparison, it is observed that the damping of oscillations in the transient state of the I-CTSLLC is damped out in the NI-CTSLLC step response. It is also observed that the steady state is reached in the NI- CTSLLC at 0.03s and in the I-CTSLLC at 1.4s. *Fig. 9* represents the frequency response of the I-CTSLLC and NI-CTSLLC comparison. From the response of NI-CTSLLC, it is observed that at two cross over frequencies the oscillations are damped out and smooth transition take place due to the effect of ESR's of the components in the CTSLLC [16].

The gain and phase margin of the NI-CTSLLC are 2.05 dB at phase crossover frequency equals to 652 rad/s and 24º at gain cross over frequency equals to 465 rad/s. For I- CTSLLC gain margin GM is -5.9 dB at 790 rad/s and phase margin PM is 0.549º at 674 rad/s. Since, the two margins are positive in the NI-CTSLLC the system is stable.

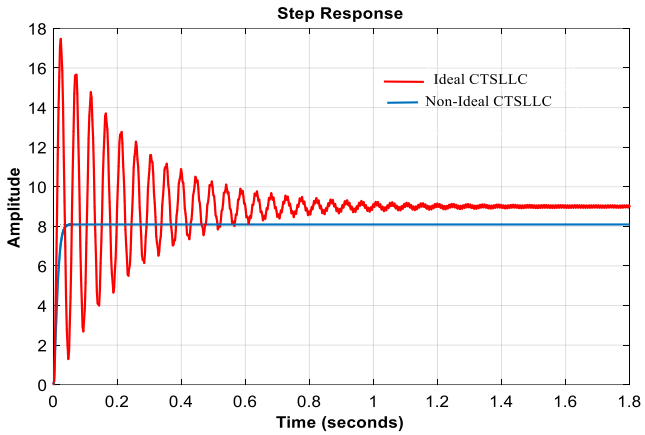

Figure. 8 Step response comparisons of I-CTSLLC and NI-CTSLLC

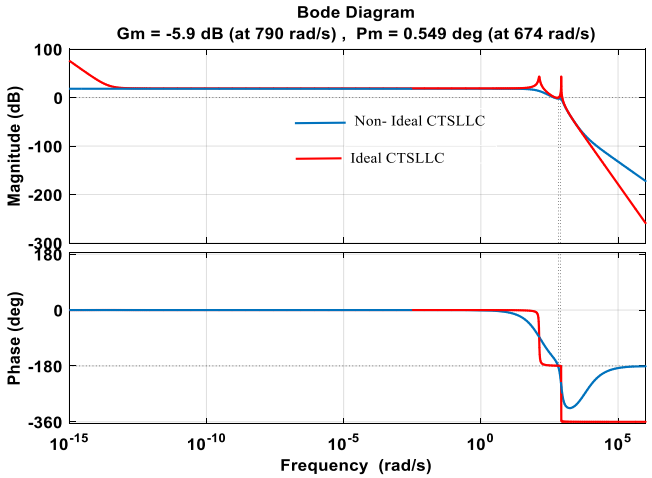

Figure. 9 Frequency response comparisons of I-CTSLLC and NI-CTSLLC

FOREX Publication
Open Access | Rapid and quality publishing
International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 10, Issue 4 | Pages 1115-1120 | e-ISSN: 2347-470X

The step response comparison graph shown in *fig. 8*, illustrates the variation of the output voltage of the converter at ideal and non-ideal conditions when the duty ratio of the converter is selected as 0.5. It is observed that in an ideal case the gain of the converter is equal to 9 while in the non-ideal case the gain is approximately equal to 8. For a fixed input voltage of a 12V, duty cycle is varied from 0.25 to 0.75 and the output voltage variation for ideal and non-ideal CTSLLC is shown in *table 2*.

It is observed from the *table 2*, that for 0.5 duty cycle, output voltage of NI- CTSLLC is 96 V. This voltage is 14V less than the converter output voltage in the ideal case, this drop in voltage is caused due to voltage drop across the parasitic resistances of the energy storage elements.

Table 2: Output voltage comparisons of the NI- CTSLLC and I- CTSLLC at steady state

Input Voltage (V_i)	Duty cycle	NI-CTSLLC Output voltage (V_0)	I-CTSLLC Output voltage (V_0)
12	0.25	61.49	64.42
12	0.5	96	108.2
12	0.75	226.16	261.28

Figure 10 shows the output voltage comparison of super lift Luo and CTSSLLC for different ratio with the input voltage fixed to 12 V. From the comparison it is inferred that for 0.5 duty ratio the super-lift Luo converter output voltage is equal to 36 V. And CTSSLLC output voltage is equal to 108 V.

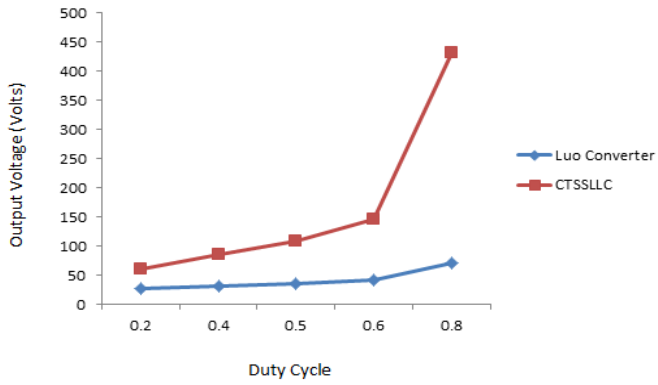

Figure.10 Output voltage comparisons of Luo and CTSLLC

6. CONCLUSIONS

Transient, steady state and stability analysis of NI-CTSLLC are addressed in this paper by considering the parasitic parameters of the passive components. From the study, it is observed that there is a damping of oscillation in the transient state and decrease of voltage transfer gain at steady state. This decrease is due to the voltage drop in the parasitic resistances. It also reveals that the stability of the converter at non – ideal condition is improved and the system is stable whereas, in ideal condition the gain margin is negative and the phase margin to the stability is less. This study concludes that the NI-CTSLLC has improved the transient state with the reduction in performance at the steady state. This modeling approach can be extended to infer the behavior of non-idealities in any DC-DC converter.

REFERENCES

[1] F.L.Luo and H. Ye "Positive output cascaded boost converters," IEE proceedings- Electric Power Applications Vol.151, issue 5, p. 590 – 640
[2] F. Luo, "Investigation on Split-inductors applied in positive output Super-Lift Luo-Converters," *2011 Chinese Control and Decision Conference (CCDC)*, 2011, pp. 2803-2808, doi: 10.1109/CCDC.2011.5968688.
[3] F.L.Luo "Investigation on hybrid split- capacitors and split-inductors applied in positive output super-lift Luo converters" IET power Electronics Vol.6, issue 9, p.328-334, 2011.
[4] Muhaideen M, Muralidharan S, Vanaja N "Multiport Converter for CubeSat" International journal of Electrical and Electronics Research Vol.10, issue 2, p.290-296, 2022.
[5] Vikash kumar, Amit Choudhary "Solar water pumping model using Zeta converter" International journal of Electrical and Electronics Research Vol.9, issue 3, p.84-88, 2022.
[6] Merlin Suba G. Kumaresan "Design of LLC resonant converter with silicon carbide MOSFET switches and nonlinear adaptive sliding controller for brushless DC motor system" *Electrical Engineering & Electromechanics*, (4), 34–3. https://doi.org/10.20998/2074-272X.2022.4.05
[7] Xiaofan Chen, Fang Lin Luo and Hong Ye, "Modified positive output Luo converters," Proceedings of the IEEE 1999 International Conference on Power Electronics and Drive Systems. PEDS'99 (Cat. No.99TH8475), 1999, pp. 450-455 vol.1, doi: 10.1109/PEDS.1999.794605.
[8] F. L. Luo and H. Ye, "Negative output super-lift Luo-Converters," IEEE 34th Annual Conference on Power Electronics Specialist, 2003. PESC '03., 2003, pp. 1361-1366 vol.3, doi: 10.1109/PESC.2003.1216785
[9] A. S. Tekade, R. Juneja, M. Kurwale and P. Debre, "Design of Positive Output Super-Lift Luo Boost Converter for Solar Inverter," 2016 International Conference on Energy Efficient Technologies for Sustainability (ICEETS), 2016, pp. 153-156, doi: 10.1109/ICEETS.2016.7582916.
[10] M. Zhu and F. L. Luo, "Modelling and Analysis of Super-Lift Converters with Switching Signal Flow Graph Method," 2006 IEEE Conference on Industrial Electronics and Applications, 2006, pp. 1-6, doi: 10.1109/ICIEA.2006.257067
[11] R. D. Middlebrook and S. Cuk, "A general unified approach to modelling switching converter power stages," in IEEE Power Electronics Specialists Conference, 1976, pp. 73–86.
[12] D. Czarkowski and M. K. Kazimierczuk, "Circuit models of PWM DC-DC converters," in IEEE Proc. of Aerospace and Electronics Conference, 1992, pp. 407–413.
[13] M. M. Garg, Y. V. Hote, and M. K. Pathak, "Notes on 'small signal analysis of energy factor and mathematical modeling for power DC-DC converters,'" IEEE Trans. Power Electron., vol. 29, no. 7, pp. 3548–3548, 2014.
[14] M. M. Garg, Y. V. Hote, and M. K. Pathak, "Leverrier's algorithm-based modeling of higher-order dc-dc converters," in IEEE India International Conference on Power Electronics, 2012, pp. 1–6.
[15] Simon Ang & Alejandro Oliva 2010, 'Power- Switching Converters', Second edition. Taylor & Francis group.