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VLSI Implementation of Integrated Massive MIMO Systems (IMMS) for N-point FFT/IFFT Processor

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ABSTRACT- The 5G technologies and OFDM introduce a substantial element of latency in the baseband Massive MIMO system. To declaim the low delay demand of multiple input and multiple outputs, a Fast Fourier Transform (FFT) and also consequent implementation was proposed. The main idea of this proposed system is to utilize the VLSI chip routing technology and reduce computations, processing time, and low latency. This proposed system is to reduce the number of computational complexities in the downlink and reorder the uplink. In OFDM implementation, the chip area of FFTs and IFFTs is occupied by memories, and these memories can be extracted using registers or RAM. An efficient data programming approach for memories and butterflies has been developed using embedded VLSI technology with multiple inputs and outputs (MIMO), known as mass embedded MIMO systems. Using this proposed scheme (Integrated Massive MIMO), N point FFT/IFFT processor design achieves a better throughput and lowest latency than for single-input pipelined FFT or IFFT architectures. In an N-point FFT/IFFT, the introduced scheme using VLSI Technology leads to more reduction in the latency. This N-point FFT/IFFT implementation is named "Integrated Massive MIMO Systems" (IMMS).

Keywords: Integrated Massive MIMO System (IMMS), OFDM, FFT, Latency, N-pt. IFFT/FFT implementation.

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1. INTRODUCTION

Rapid growth in wireless communication services, such as automation of all appliances, internet usage services, and machine-to-machine communications, leads to optimizing the 5G communication system. The new technology MIMO-OFDM has been used for the next generation communications such as 3GPP-LTE, wireless LAN, etc. MIMO, the multiple input multiple outputs, uses more transmitters and receivers to increase the channel capacity, spectral efficiency, and bandwidth without increasing the transmit power. The main objective of this work is to minimize delay and power consumption in the MIMO-OFDM communication system. The basic MIMO system consists of sending and receiving antennas, as shown in *figure 1*.

The MIMO OFDM transceiver, implementing the IFFT/FFT, requires more memory references to compute the butterfly diagram and twiddle factors that increase the cost and power consumption. The long delay in the MIMO OFDM also increases the inter-symbol interference (ISI).

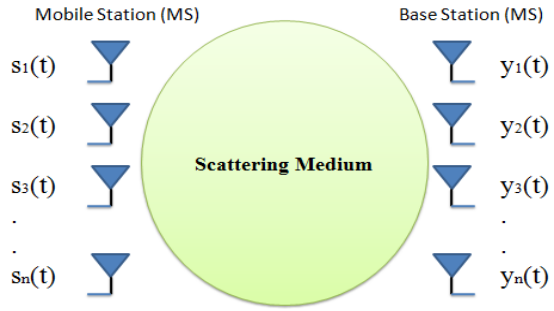

Figure 1: Basic structure of MIMO

This new proposed system, named as Integrated Massive MIMO Systems (IMMS) for Fast Fourier Transform (N-Point FFT)/ IFFT processor hardware is implemented with the help of Xilinx Software and their development boards.

M-MIMO (Massive-MIMO) technology could be a core component of the 5G New Radio (NR), which consists of excessive antennas at the bottom station to boost range and transmit energy efficiencies. At the same time, the additional antennas will help to improve the vast improvements in efficiency, power, throughput, and delay.

Due to high energy efficiency, OFDM guard bands dominate in implementing the 5G new radio structure. The massive MIMO technology is also essential in leading upcoming challenges the citizens' face, including using cheap, low-power components,

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low delay, and transcription of the MAC layer. To design an FFT processor that can be used in the communication systems to reduce the delay as much as possible. This paper acts as a point of convergence on designing the N-point FFT (Fast Fourier Transform) and achieving the term Low Latency. The N point FFT will be implemented by using Xilinx software for good communication between users with reduced delay.

Massive MIMO is a5G communication technology in which base stations are made with advanced antenna elements to enhance spectral and energy efficiency. It has an intelligent range design to achieve high output, communication reliability, and user density in large MIMO 5G communication systems. It utilizes spatial signal processing techniques, including beam forming.

In an OFDM system, it modulates the original symbol with a time period of Ts but this time period length has been extended to T_{sym}= NTs by transmitting N symbols in a parallel form. So, a considerable part of latency is introduced by OFDM (de)modulation in MIMO systems.

To address the low-latency demand of integrated bulk MIMO systems, the Fast Fourier Transform (N-Point FFT) processor and related sequence scheme are proposed, which reduce the processing computation delay and sequence of OFDM-based systems, respectively.

2. SYSTEM MODEL

In Massive MIMO systems, a Fast Fourier Transform processor was proposed and identified in a Low Latency FFT/IFFT Architecture for Massive MIMO Systems [1], reducing the computational processing delay, latency, and reordering the latency of OFDM- Receiver systems. Chip layout 2048-pt FFT has been developed using CMOS Technology in 28 nm. Mainly presented and set on latency reduction scheme was developed respectively [1]. Multi-User MIMO offers significant compensation more than conventional end-to-end MIMO [2]. The large MIMO networks can be enabled with Ultr end-to-end and Low-Delay Communication Mm-Wave [3].

Reduced the edge effect DFT based channels and computational complexity using FFT and channel estimation for uplink Massive MIMO systems [4]. Each subcarrier uses only two specific ZF and LMMSE operations and FFT operations. On the other hand, the difficulty of evaluating the equalizer coefficients only requires the information of the derivatives of the corresponding channel frequency response [5]. Ultra-Reliable and Low Latency Communication in mm Wave-Enabled Massive MIMO Networks [6] proposed a scalable framework for the Down Link pilots design, Down Link CSI acquisition, and the parallel CSI feedback in the Up Link, concentrated on FFT-based pilot and FDD mode. Finally proposed and designed an FFT-based pilot scheme [6].

The wavelet-based MIMO OFDM system is designed and compared with the FFT-based MIMO OFDM systems, and concluded that the BER is improved for their proposed system [7]. The main drawbacks of CDMA can be overcome by using IDMA, which can be easily integrated with MIMO OFDM and improves the BER [8]. With the help of MATLAB, Simulink analysed the MISO and MIMO OFDM, the MIMO which is increasing the performance of the receiver [9].

The hardware implementation of the MIMO OFDM system is developed, and a physical layer link is implemented in Xilinx FPGA with partial reconfiguration [10]. The computational design complexity and power consumption can be reduced by designing mixed Radix 4/2 with bit reversal architecture proposed with minimal hardware and less power consumption [11].

To increase the throughput and less power consumption, they proposed the FFT structure is the grouping of memory reference decrease method with binary scaling technique and Radix-4 booth multiplier. The proposed system performs better in BER and SNR [12]. Massive MIMO and Multi-User MIMO System for future generation wireless systems than pt. to pt. communication. An essential part of this paper focuses on the large potential of large MIMO systems that enable technology for the future beyond 4M cellular systems. The scheme offers a wide range of benefits regarding energy efficiency, spectral efficiency, visibility, and reliability [13]. Mainly concentrated on a highly efficient programmable fast Fourier transform (FFT) processor designed for supporting variable points, Fast Fourier transforms, and discrete Fourier transforms (DFTs) [14]. The address production scheme for FPGA implementation of simple FFT by introducing an algorithm and hardware to recreate the tweed factors for FFT Radix-2 multiplication [15].

It mainly focuses on designing the FFT (fast Fourier transforms, and also it can achieve total hardware butterfly efficiency and reduce the number of adders. Implemented FFT Processor using Viterbi algorithm and concentrated MDC- Multi Path Delay commutator basic architecture [16]. A split-radix fast Fourier transform (SRFFT) pipeline architecture design. They have used the Cooley–Tukey-based algorithms for designing, which are regular and extensible for any 2^n –point [17]. The 8192 pt. is designed for Sequential input and output FFT Chip. Here new radix technique 22 x 22 FFT algorithm is introduced for data partition and allocation of data. These 8192 chips are mainly used in DVB- Digital Video Broadcasting applications. The clock rate of 8MHz, Chip area, and supply voltage of 1.33 is measured in A Combined SDC-SDF Architecture for Normal I/O Pipelined Radix-2 FFT [18]. They introduced new technology, *i.e.*, MDC- Multipath delay commutator for implementing the FFT Processor of MIMO-OFDM. Here analyse the performance and complexity of the FFT Processor. Finally achieved 100% utilization rate for implementing FFT processor and concentrated on Energy consumption and chip area [19-20]. Understanding MATLAB SIMULINK & Xilinx EDA tool environment; programmed chips are used for 6T Static Random-Access Memory cell, the approach of FFT for frequency domain, delay & latency observations and Coding of VHDL using Xilinx [21-31].

3. PROPOSED SYSTEM

The proposed architecture is implemented to style the Fast Fourier Transform in memory base and pipelined architecture.

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In memory base architecture, no. of processing elements is very high. This might get a protracted-lasting delay, but our main aim is to get the Fast Fourier Transform processor with a very low delay.

The pipelined architecture has high throughput and low delay, and the price is affordable. So, we've designed this idea in a hardware kit with FPGA Spartan F3. An N point FFT processor has been designed with FPGA Spartan F3 kit, and it may be used anywhere within the communication systems.
The block diagram is shown in *figure 2*.

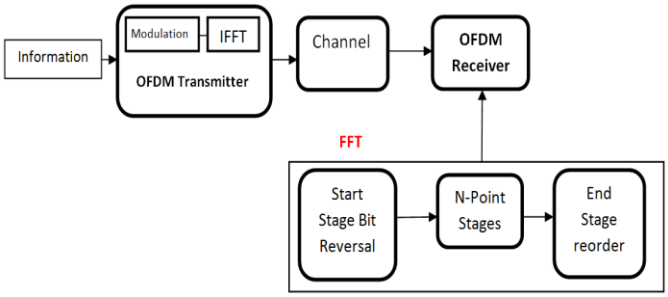

Figure 2: Proposed Structure of Communication Network using N-Point FFT Block Representation

Figure 2 shows the N point FFT processor to get the low latency and low power consumption by directly converting the Simulink block into required HDL synthesis code.

In this proposed system, the delay and memory usage of N point FFT has been calculated by using both VLSI software and MAT lab simulation. Using the proposed scheme (Massive MIMO), N-point FFT/IFFT processor design achieves a better throughput and lowest latency than for single –input pipelined FFT/IFFT architectures.

4. THE METHODOLOGY OF THE PROPOSED SYSTEM

The OFDM (Orthogonal Frequency Division Multiplexing) guard bands help to minimize the channel noise and also to produce the error free channel and it consists of multiple arrays of antennas at the transmitter and also at the receiver,

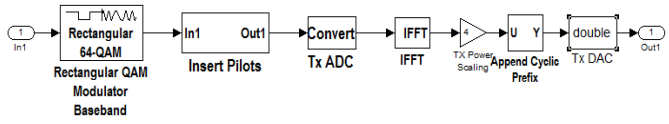

Figure 3a: Block diagram of OFDM transmitter

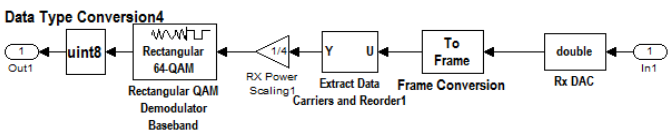

Figure 3b: Block diagram of OFDM receiver

4.1 Proposed Less Computational Delay for FFT

The main aim of this proposal is to get low latency, less computations and low cost while converting the time domain signals to frequency domain. The following figure shows the VLSI architecture to get reduced delay for different stages of butterfly effect.

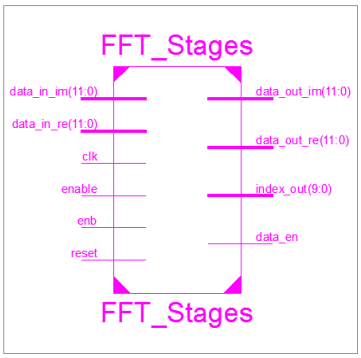

Figure 4: VLSI Architecture for reduced delay for Different Stages of Butterfly

The *figure 4* shows, the reduced delay architecture for different stages of FFT.

In FFT, the twiddle factor can be calculated by reversing the bits. The reordering scheme starts depends on the index value.

For an N point FFT, the twiddle factor is given in the *equation 1*.

$$W_N = e^{-j\frac{2\pi}{N}} \text{----- (1)}$$

In the *equation 1*, W_N represents the twiddle factor and N is the number of bits. The FFT and IFFT representation of the given time domain signal is given by *equations 2 and 3*.

$$X_K = \sum_{i=0}^{N-1} X_i W_N^{ki} \ , 0 \le k \le N \text{ ----- (2)}$$

$$x_i = \sum_{k=0}^{N-1} X_k W_N^{-Ki}, 0 \le k \le N \text{ ----- (3)}$$

Equation 2, 3 indicates the inputs where, "i" is the sample index and K is the subcarrier index.

The N point FFT has been designed using MATLAB Simulink and is converted directly into HDL synthesis to calculate the delay and number of clock cycles. The *figure 5* shows the HDL synthesis of N-point FFT.

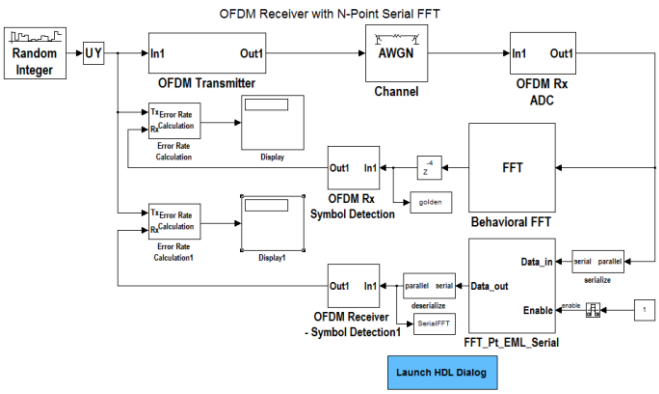

Figure 5: Proposed Structure of N-Point FFT MATLAB - Simulink Block

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The designed block diagram as shown in the *figure 5*
The HDL code conversion and code execution are shown in *figure 6a* and *6b*.

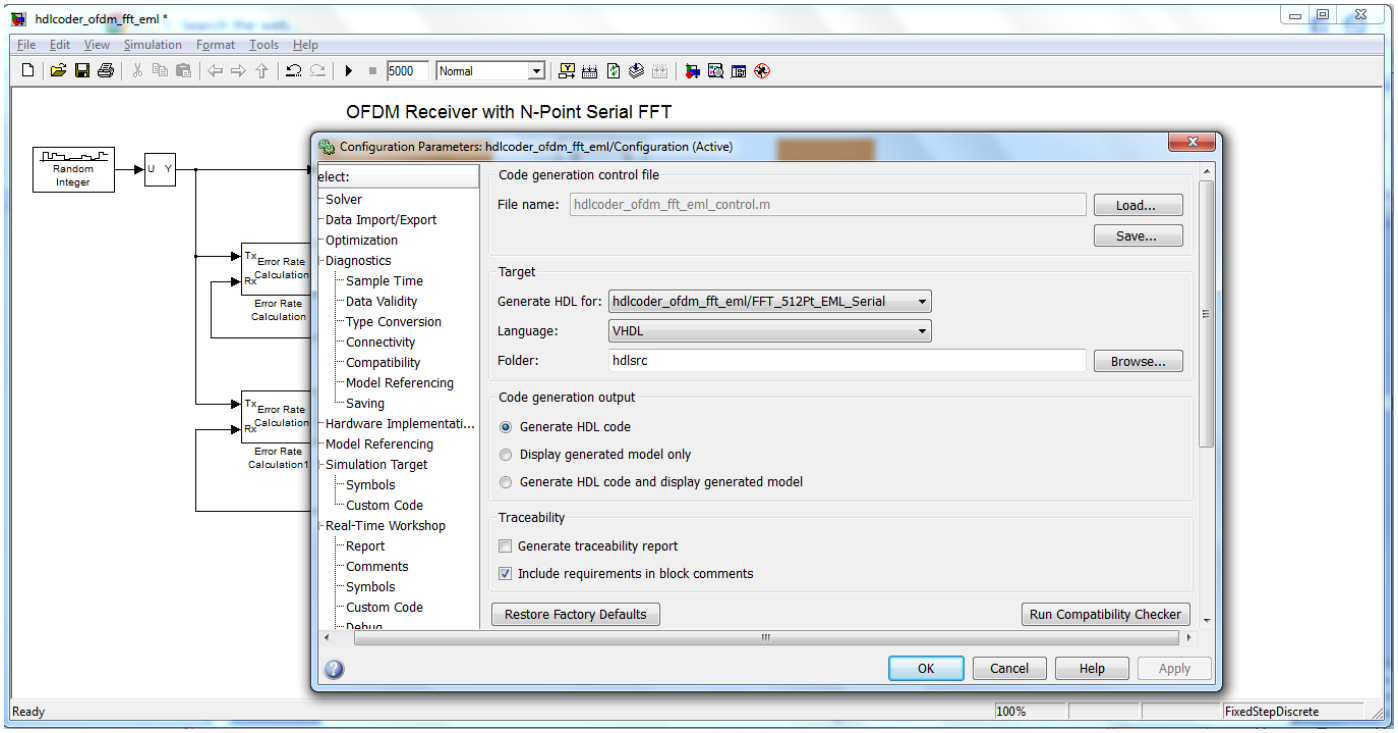

Figure 6a: HDL Code conversion in MATLAB-Simulink

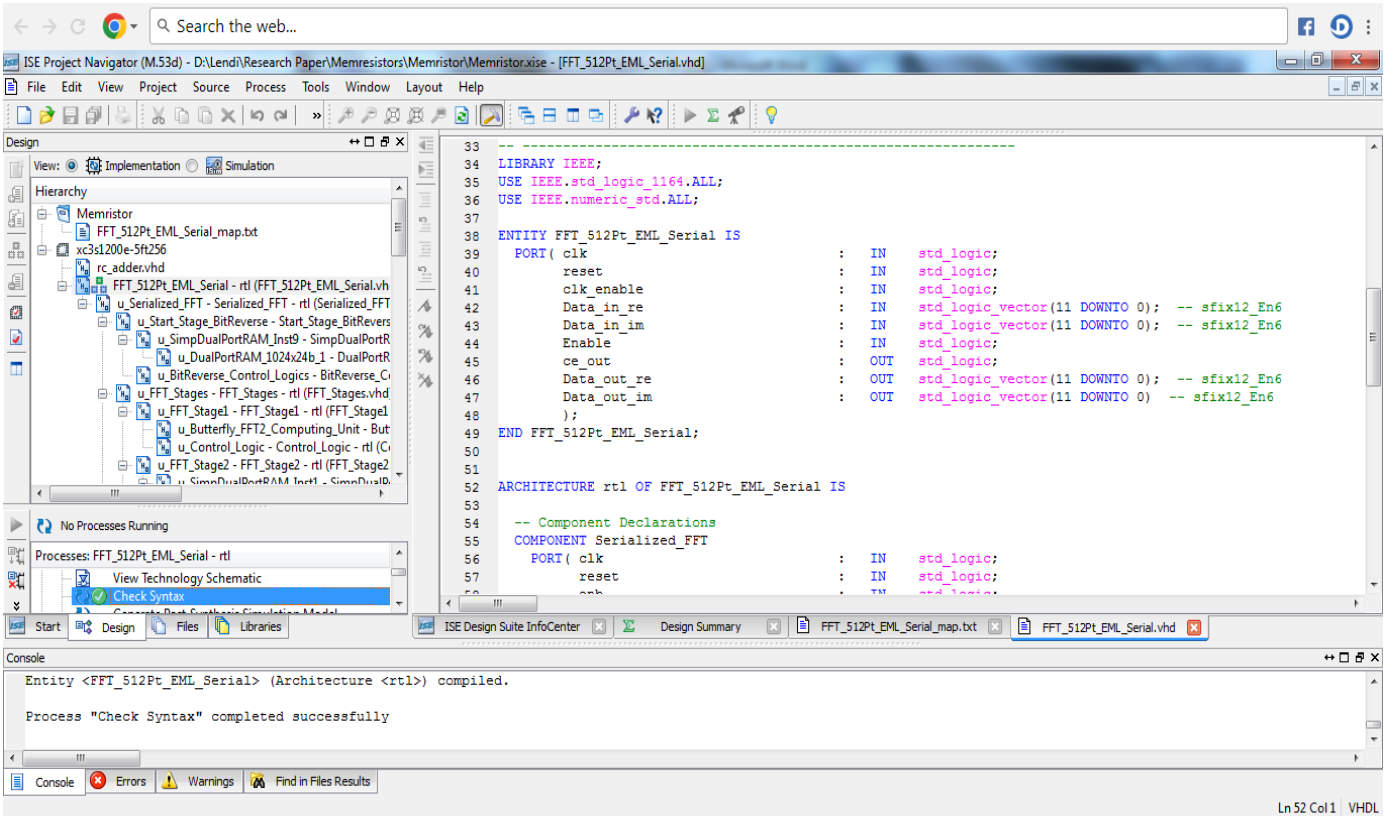

Figure 6b: HDL Code Executing in Xilinx

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Figures 6a and *6b* are the HDL code conversion and code execution in N point FFT using MATLAB Simulink.

4.2 Cooley–Tukey Fast Fourier Transform algorithm

Among so many existed algorithms, in the proposed system, Cooley-Tukey FFT algorithm has been used because of reduced computations and also easily implemented in Verilog. The calculation of twiddle factor involves computational algorithms. But in the Cooley Tukey algorithm, no of additions and multiplications for all of them is simply NlogN, so the speed and execution time will be very less in this algorithm. This algorithm uses the periodic properties of the sine and cosine function to implement the butterflies.

Step 1: Start the Implementation.

Step 2: Give the Input values

Step 3: Select the point of the FFT and for which you are designing.

Step 4: To compute the FFT, the FFT enable value should always equal to 1

Step 5: Take a condition that if operating mode value is 0 if this condition is true then start the FFT computation otherwise store the outputs.

Step 6: If it is true the output must be bit reversed otherwise stop the execution.
The *figure 7* shows the flow chart implementation of algorithm. The process is as follows

Flow Chart of FFT Algorithm

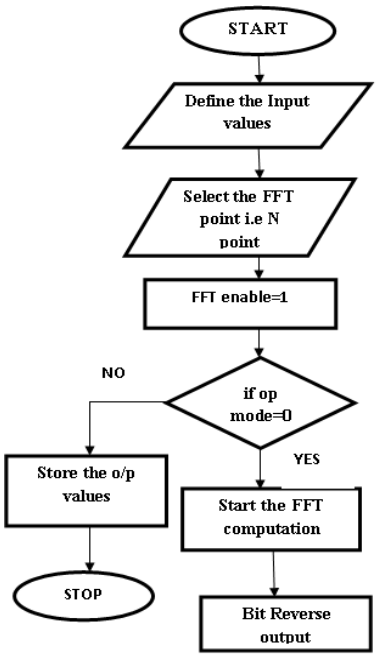

Figure 7: Flow Chart of FFT Implementation

5. RESULTS

Below figure shows that designing of N- point FFT as there are n stages.

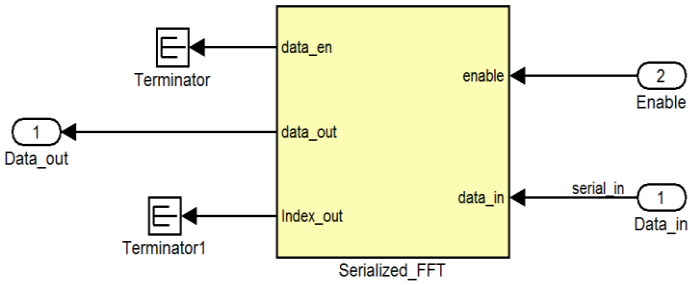

Figure 8a: Schematic structure of N point FFT

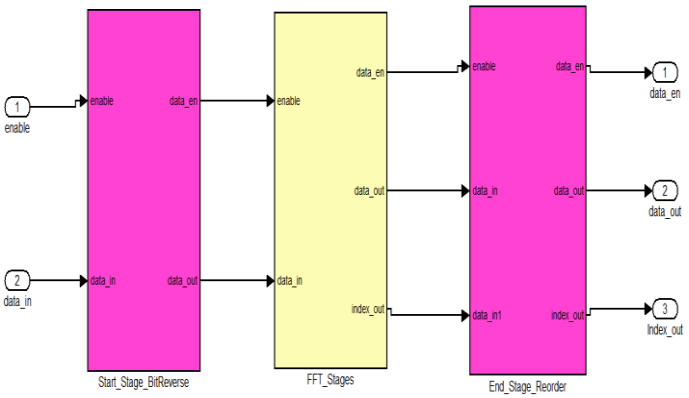

Figure 8b: Three stages of FFT

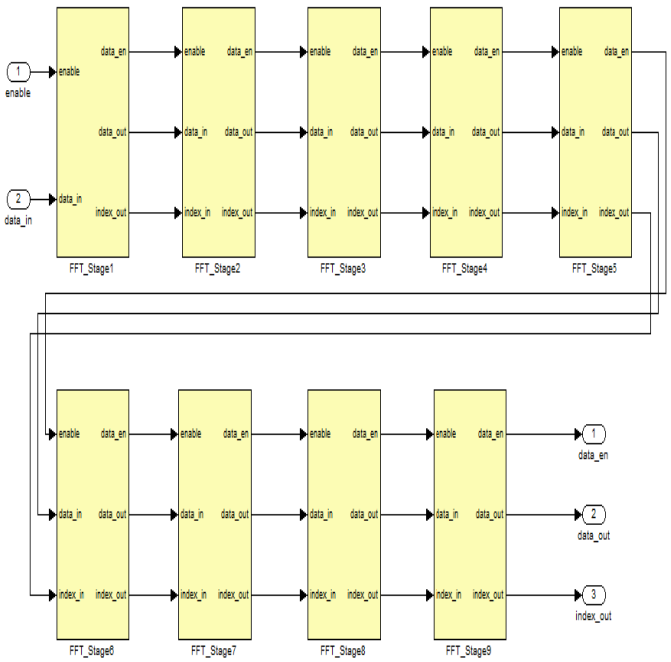

Figure 9: Block diagram representation of FFT N- stages

The 8-point representation of FFT is as shown in the figure.

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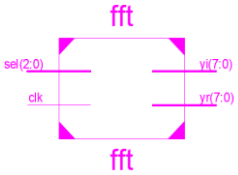

Figure 10: Schematic diagram of 8-point FFT Top Level Block

Figure 9 illustrates the 8-point FFT implementation

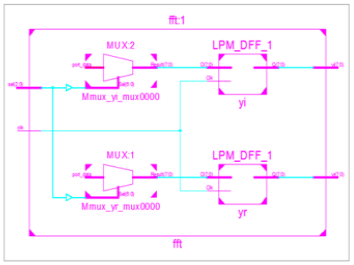

Figure 11: RTL schematic of 8pt FFT

Figure 11 represents the RTL schematic diagram of the 8point FFT.
For an eight-point FFT, there are 3 butterfly stages and each stage are calculated and obtained results as shown in the *figure 1*.

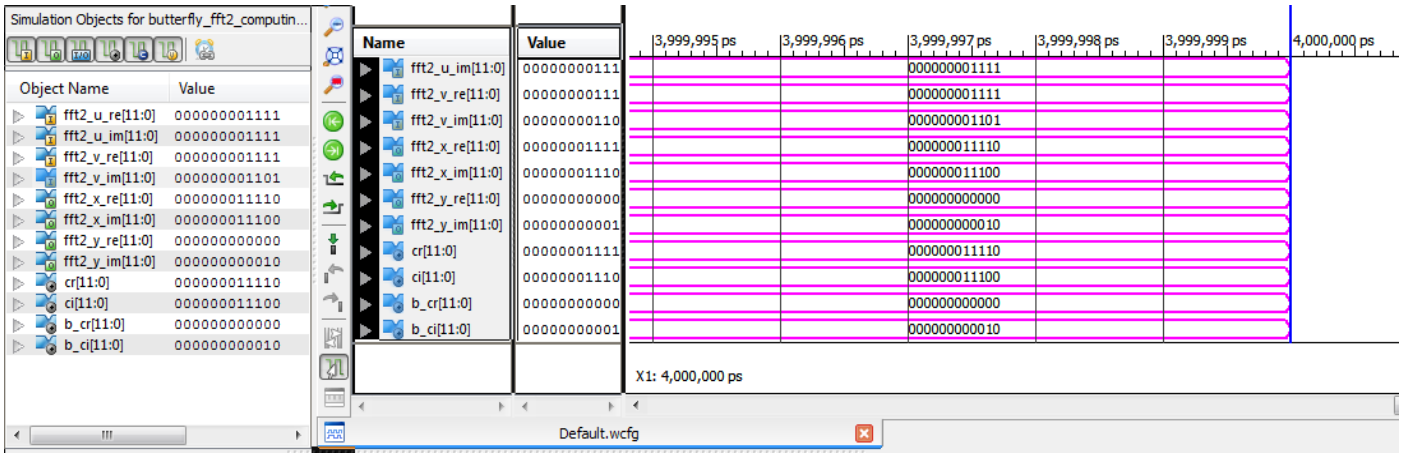

Figure 12: Timing Diagram of 8 POINT FFT

Table 1: Final Report of Design Statistics of 8 pt. FFT

S. No	Particulars	Count
1.	IOs	20
2.	BELS	39
3.	AND2	6
4.	AND3	5
5.	INV	12
6.	OR3	8
7.	OR4	5
8.	OR5	1
9.	OR6	2
10.	Flip Flops/Latches	16
11.	IO Buffers	20
12.	IBUF	4
13.	OBUF	16

And we have estimated the latency of above point and we have observed that maximum delay occurring at the time of the designing is 0.003ns. For 64-point FFT is implemented and the corresponding designing, RTL schematic, timing diagram and final report is shown in below *figure12*. *Figure 13a* shows the schematic diagram of 64-point FFT

In the below figure there are 6 butterfly stages and each and every stage we have designed each and every stage and finally got the result as observed in the below figure.

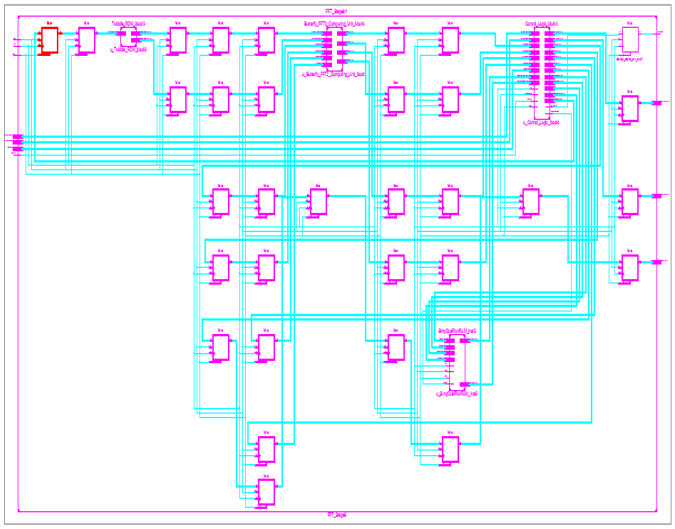

Figure 13a: RTL Schematic of 64 Point FFT

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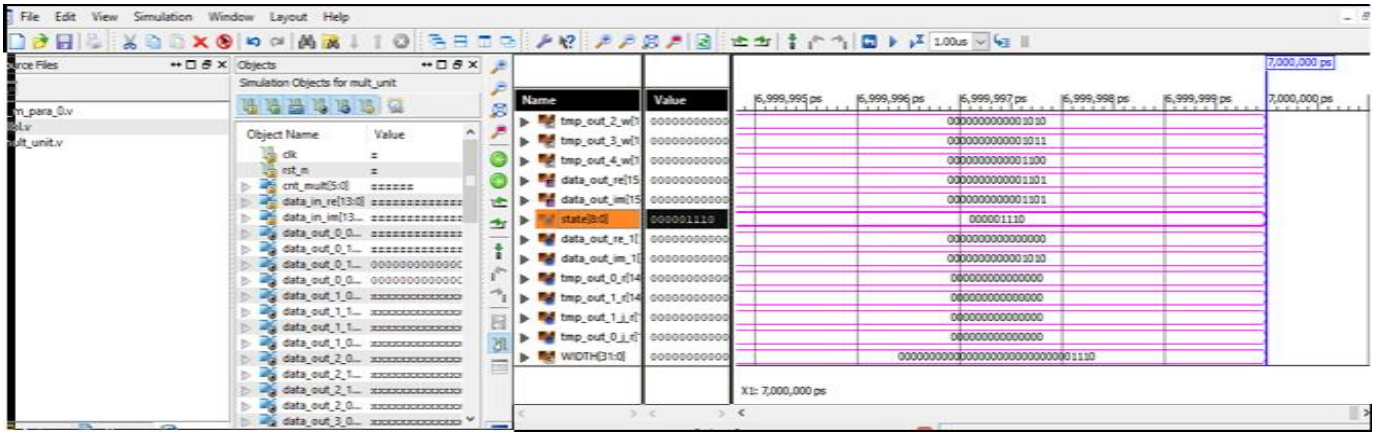

Figure 13b: Timing Diagram of 64 Point FFT

In final report we have observed the following results

Table 2: Final Report of Design Statistics of 64 pt. FFT

S. No	Particulars	Count
1.	IOs	68
2.	BELS	16656
3.	AND2	5385
4.	AND3	412
5.	AND4	37
6.	AND5	63
7.	AND6	2
8.	INV	4113
9.	OR2	3557
10.	OR3	106
11.	OR4	30
12.	XOR2	2951
13.	Flip Flops/Latches	32
14.	FDC	32
15.	IO Buffers	68
16.	IBUF	36
17.	OBUF	32

And we have estimated the latency of above point and we have observed that maximum delay occurring at the time of the designing is 0. 054ns.Now we have implemented the 512 point and the corresponding latency calculation, designing and the RTL schematic is shown in below figures.

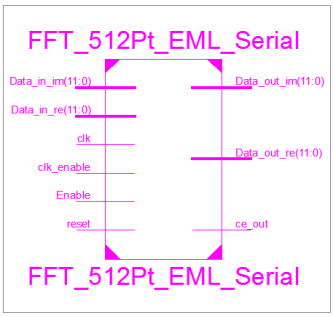

Figure 14: 512 Point FFT Top Level Block

In the below figure there 9 butterfly stages for each and every stage is designed and finally we got the results as shown below. To calculated the time delay as shown in the below figure it is in nanoseconds,

Table 3: Analysis of Delay

S. No	Particulars	Delay
1.	Minimum input arrival time before clock	6.24 ns
2.	Minimum output arrival time after clock	5.962 ns
3.	Maximum combinational path delay	5.464 ns

Table 4: Comparison Results of Latency for FFT Processors with existing models

S. No	Particulars	Delay
1.	JSSC [30]	102.4 µs
2.	TVLSI [16]	51.4 µs
3.	TCAS-I [31]	4.11 µs
4.	Existing Model [1]	4 µs
5.	Delay of Proposed Work	5.464 ns

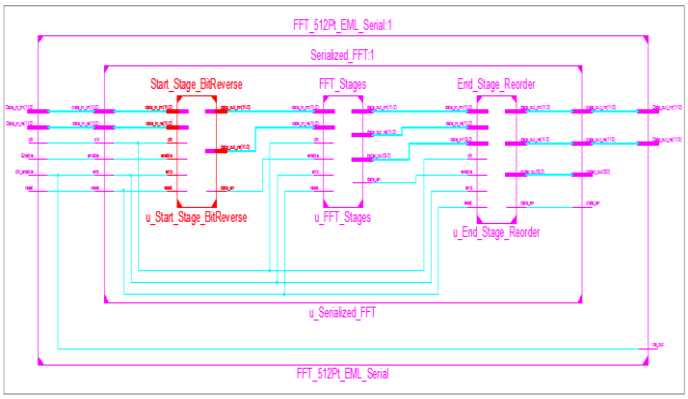

Figure 15: RTL Schematic of 512 pt. FFT with Serialized Stages

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6. HARDWARE IMPLEMENTATION

The hardware implementation of our proposed work was done on FPGA Spartan 3 as shown in *figure 16*. The FPGA kit acts as a N bit processor and can be easily used in any communication systems.

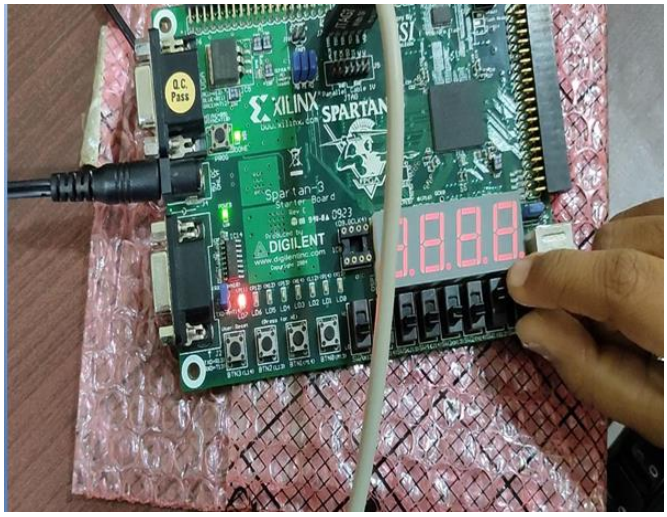

Figure 16: The implementation of N point FFT on FPGA SPARTAN 3 KIT

7. CONCLUSION AND APPLICATIONS

In this paper, VLSI implementation of integrated Massive MIMO systems for N point FFT has been Proposed. This proposed system utilizes the chip routing technology at every moment to obtain the latency in 5.464 nanoseconds compared with existing models as mentioned in *table 4*. and the no. of computations and the clock cycles are reduced. Finally, this proposed system has been implemented in VLSI integrated circuits such as FPGA Spartan 3e. This can be used in the 5G Communication for good Transmission and Receiving with low latency and less complexity.

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