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International Journal of
Electrical and Electronics Research (IJEER)
Survey Article | Volume 10, Issue 4 | Pages 1191-1198 | e-ISSN: 2347-470X

A Comparative Analysis of FinFET Based SRAM Design

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ABSTRACT- FinFETs are widely used as efficient alternatives to the single gate general transistor in technology scaling because of their narrow channel characteristic. The width quantization of the FinFET devices helps to reduce the design flexibility of Static Random Access Memory (SRAM) and tackles the design divergence between stable, write and read operations. SRAM is widely used in many medical applications due to its low power consumption but traditional 6T SRAM has short channel effect problems. Recently, to overcome these problems various 7T, 9T, 12T, and 14T SRAM architectures are designed using FinFET. This article provides a comprehensive survey of various designs of SRAM using FinFET. It offers a comparative analysis of FinFET technology, power consumption, propagation delay, power delay product, read and write margin. Additionally, the article presents the simulation of the 5T and 6T SRAM design using CMOS and FinFET for 14 nm technology using Microwind 3.8 simulation tool. The outcomes of the proposed SRAM design are compared with several recent designs based on power, delay, and, and various stability analysis parameters such as read, write and hold noise margin. Finally, the article discusses the challenges in SRAM design using FinFET and provides the future direction for optimization of accuracy, area, speed, delay, and cost of the FinFET-based SRAMs.

Keywords: FinFET Technology, Static Random Access Memory (SRAM), Very Large Scale Integrated Circuits, Device Circuit Co-optimization.

ARTICLE INFORMATION
Author(s): Vijayalaxmi Kumbar and Manisha Waje;
Received: 08/07/2022; **Accepted**: 06/12/2022; **Published**: 25/12/2022;
e-ISSN: 2347-470X;
Paper Id: IJEER220716;
Citation: 10.37391/IJEER.100468
Webpage-link:
https://ijeer.forexjournal.co.in/archive/volume-10/ijeer-100468.html

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1. INTRODUCTION

In today's world, many memory cells are available such as Dynamic Random Access Memory (DRAM), SRAM, Ferroelectric RAM (F-RAM), Phase change RAM, etc. Due to technology scaling power consumption and speed plays a very important role in their use in digital circuits. As per Moore's law number of transistors doubles about every two years. This law has led to technology scaling to enhance the different performance parameters such as area, power, and speed. The geometric scaling of metal and through routing, in addition to transistor scaling, boosts the back-end wire RC load, reducing SRAM operating speed dramatically [24].

A well-designed SRAM cell has excellent integration density and stability. The read, write and hold static noise margin (SNM) terms are used to describe the stability of SRAM during read, write and hold operations, respectively. In SRAM cell design, integration density and device stability are conflicting factors. Augmenting the size of the SRAM cell to increase stability usually means lowering the integration density [32].

Scaling traditional MOSFETs below 50 nm, fabrication is difficult [35]. It is not expected to design a 6T SRAM with a gate resistance of less than 45nm because MOSFETs have a greater gate resistance, which induces unregulated flickering noise [16]. FinFETs give a better solution to short-channel electro-static effect, sub-threshold leakage, ability to operate at low voltage, lower variability due to doping variability, and higher device parameter variability [42][43][44].

The separate front and rear gates can be biased differentially to regulate the device threshold voltage and the current is one of the most essential aspects of FinFETs. SRAM cells can be deliberated for low power consumption by regulating the back gate of FinFETs [33] [6].

This paper provides a comprehensive survey of various recent FinFET-based SRAM designs. It provides the comparison of the various performance parameters of SRAM design using FinFET that need to be considered while choosing various applications. It focuses on the technology used for the SRAM design, various performance metrics, and merits and demerits of the design to conclude the basic findings from the survey.

The remaining article is arranged as follows: *Section 2* describes SRAM design. *Section 3* offers a brief discussion about various FinFET devices utilized for the SRAM design. *Section 4* gives a review of various SRAM designs using FinFET and a discussion on the comparative analysis of its performance metrics. Lastly, *Section 5* concludes the article and provides the future direction for the optimization of various attributes of SRAM design using FinFET.

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2. STATIC RANDOM ACCESS MEMORY DESIGN

With the growth of CMOS technology, traditional 6T SRAM faces issues with leakage current and device stability, hence multiport SRAM was introduced. FinFETs have several advantages compared to MOSFETs, including improved Ion/Ioff, lesser power consumption, and faster switching speeds. Furthermore, it has solved the MOSFETs' scalability restrictions. The three operating modes of the FinFET are Low Power (LP) mode, Shorted Gate (SG) mode, and Mixed LP-IG mode. The SG model is similar to a MOSFET; however, the LP model is well suited to low-power applications [7] [8].

The traditional structure of 6T SRAM using FinFET is illustrated in *figure 1*. The 6T SRAM stores one bit. It consists of two inverters (T1, T3, and T2, T4) connected back-to-back and access transistors (T5 and T6). The T5 and T6 are enabled through the write line. The bit-line and inverted bit-line are used for read and write operations. It performs three important operations: hold, read and write [30] [25]. Various SRAM structures such as 5T-SRAM, 7T-SRAM, and 8T-SRAM are illustrated in *figure 2-4* respectively.

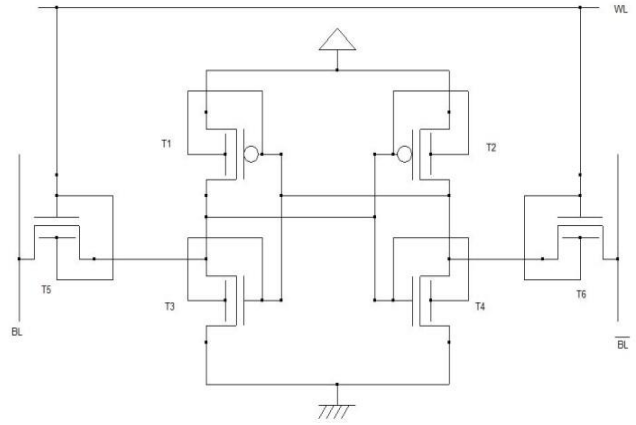

Figure 1: Conventional 6T-SRAM circuit

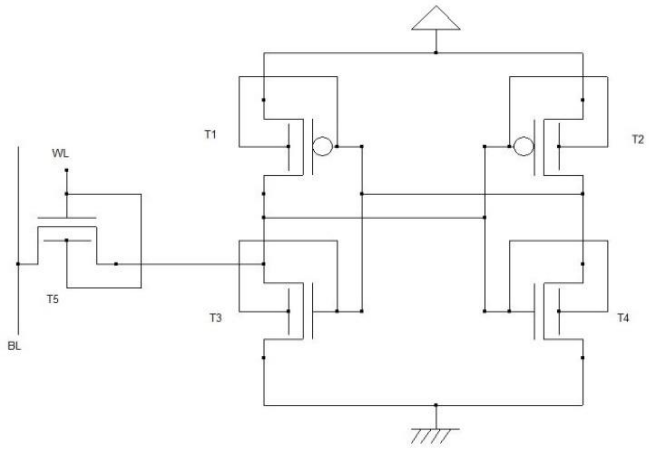

Figure 2: 5T-SRAM circuit

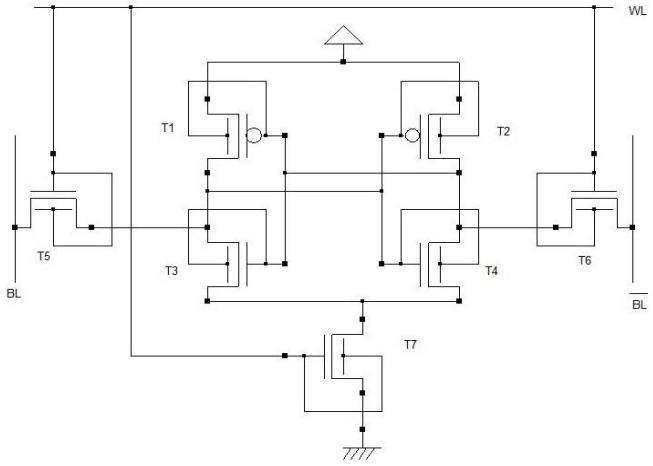

Figure 3: 7T-SRAM circuit

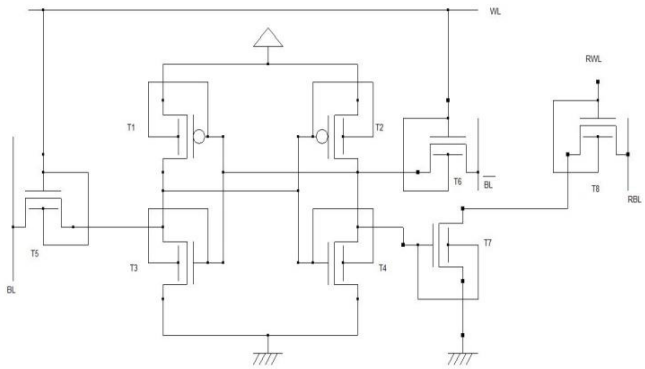

Figure 4: 8T-SRAM circuit

If word line (WL=1), then both the access transistors will be in the ON state and it is feasible to attain both write and read operations. If WL=0, then both the access transistors will be in the OFF state and it performs a hold operation. When we want to write into the memory, the bit line (BL) and BL Bar will act as input and vice versa during the read operation as described in *table 1*.

Table 1. SRAM Hold, Read, and Write operations

HOLD Operation	READ Operation	WRITE Operation
Write Line =Logic '0'	Write Line = Logic '1'	Write Line = Logic '1'
M5 & M6 are in OFF State	M5 & M6 are in ON State	M5 & M6 are in ON State
	BL & BL Bar acts as outputs	BL & BL Bar acts as inputs

The performance of the SRAM is assessed using several performance measures like power dissipation (static, dynamic, short-circuit), propagation delay, and power delay product as shown in equations 1-5. Power dissipation is one of the important parameters while designing the memory that decides its application and should be minimum for bio-medical applications. FinFET helps in reducing power consumption.

$$P_S = I_{leakage} \times V_{DD} \quad (1)$$

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$$P_D = \frac{C_L \times V_{DD}^2}{t_p} \quad (2)$$

$$P_{SC} = \frac{\beta}{2}(V_{DD} - 2V_t)^3 \frac{t_{rf}}{t_p} \quad (3)$$

$$T_p = \frac{T_{pLH} + T_{pHL}}{2} \quad (4)$$

$$PDP = P \times T_p \quad (5)$$

Where $I_{leakage}$ stands for leakage current, V_{DD} is the supply voltage, T_{pLH} is low to high propagation delay, T_{pHL} is high to low propagation delay, T_p denotes propagation delay, P_s represents static power dissipation, P_D represents dynamic power dissipation, P_{SC} depicts short circuit power dissipation, and PDP provides power delay product.

3. FinFET CONFIGURATIONS

The FinFETs are majorly classified into four groups depending upon the gate structure, shape of a gate, number of gates, and fabrication platform as given in *figure 5*.

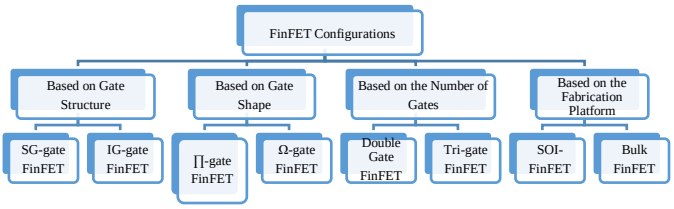
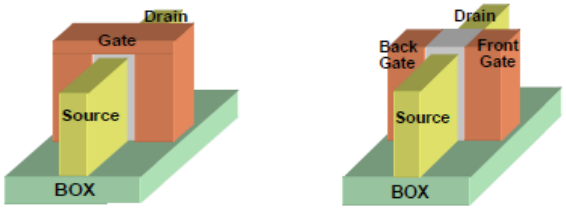


Figure 5: Categorization of FinFET Configurations

3.1 Shorted Gate FinFET (SG-FinFET) and independent gate FinFET (IG-FinFET)

The FinFETs are categorized into two types based on the gate structure such as SG-FinFET and IG-FinFET as illustrated in *figure 6*. The SG-FinFET and IG-FinFET are often recognized as 3-terminal (3T) and four-terminal (4T) devices [31] [1]. The rear and front gates of SG FinFETs are both physically shorted, whereas the gates of IG FinFETs are physically isolated [45]. Therefore, in SG-FinFETs, both gates are employed to control the channel electrostatics.



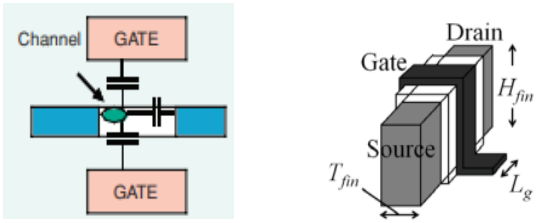
(a) (b)

Figure 6: FinFET configurations (a) SG-FinFET (b) IG-FinFETs [29]

SG-FinFET-based designs provide superior performance because of lesser delay compared with IG-FinFET [34]. IG-FinFET-based designs result in more delay because of the uneven structure of pull-down and pull-up transistors. It is preferred for low-power-consuming devices [28]. IG-FinFET is a better choice for increasing cell stability. It is concluded that in DG IG-FinFET, due to controlling both gates independently, cell stability of 6T SRAM cell increases. The leakage current is lower in the case of the DG IG-FinFET SRAM cell [26].

3.2 Double Gate and Tri-gate FinFET

Based on the number of gates the FinFETs are categorized into the double-gate and tri-gate FinFET devices. In double-gate (DG) FinFETs, the two gates are arranged opposite each other. This structure is preferred for controlling short-channel effects (SCEs). In tri-gate FinFET, the gate electrode is wrapped over 3 sides of the fins. *Figure 7* shows the structure of double and tri-gate FinFET devices.



(a) (b)

Figure 7: FinFET configurations a) Double-Gate [18] b) Tri-Gate FinFETs [20]

DG FinFETs are popularly used for SRAM applications since it efficiently boosts threshold voltage and thus improves static noise margin and write margin [9]. Tri-gate FinFET-based SRAMs are used in complex designs and high-performance devices [17].

3.3 π-gate FinFET and Ω-gate FinFETs

Depending upon the shape and structure of the gate, the FinFET devices are grouped into π-gate FinFETs and Ω-gate FinFETs. The comparative analysis of these FinFETs structures is illustrated in *figure 8*. In the π-gate structure, the number of effective gates is extended from three to four, which improves electrostatic integrity.

(a) (b)

Figure 8: FinFET configurations a) π-gate FinFET b) Ω-gate FinFETs [15]

In the π-gate structure, the gate structure looks like a pi shape. In the Ω-gate structure, the gate structure looks like the Ω structure. Multi-gate FinFETs are utilized for the smallest SRAM designs [4].

3.4 Silicon-On-Insulator (SOI) FinFETs and bulk Si FinFETs

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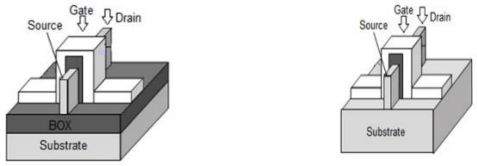
The FinFETs are classified into SOI-FinFETs and bulk Si FinFETs based on the fabrication platform as illustrated in *figure 9*. The SOI-FinFETs are fabricated on SOI wafers. It has an insulation layer (Buried Oxide layer) between the silicon substrate and fins. The bulk FinFET uses bulk silicon for fabrication. The SOI-FinFETs are used for analog applications that require high voltage gain. Drain-induced barrier-lowering effects are less bulk FinFET than SOI-FinFET as effective channel length approaches below 50 nm.



(a) (b)

Figure 9: FinFET configurations a) SOI-FinFET b) Bulk-FinFETs [15]

4. SURVEY OF FinFET BASED SRAM DESIGN

This section highlights the various implementations of the SRAM design using various configurations of the FinFETs. Raushan et al. (2020) [5] implemented the 12T and 14T SRAM using 22nm FinFET. Simulation results of Parameters like power delay product, power consumption, energy-delay product, and propagation delay using 22 nm FinFET are compared with traditional 12T and 14T SRAM. They have shown that average power consumption is increased and the delay of conventional SRAM is high compared to FinFET. So, they have significantly improved the performance of these parameters for both circuits. Rahebeh et al. (2020) [10] presented Reliable and High-performance Asymmetric SRAM using back-gate biasing ((RHABG). This 6T SRAM is based on the independent gate and tied-gate transistors. Here the SRAM cell uses the back-gate control method with built-in feedback to increase the soft error resilience, read performance characteristics, and reliability against aging effects. Mushtaq et al. (2020) [11] designed the 6T SRAM using low-power SG-FinFETs at 7-nm technology. The simulation results show that FinFET input-dependent technique minimizes the read and write leakage power dissipation by 32.08% and 13.50%, respectively. There is a reduction in average power. Duariet al. (2020) [12] proposed an 8T SRAM cell with low leakage and superior stability. The researchers depicted the effect of operating temperature variation on the device's stability. It provided a comparative analysis of leakage power of 6T and 8T SRAM for different supply voltages. The comparison gives better performance and improved leakage. Birla et al. (2020) [13] proposed 8T SRAM using the shorted gate and low power-independent gate mode FinFET. Simulation results of both modes are compared and measured. They demonstrated that a FinFET based SRAM with a low power-independent gate provides greater stability even at low supply voltages, and that power reduction increases as the supply voltage decrease. Sina Sayyah Ensan et al. (2019) suggested a 7T asymmetric single-ended SRAM cell [18]. Their design utilizes just one bit-line and minimizes the drain-induced barrier lowering (DIBL) effect in the readout path to minimize leakage power and total energy consumption. The suggested cell improves cell area, PDP, static and average power. Further, Sina et al (2018) [20] proposed an 11T SRAM using tri-gate 10nm FinFET technology. The offered cell minimizes average power, write delay, and power delay product as compared to the 9T single-ended SRAM cell. It also enhances the write static noise margin. Saxena et al. (2016) [22] proposed the design of 13T SRAM using FinFETs with a power gating technique. The simulation results are compared with 11T SRAM. This transistor layout is one of the most enticing alternatives to classic planar CMOS technology because of its improved gate controllability, low power consumption, and scalability. A. A. Kumar et al. (2019) [19] demonstrated a 6T SRAM based on FinFETs. According to simulation results, FinFET based SRAM has little leakage than planar SRAM. FinFET SRAM also has less standby leakage than conventional SRAM [21].

Girish and Shashikumar [36] developed a predictive search optimization algorithm to optimise FinFET/SRAM design structure (PAOD). This gives dynamic computing devices and applications exceptional fault tolerance. Mathematical methods allow the model to deliver meaningful findings with more simulation iterations in less time. Better convergence of FinFET/SRAM architecture makes this POAD cheaper than a recursive design. Huo et al. [37] used quantum physics to evaluate the 6T SRAM cell using 7-nm FinFET technology. Variation control, device design tradeoffs, materials band engineering, and device design are examined as a 6T SRAM cell affects seven critical device design parameters. Control gate length (Lg) and spacer thickness to raise delay 19.3%, reduce leakage 56.7%, boost read noise margin (RNM) 8.6%, hold noise margin 7.9%, and write margin 10.8%. (TSPC). High-speed SRAM cell designs should optimise architecture and auxiliary circuits. Sina Sayyah Ensan et al. [38] constructed a FinFET based single-ended low-power 7T SRAM cell.

This cell increased read performance by removing the storage node from the read route. Detaching the cross-coupled inverters' feedback loop boosts writing WSNM by nearly 7.7 times compared to an 8T SRAM cell. This cell employs one bit-line, reducing power consumption and PDP by 82% and 35%, respectively, compared to an 8T SRAM cell. Two 3-D monolithic FinFET-enabled 8T SRAM cell designs by Abdullah Guler et al. [39] reduced leakage current and improved read times. The FinFET-supported 8T SRAM cell was compared to 6T and 8T SRAM cells. The created cell has a footprint area 28.1% and 43.8% smaller, a leakage current 31.6% and 43.2% smaller, and a read time 53.2% and 29.0% lower than 6T and 8T SRAM cells, respectively. Andrew Carlson et al. [40] recommended FinFETs based SRAM to improve SRAM read and WM. FinFETs are the best option because to their scalability and ability to improve SRAM performance and yield *via* independent gating. Two cell designs with individually gated FinFETs were tested for read/WM and yield increases. FinFET-based 6-T SRAM cells with pass-gate feedback (PGFB) improve cell read stability without losing area.

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Asen Asenov et al. [41] simulated DTCO using 14 nm FinFET/SRAM. Draft-diffusion simulations calibrated to ensemble Monte Carlo simulations analyse the process and statistical variability space. Dataset processing and tool flow automation enable this. Process-statistical variability interactions have been extensively studied. A two-stage compact model captures process-statistical variability relationship. To close the DTCO loop, FinFET-based SRAM write and static noise margin sensitivity to cell design variability and factors is examined. The summary of various SRAM designs using FinFET configurations is described in *table 2*.

Table 2: Comparison of SRAM Design using FinFET

Author	Power Consumption	Propagation Delay	Power Delay Product
Raushan, R.K. et al. (2020) [5]	Improved by 99% compared to conventional SRAM	Improved by 79.2% compared to conventional SRAM	Improved by 99.7% compared to conventional SRAM
	Improved by 99% compared to conventional SRAM	Improved by 76.5% compared to conventional SRAM	Improved by 99.4% compared to conventional SRAM
Rahebeh Niaraki Asli et al. (2020) [10]	Least read power consumption	NA	NA
Mushtaq et al. (2020) [11]	Leakage Power: 10.68 µW for a read operation and 31.01 µW for a write operation	12.8 psec for a read operation and 13.98 psec for a write operation	SRAM read operation: 136.8 aJ SRAM write operation:195 aJ
	Leakage Power: 7.26 µW for a read operation and 26.5 µW for a write operation	18.01 psec for a read operation and 16.1 psec for a write operation	SRAM read operation: 129.6 aJ SRAM write operation:426.6 aJ
Duari et al. (2020) [12]	Leakage Power at 0.5 V conventional CMOS 5.63nW and FinFET 52.3pW Power at 0.9 V conventional CMOS 62.2nW and FinFET 572pW	NA	NA
Birla et al. (2020) [13]	The leakage power of SG SRAM for 0.5 V is 12.61 nW LP-IG SRAM is 8.92 nW	NA	NA
Sina Sayyah Ensan et al. (2019) [18]	Average Power: 1.77 µW	Read Delay: 394ps Write Delay: 318 ps	0.79 fJ
Ensan, Sina et al (2018) [20]	Average Power: 137.66 nW Static Power: 5.17nW	Read Delay: 491.8ps Write Delay: 230.46 ps	168.57 aJ
Saxena, Shilpa et al. (2016) [22]	Leakage Power : 0.096 nW	7.8 ns	0.7488 fJ
Agarwal S., Chandel R. (2022) [2]	NA	NA	PDP is 73% lower than traditional SRAMs design
Abbasian et al. [3]	3.74, 1.56, 4.59, 5.38, and 4.83 times lower leakage power than the 8 T, ST2, FC11T, MPPN10T, and ST12 bit-cells	NA	NA
Vallabhuni, R.R. et al. (2020) [14]	VDD = 0.1 V 7T: 0.001224 mW 8T: 0.001239 mW 9T: 6.99 mW 10T: 0.00308 mW	VDD = 0.1 V 7T: 0.2943 nS 8T: 0.915 nS 9T: 0.2255 nS 10T: 0.497 nS	VDD = 0.1V 7T: 0.003602 pJ 8T: 0.01135pJ 9T: 0.01 pJ 10T: 0.0153 pJ
Verma et al. (2019) [17]	Write mode 6T: 0.0236 µW 8T: 0.0268 µW 10T: 0.02696 µW	6T: 0.0219 nS 8T: 0.0383 nS 10T: 0.0385 nS	6T: 0.000516 fJ 8T: 0.001026 fJ 10T: 0.001037 fJ
M. A. Turi et al. (2020) [9]	Power saving is more but reduces the speed	NA	NA
G. Ravi Kishore et al. (2021) [4]	NA	33.28 pS	NA
N. Kaur et al. (2016) [26]	Write mode 6T: 2.4538 nW 10T: 138.82 nW Read Mode: 6T: 62.249 nW 10T: 24.52 nW	Write mode 6T: 60.069 nS 10T: 0.010403 nS Read Mode: 6T: 0.00049619 nS 10T: 0.00024056 nS	Write mode 6T: 147.40 aJ 10T: 1.4442 aJ Read Mode: 6T: 0.030887 aJ 10T: 0.0058986
Dani et al. (2015) [28]	Read Operation (9.45 nW for 7nm) Write operation (0.010 µW for 7nm)	Read Operation (1.51 psec for 7nm) Write operation (2.64 psec for 7nm)	Read Operation (0.0143 aJ for 7nm) Write operation (0.028 aJ for 7nm)
S. S.R. et al. (2017) [23]	Reduced leakage power	NA	NA
Verma et al. (2015) [27]	Write operation 7.561 nW Read Operation 1.709 µW	Write operation 20.55 nS Read Operation 21.44 nS	NA

5. SIMULATION RESULTS AND DISCUSSION

This section provides a simulation of the various SRAM technologies using the Microwind 3.8 layout simulator. The performance of these SRAM technologies is evaluated using propagation delay, power dissipation, and PDP. *Figure 10* shows the simulation results of the 5-T and 6-T SRAM cell layout using Microwind 3.8.

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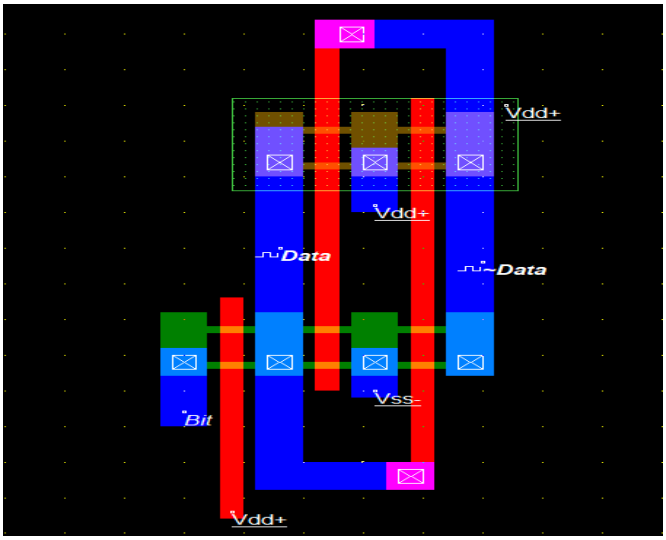
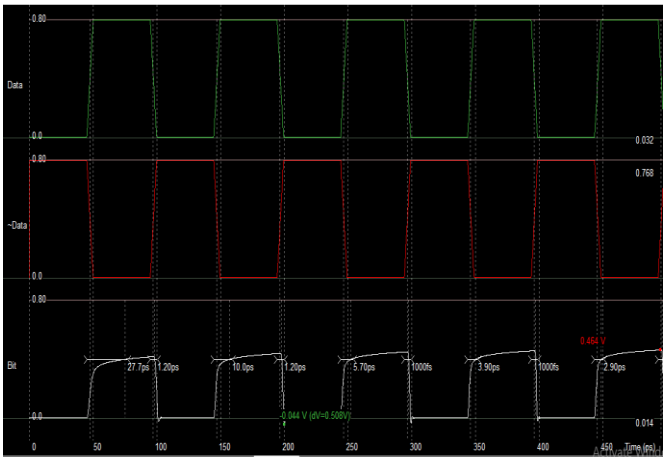
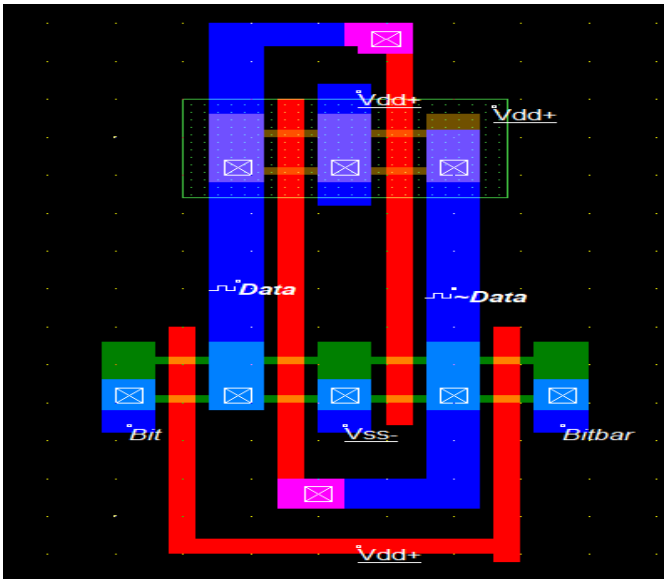


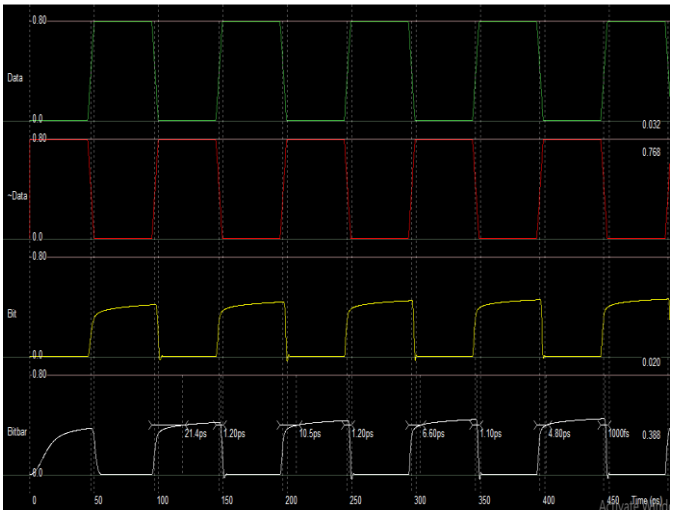
(a) 5T-SRAM layout design using Microwind



(b) Simulation results of 5T-SRAM



(c) 6T-SRAM layout design using Microwind



(d) Simulation results of 6T-SRAM

Figure 10: Simulations of 5T-SRAM and 6T-SRAM using Microwind

The performance of the 5T and 6T SRAM using FinFET are compared with traditional CMOS-based SRAM designs as given in *table 3*. It is observed that the FinFET-based SRAM designs provide lesser propagation delay, low power dissipation, and lower PDP. Also, the effectiveness of the proposed design is compared with traditional state of arts based on various stability factors such as read, write and hold static noise margin as described in *table 3*.

Table 3: Performance comparison of SRAM technologies

Authors	SRAM Type	Propagation Delay (nS)	Power Dissipation (µW)	PDP (W-sec)	Read SNM (mV)	Write SNM (mV)	Hold SNM
Banu et al. (2022) [1]	6T-SRAM	NA	0.016	NA	NA	NA	NA
Duari et al. (2020) [12]	6T-SRAM	NA	52.3E-6	NA	60	180	203
Verma et al. (2015) [27]	6T-SRAM	0.0219	0.0236	0.000516	140	235	NA
Mushtaq et al. (2020) [11]	6T-SRAM	0.02678	41.69	569.8	124.45	195	NA
Proposed Scheme	5T-SRAM CMOS	1.23	0.987	1.21e-15	35	68	80
	5T-SRAM FinFET	0.96	0.839	0.805e-15	45	70	95
	6T-SRAM CMOS	1.56	1.341	2.09e-15	80	96	115
	6T-SRAM FinFET	0.99	0.985	2.05e-15	155	315	250

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6. CONCLUSION AND FUTURE SCOPE

This article explains the necessity for and difficulty of optimizing different device aspects such as power, performance, area, speed, accuracy, and cost. This survey study provides a widespread survey of SRAM design using FinFET, its performance parameters, optimization methodologies etc. The FinFET-based SRAM designs provide a superior solution to the short channel electrostatic effect, sub-threshold leakage, low voltage operation, reduced doping variability, and more device parameter variability compared with a traditional single-channel standard transistor. It is observed that the FinFET based SRAM designs provides reduced power consumption, reduced delay, improved read, write and hold noise margin. Still, there is need for co-optimization of different parameters to improve the performance of SRAM memory cells. In the future, efforts might be expanded to reduce power dissipation, address the issue of variability, and enhance speed, power, area, and cost.

ACKNOWLEDGMENT

I would like to thank the management and Principal of Pimpri Chinchwad College of Engineering and Research, Ravet, Pune for providing me with continuous support for the research work.

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