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Design of Low Power and Process Control Hybrid Adder with Complemented Carry Structure

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ABSTRACT- A Hybrid logic style is most popular when compared to other logic styles in implementation of full adder circuits. Conventional hybrid adder uses truth table with true form of carry in and carry out. This will result in non-identical outputs of sum and carry for about 75% of the input combinations. Alternate truth table has been proposed to increase the similarity of sum and carry outputs. In this paper, circuit is designed for complemented carry in and complemented carry out of full adder. This novel structure allowed to design 20-T hybrid adder with process control, low power and low power delay product. The proposed adder structure is applicable for ripple carry adder. The performance of the designs is measured by simulating it in tanner T-spice environment using 0.25um technology. Proposed design has also been implemented up to 64-bit for its scalability. All the results were taken at several operating frequencies with varying word size of the adder. The proposed adder minimizes the power by 9.5%-51.5% and the power delay product by 3%-60% when compared to its counterparts for N-bit adder.

General Terms: Hybrid adder with ripple carry structure for wide word length.
Keywords: Adder, Complemented Carry, Process Control, Hybrid logic, Power.

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1. INTRODUCTION

Electronic system designers aim for low area, low delay and power efficient circuits. Arithmetic circuits are the basic building blocks of many electronic systems. Many of the arithmetic circuits like multipliers uses adders as a basic block [1]. In high-speed microprocessors, 33% of the power is consumed by the arithmetic circuits. To improve the performance of electronic system, adder performance needs to be enhanced [3]. Logic styles can be classified into classical and hybrid logic style. The complementary CMOS is an example of classical approach as in [3]. It gives full swing outputs against supply voltage scaling. Speed of the adder is degraded due to high input capacitance.

One more example in classical approach is complementary pass transistor logic as in [3]. This structure offers low delay and full swing outputs. Large number of internal nodes leads to high power consumption. One more classical approach in designing full adders is pass transistors. Pass transistor does not offer full swing at the outputs, when logic "1" is driven through NMOS and logic"0 is driven through PMOS. This issue can be resolved by transmission gate-based approach where the structure has PMOS and NMOS transistors in parallel with their gate inputs connected in true and complemented form. This structure offers weak driving capability and can be resolved by inserting buffers at the intermediate stages. [4] discussed about a system, a low power area reduced and speed improved serial type daisy chain memory register also known as shift Register is proposed by using modified clock generator circuit and SSASPL (Static differential Sense Amplifier based Shared Pulsed Latch). This latch-based shift register consumes low area and low power than other latches. There is a modified complementary pass logic based 4-bit clock pulse generator with low power and low area is proposed that generates small clock pulses with small pulse width.

Structure of the full adder is divided into three modules in hybrid design style [5-6]. Full output voltage swing is not produced in XOR/XNOR stage and level restorer is used to achieve it [7]. Hybrid style full adder performance is good as a single unit or for small word lengths. Driving capability is the limitation when word length is more [8]. Hybrid logic style is used for designing the full adders. Pass transistor logic is used for designing XOR-XNOR module in which sum and carry modules are realized using minimal size of a data selector [9]. XOR-XNOR outputs generated simultaneously using pass transistor logic and to design carry output complementary CMOS is used [10]. XOR-XNOR module is generated using feedback transistor, where sum is implemented using pass transistor logic and carry is implemented using minimal size data selector in low power and high-speed adder [11]. Various approaches are presented in recent years for developing XOR-

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XNOR circuits. In first approach, XOR is designed and not gate is cascaded to produce complemented XOR output.

This approach has a drawback of XNOR output gets delayed, which increases the glitches at the other two modules [12]. XOR-XNOR outputs are generated simultaneously in [3,6]. XOR-XNOR circuit designed with six transistors has a worst-case delay when both the inputs are identical [13]. XOR-XNOR structure offered less delay but with high power consumption [14]. XOR-XNOR module is designed using 12 transistors offers low power along with high speed when compared to other circuits [15]. XOR-XNOR circuit is designed with only ten transistors which offer high speed and low power [16].

Adder is designed using four modules, where module1 generates AND, OR logic and module 3 generates XOR logic, module 2 is designed using Transmission gate-based mux to generate carry output and module 4 requires XOR to produce sum output [17]. True form of logic is used for generating both the sum and carry has more logical in -equality as in [3,6,14,15,16,17,18,19,21,22,23,24,25].Proposed approach is to go with complemented logic for carry in and carry out such that it will lead to more logical equality between the two outputs. This can also reduce the power consuming switching activity. Novel delay analysis is also proposed to increase the degree of confidence and also to validate the results.

2. REVIEW OF FULL ADDERS

This section reviews few of the hybrid full adder and adder structures, where they have shown the best performance of the existing structures. Design of full adder is also analyzed for the delay and power consumption.

P. Bhattacharyya *et al* [12] XNOR block is generated and then an inverter is used to produce XOR block, this will lead to increase in the delay. To design carry block, two transmission gates are used to produce true form of output. To design sum block, one more XNOR block is designed by efficiently utilizing the not gate which was used to design XOR. Two XNOR structures with 12 transistors are used to design sum block and two transmission gates with 4 transistors are used for designing the carry block. There are four number of transistors in the critical path for producing both the sum and carry outputs. Total number of internal and external nodes are five in the circuit which can have the activity.

Hamed Naseri and Timarchi [15] XNOR/XOR logic is proposed with 12 number of transistors in the module1. In the module2 for generating carry out, two transmission gates will produce full swing for all the input combinations, an inverter is also used for better driving purpose. In the module3 for generating sum, two transmission gates will produce full swing for all the input combinations, an inverter is also used for better driving purpose. Output logic will be generated through the XNOR/XOR block in the first level, transmission gates in the second level, not gate in the third level.

J. Kandpal *et al* [16] Design4 of XNOR/XOR module is designed concurrently with 10 transistors by utilizing the complemented input of B for generating both the outputs as module1. Module2 for sum block has designed such that it will have four paths to generate the output and all those paths to be activated, it will take three transistors to be on.
Module3 for carry has designed such that it will have four paths to produce the output, but to activate two paths it requires only two transistors and for the rest it needs three transistors to be on. [2] emphasized that people who are visually impaired have a hard time navigating their surroundings, recognizing objects, and avoiding hazards on their own since they do not know what is going on in their immediate surroundings. We have devised a new method of delivering assistance to people who are blind in their quest to improve their vision. An affordable, compact, and easy-to-use Raspberry Pi 3 Model B+ was chosen to demonstrate how the proposed prototype works.

M. Hasan *et al* [17] To design the sum block, XOR logic with inverter for A is used and in the second level instead of using inverter for XOR, inverter is used for carry input to produce the sum. To design the carry, in the first level two transmission gates and two pass transistors are used and in the second level two more transmission gates are used to generate the carry. Two not gates with inputs as A and Cin are needed. Four transmission gates and two pass transistors are needed to design carry output. two transmission gates and four pass transistors are needed to design sum output. Total number of internal and external nodes are seven in the circuit which can have the activity.

3. PROPOSED FULL ADDER

Table 1: Truth table of full adder with complemented carry in and carry out

A	B	CIN'	SUM	COUT'
0	0	0	1	1
0	0	1	0	1
0	1	0	0	0
0	1	1	1	1
1	0	0	0	0
1	0	1	1	1
1	1	0	1	0
1	1	1	0	0

Table 1 shows the truth table of full adder with complemented carry in and carry out. Since at the least significant stage of full adder there will not be any carry in, but we assume that as logic'0' and the Proposed adder considers complemented carry in, where it can be assumed at as logic'1'. In the ripple carry structures, at the most significant stage an inverter is needed to produce the true form of carry output. Truth table for sum output can be divided into two subsets as in *Table 2* and *3*.

Table 2: First subset of truth table for sum

A	B	CIN'	SUM
0	0	0	1
0	1	0	0
1	0	0	0
1	1	0	1

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Table 2 clarifies that when CIN'='0', SUM is logically equal to A XNOR B. It means that PMOS transistor whose gate input will be CIN' and the logic it is expected to drive is A XNOR B. The problem can occur when A XNOR B is logic '0' due to the lack of full swing. Boolean equation is

SUM= (CIN')'.(A XNOR B) …….. (1)

Table 3: Second Subset of truth table for sum

A	B	CIN'	SUM
0	0	1	0
0	1	1	1
1	0	1	1
1	1	1	0

Table 3 clarifies that when CIN'='1', SUM is logically equal to A XOR B. It means that NMOS transistor whose gate input will be CIN' and the logic it is expected to drive is A XOR B. The problem can occur when A XOR B is logic '1' due to the lack of full swing. Boolean equation is

SUM= (CIN').(A XOR B)…….. (2)

Table 4: Lack of full-swing input combinations for sum

A	B	CIN'	SUM
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1

Table 4 clarifies that when A XOR B = '1' or A XNOR B ='0', then SUM is logically equal to CIN'. It means that NMOS transistor whose gate is A XOR B and the PMOS transistor whose gate is A XNOR B can give full swing and logic it is expected to drive is CIN'. Boolean equation is

SUM= (A XOR B).(CIN')…….. (3)

Table 5: First subset of truth table for carry out

A	B	CIN'	COUT'
0	0	0	1
0	0	1	1
1	1	0	0
1	1	1	0

Table 5 clarifies that when AB="00" then logic required for complemented carry out is '1'. when AB="11" then logic required is '0'. Two PMOS and two NMOS in series make sure that full swing is achieved. Boolean equation is

(COUT') = (A'.B').(A.B)'……(4)

Table 6: Second Subset of truth table for carry out

A	B	CIN'	COUT'
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1

Table 6 logic requirement is also same as *table 4*. XNOR and XOR structures are needed to design the full adder and they are taken from the (J. Kandpal *et al*., 2020) where only 10 transistors are required.

(COUT')= (A XOR B).(CIN')…….. (5)

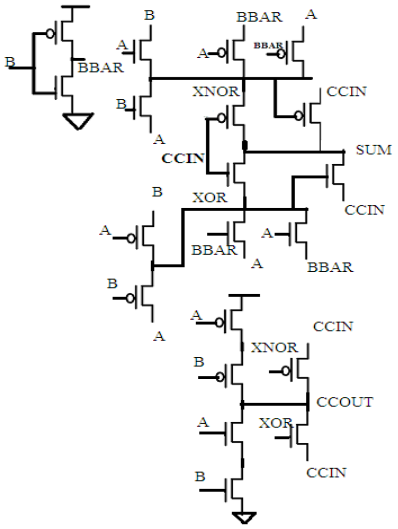

Figure 1: Proposed adder

Proposed adder in *figure 1* has only two modules, where XNOR/XOR is embedded in the sum and complemented carry module. For the sum, when complemented carry in= '0' then A XNOR B is transmitted to the output. When complemented carry in ='1' then A XOR B is transmitted to the output. For the complemented carry out, when A and B are "00" or "11" then two PMOS and two NMOS transistors are used to realize the logic. For the sum and complemented carry output, when XNOR= '0' it means that XOR= '1' then complemented carry in is propagated to the outputs. First internal node is NOT gate which is used for B input, second and third internal nodes are XNOR/XOR. External nodes are module1 and module2 which are needed to generate sum and carry outputs.

4. PERFORMANCE ANALYSIS

This section has both delay and power analysis in detail for the validation of the results.

4.1 Delay analysis

To estimate the delay of sum and complemented carry output of full adder, truth table of full adder needs to be rearranged for the output possibilities of '0' and '1'.

Table 7: Rearranged truth table of sum for delay analysis

A	B	CIN'	Decimal	SUM
0	0	1	1	0
0	1	0	2	0
1	0	0	4	0
1	1	1	7	0
0	0	0	0	1
0	1	1	3	1
1	0	1	5	1
1	1	0	6	1

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Truth table for sum output is shown in the above *table 7*. There are four possibilities of output '0' and output '1' which means that 4*4 possible low to high and high to low transitions. All these possibilities need to be applied for measuring the propagation delay from low to high and vice-versa.

To do the delay analysis efficiently, for about 33 test vectors need to be generated to find out the delay for the sum output. Generating the test vector for only activating the critical path may not be sufficient, since delay does also depend on the previous test vector. It may take more time for a particular node to be discharged and charged based on previous input.

Table 8: Rearranged truth table of complemented carry out for delay analysis

A	B	CIN'	Decimal	COUT'
0	0	0	0	1
0	0	1	1	1
0	1	1	3	1
1	0	1	5	1
0	1	0	2	0
1	0	0	4	0
1	1	0	6	0
1	1	1	7	0

Truth table for complemented carry output is shown in the below *table 8*. There are four possibilities of output '0' and output '1' which means that 4*4 possible low to high and high to low transitions. All these possibilities need to be applied for measuring the propagation delay from low to high and vice-versa.

Table 9: Delay for 1-bit proposed sum output with supply 5v at frequency of 1GHZ with delay units ps

ABCCIN	0	1	2	3	4	5	6	7
0	N	50	58	N	36	N	N	145
1	67	N	N	62	N	32	90	N
2	170	N	N	8	N	17	108	N
3	N	152	6	N	21	N	N	115
4	137	N	N	17	N	8	148	N
5	N	119	19	N	8	N	N	154
6	N	37	38	N	63	N	N	58
7	14	N	N	42	N	60	58	N

Table 9 shows the delays for the possible events of the sum. N indicates no change of output. Proposed adder critical path delay for sum is 170ps for "2-0" input test sequence. Conventional 1-bit adder designs critical path delay is ranging from the minimum of 156 Pico seconds to the maximum of 180 Pico seconds for different input test sequences.

Proposed design is slower for about 14ps when compared to the best performer of the existing designs. Proposed design sum generation may be slower but the carry computation will be very fast, which in turn generates the next level sum output faster for the ripple carry structures.

Table 10: Delay for 1-bit proposed carry output with supply voltage 5v at operating frequency of 1GHZ with delay units ps

ABCCIN	0	1	2	3	4	5	6	7
0	N	N	85	N	49	N	23	57
1	N	N	78	N	57	N	49	54
2	78	10	N	13	N	41	N	N
3	N	N	17	N	21	N	15	68
4	68	14	N	23	N	14	N	N
5	N	N	32	N	12	N	5	72
6	67	54	N	54	N	81	N	N
7	63	44	N	44	N	89	N	N

Table 10 shows the delays for the possible events of the carry. "N" indicates no change of output. Proposed adder critical path delay for carry is 89ps for "7-5" input test sequence. Existing 1-bit adder designs critical path delay is ranging from the minimum of 145 Pico seconds to the maximum of 195 Pico seconds for different input test sequences as shown in *table 11*, 12.

Table 11: Delay for 1-bit carry output with supply voltage 5v at operating frequency of 1GHZ with delay units ps for different adders

ABCin (Decimal)	15	16	17	12
3-0	110	37	20	11
3-1	142	38	104	195
3-2	122	60	9	10
3-4	140	52	20	11
5-0	140	62	20	11
5-1	162	95	88	177
5-2	136	82	25	15
5-4	122	60	9	10
6-0	130	82	10	17
6-1	135	94	18	15
6-2	149	95	30	26
6-4	186	35	43	145
7-0	163	102	18	17
7-1	135	105	37	23
7-2	160	145	27	25
7-4	150	68	58	130
0-3	150	76	40	121
1-3	116	30	40	118
2-3	137	75	9	10
4-3	134	52	28	12
0-5	151	138	81	10
1-5	122	130	75	12
2-5	131	96	16	11
4-5	105	74	10	9
0-6	143	102	68	9
1-6	144	98	12	10
2-6	146	106	97	101
4-6	110	34	151	118
0-7	142	98	13	10
1-7	133	70	12	8
2-7	141	57	13	12
4-7	104	30	11	12

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Table 11 shows the delays for the adders reported in the [12,15,16,17] for the carry outputs. All the possible 32 input combinations which will be able to measure the delay for both propagation delay from low to high and high to low are applied and tabulated. Proposed adder reported 89 ps and Critical path has shown for the adder in [17] input vector to vector applied is "7-2" in decimal and the delay is 145 ps. Maximum delay is reported as 195 ps in [12] when previous input is "011" and present input is "001".

Table 12: Delay for 1-bit sum output with supply voltage 5v at operating frequency of 1GHZ with delay units ps for different adders

ABCin (Decimal)	15	16	17	12
0-1	137	51	9	8
0-2	098	30	113	130
0-4	135	98	120	154
0-7	137	38	40	7
3-1	150	60	72	150
3-2	038	48	55	50
3-4	070	65	57	40
3-7	122	180	105	48
5-1	145	77	66	136
5-2	067	62	58	35
5-4	038	44	56	50
5-7	110	125	156	63
6-1	142	48	20	12
6-2	125	63	75	93
6-4	095	76	120	157
6-7	137	51	9	8
1-0	120	24	8	8
2-0	145	37	100	155
4-0	152	55	87	142
7-0	130	17	30	15
1-3	134	75	130	141
2-3	068	88	50	50
4-3	088	90	52	75
7-3	151	102	115	102
1-5	148	142	67	170
2-5	095	95	48	75
4-5	068	88	50	52
7-5	118	112	87	170
1-6	142	92	19	8
2-6	177	173	67	67
4-6	177	112	73	87
7-6	120	17	10	7

Table 12 shows the reported delays for the adders in the [12,15,16,17] for the sum outputs. Proposed adder reported 170 ps and the adder reported in [16] is 156 ps when input vector to vector applied is "5-7" in decimal. Critical path has shown for the adder in [17] when input vector to vector applied is "3-7" in decimal and the delay is 180 ps.

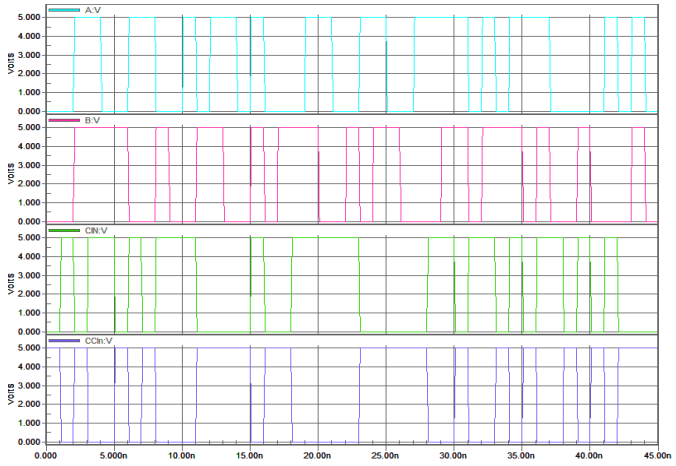

Figure 2: Test set1 for delay analysis

4.2 Power Analysis

Power is consumed only when either any internal node or external node has an event, which has a transition from low to high or high to low. Power analysis of the adder can be done by generating the test vectors which will activate all the power consuming transitions in the circuit. Test set1 is only enough to activate the events in sum and carry outputs. Test set2 can measure the activity in the internal nodes of the circuit by [23].

Table 13: Performance comparison with supply voltage 5v at operating frequency of 1GHZ for 1-bit adder

Design	Delay (ns)	Power (mw)	PDP (pj)
Our	0.170	1.489	0.253
16	0.180	1.875	0.337
17	0.156	1.816	0.283
15	0.186	3.204	0.595
12	0.195	1.814	0.353

Table 13 shows that our (proposed adder) outperforms existing designs when compared with power and energy.

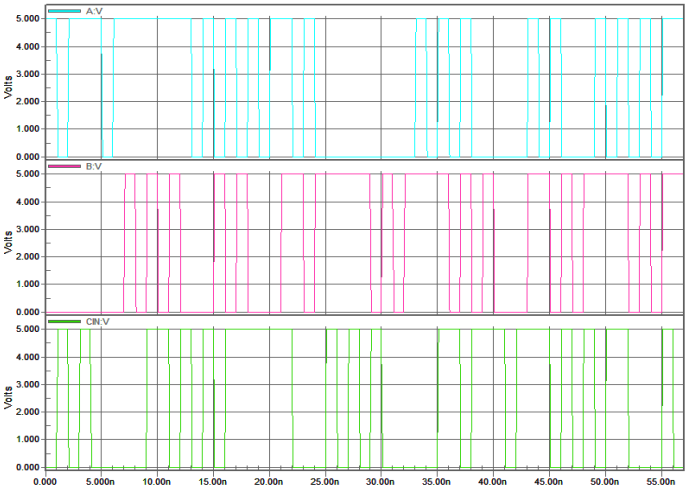

Figure 3: Test set2 for power analysis

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Figure 3 shows all possible 56 input transitions. Test set for the proposed adder is with complemented version of Cin and in [12,15,16,17] is true form of Cin.

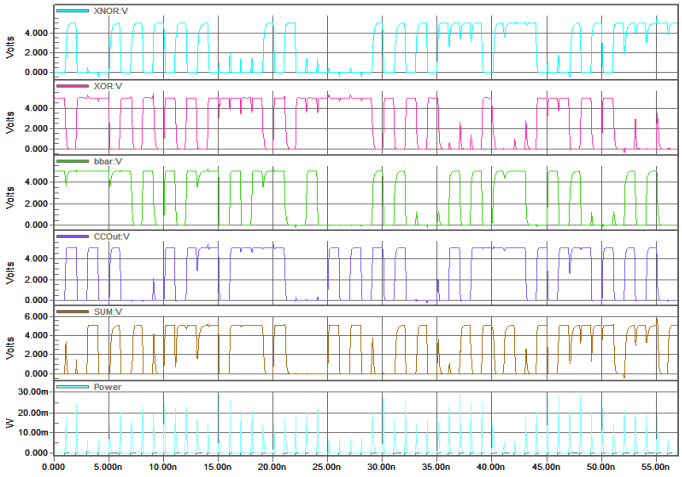

Figure 4: Test set2 results for proposed adder

Figure 4 shows the output wave form of all the power consuming internal and external nodes of the proposed adder.

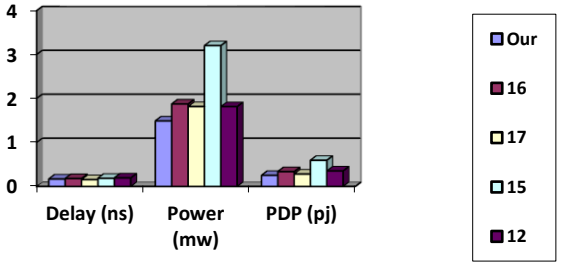

Figure 5: Results for 1-bit adder

Figure 5 shows the comparison of delay, power and power delay product of proposed adder and the adders in 12,15,16,17.

4.3 4-Bit Adder

The proposed adder and conventional adders were also implemented for 4-bit ripple carry structure and difference in the architectures are shown in *figure 6* and *figure 7*. Test set1 is being applied to the least significant bit stage of the adder and for the remaining stages inputs of A and B are taken from test set2 and for the carry inputs, generated outputs from the previous stages are given for all the designs.

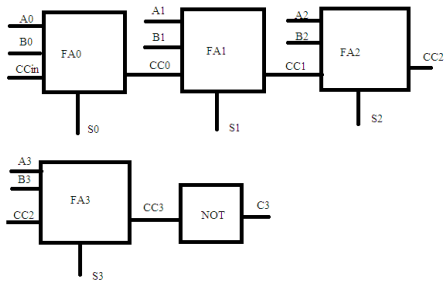

Figure 6: Proposed 4-bit adder structure

Figure 6 shows FA0 which is LSB stage of adder with complemented carry input (CCin) and this adder also generates carry output in complemented version named as CC0. In the similar fashion all the adders FA1, FA2, FA3 does have their carry inputs and carry outputs in the complemented version. Finally, not gate is needed to generate the FA3.

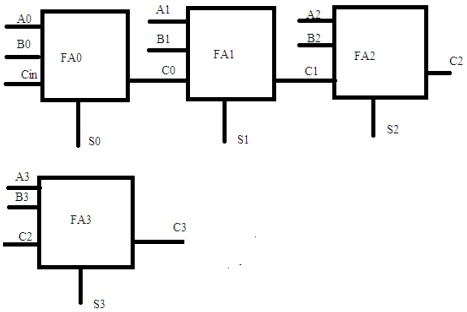

Figure 7: Conventional 4-bit adder

Figure 7 shows FA0 which is LSB stage of adder with true form of carry input (Cin) and this adder also generates carry output in true version named as C0. In the similar fashion all the adders FA1, FA2, FA3 does have their carry inputs and carry outputs in the true version. In the similar fashion, N-bit adder can be designed with 1-bit cascaded structure.

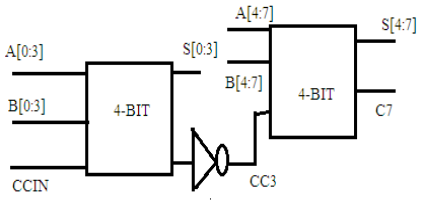

Figure 8: Proposed 8-bit adder structure

Figure 8 shows the structure of 8-bit, where two 4-bit adder structures in *figure 6* and one not gate are required. In the similar fashion, 16-bit adder structure can be designed by using two 8-bit adder structures and one not gate. This methodology is also followed to design 32-bit and 64-bit. To evaluate the power for conventional and proposed N-bit adder, A input and B input in test set2 is applied for corresponding A(LSB:MSB) and B(LSB:MSB). Carry input in test set2 is applied for all the conventional adders and complemented carry input is applied for the proposed adder. All the results in *table 12, 15,16,17* for 4-bit, 8-bit, 16-bit, 32-bit and 64-bit are taken with pulse width of 1ns, 2ns, 4ns, 10ns, 20ns respectively.

Table 14: Delay comparison with supply voltage 5v for different adder circuits with different sizes of adder in ps

Adder	15	16	12	17	Prop
4-bit	775	563	295	300	505
8-bit	1675	1237	980	840	1200
16-bit	3450	2560	2450	2280	2650
32-bit	7000	5225	5700	5270	5550
64-bit	14100	10010	12200	11260	11250

Table 14 shows the comparison of delay for proposed adder and the adders in [12, 15, 16, 17]. Adders in [12,17] unable to

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produce acceptable voltage levels from 16-bit to 64-bit with pulse width of 4ns, 10ns, 20ns respectively but reported less delay up to 8-bit. Insertion of buffer is needed for every 8-bit.

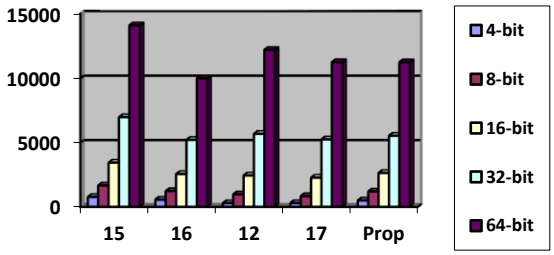

Figure 9: Delay results for adder

Adder in [16] has reported less delay from 32-bit to 64-bit. Proposed design is better than the designs in [12,15].

Table 15: Power comparison with supply voltage 5v for different adder circuits with different sizes of adder in mw

Design	15	16	12	17	Prop
4-bit	14.45	8.78	7.93	7.75	7.01
8-bit	14.8	9.06	9.73	9.34	7.57
16-bit	15.1	9.3	11.44	11.08	7.96
32-bit	12.2	7.63	10.08	9.7	6.56
64-bit	12.21	7.7	10.57	10.14	6.64

Table 15 shows the comparison of power and proposed adder reported least power consumption consistently from 4-bit to 64-bit.

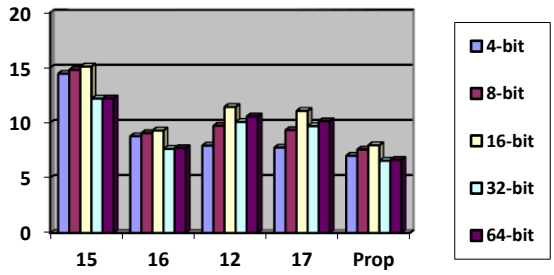

Figure 10: Power results for adder

In *figure 10*, proposed adder has shown a power savings of 9.5% to 16.5% with it's best counterpart from 4-bit to 64-bit.

Table 16: Energy comparison with supply voltage 5v for different adder circuits with different sizes of adder in fj

Design	15	16	12	17	Prop
4-bit	11198	4943	2339	2325	3540
8-bit	24790	11207	9535	7845	9084
16-bit	52095	23808	28028	25262	21094
32-bit	85400	39866	57456	51119	36408
64-bit	172161	77077	128954	114176	74700

Table 16 shows the comparison of energy for proposed adder and the adders in [12,15,16,17]. **A**dder in [17] reported less energy from 4-bit to 8-bit.

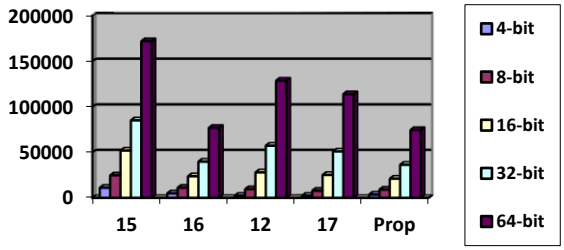

Figure 11: Energy results for adder

5. CONCLUSION

1-bit adder has been proposed with complemented carry in and complemented carry out structure. This way of proposal has led to the change of truth table, which in turn gives a novel way of designing the logic. Adder was evaluated for power, delay, energy and process control. Proposed adder outperformed conventional designs when compared to the power for about 15.5% -53.75% and Energy savings for about 8.8% -57.3%. Proposed adder needs (N-1)*20+ 22 number of transistors. Conventional designs are in the range of minimum (16*N) to the maximum of (26*N) number of transistors. Results reveal that few designs given good performance for small sizes. When implemented at larger word lengths, few designs needed insertion of buffers.

6. FUTURE SCOPE

The proposed methodology of adder design can also be applied for the design of multipliers. Partial products of the multiplier can be modified to redesign the adder blocks which are needed with wide variety of versions for their enhanced performance. This way of approach gives the default advantage of low power due to its less switching activity.

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