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Mitigation of Critical Delay in the Carry Skip Adders Using FinFET 18nm Technology

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ABSTRACT- In this paper optimization of full adder in 3-dimensional (3-D) using Fin Field Effect Transistor (FinFET) with Gate Diffusion Input (GDI) is proposed to optimize critical delay, power. FinFET technology is more suitable for below 10nm technology process. The major aim of this work is to indemnify significant factor in adder structure i.e. critical delay. Pipelining architecture is enforced to accomplish the objective with the aid of FinFET 18nm technology. The structure is optimized to get the minimum delay confinement. Suggested design needs less logic resources. The outcomes are validated using FPGA synthesis methods. By applying the FinFET technique, we developed adder topology yielding up to 90% performance improvement with respect to delay, power and area compared to the conventional adders. The simulation was carried out with low power cds ff mpt PDK. The study also includes a carry skip adder design for FPGA implementation.

General Terms: MOSFET, Power, FIR Filters, Design Rule Check.
Keywords: FinFET, Critical delay, 8T Full Adder, Carry Skip Adder, FPGA.

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1. INTRODUCTION

Today many of the industrial applications are designed in portable range. The dimensions of the transistor are constricted with the occurrence of short channel effects.

The FinFET technology applied for ultra-modern devices to design and fabricate all digital devices. New kind of device called FinFET is fascinating to overcome the short channels, leakage current and it has better control over the channel.

The above discussed will be thoroughly investigated in this paper. The 3-D FinFET is the best device for the design of Nano meter technology as it has higher scalability compared to CMOS. The essential elements of ICs are conductor, semiconductors; insulators are making objectives, and electrical properties to fabricate Very Large Scale Integrated (VLSI) circuits that are central components of all advanced electronic system devices [12][17][26]. These electronic systems pave the path for military, security, medical services, energy-saving, industrial, and home automation with IOT, transport, multimedia, infotainment, and the advanced digital society of present-day culture.

Throughout the 1960s, BJT manufacturing technology is endeavored. With reduced cost and switching power, CMOS technology emergence caused an increase in switching speed with enhanced memory capacity. The device physics of SCEs in conjunction with Moore's law-imposed constraints due to continuous miniaturization of planar CMOS technology to accomplish improved performance with limited power consumption [26]. The additional adverse effects in the short channel MOS Devices include process variability-induced device parameter variation due to leakage current [19] [24][12].

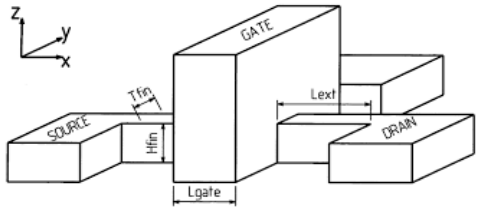

Figure 1: Three-dimensional FinFET structure on silicon-on-insulator substrate

To compensate for the adverse effect, the end body of silicon is added with an extrinsic doped source and another end i.e., Drain is made as a replica of the source with a similar doping concentration. This integrated source & drain terminals just on Gate terminal constitute a multi gate MOSFET, that is utilized to regulate flow of current there in inverted body of silicon when a defined potential is applied. With the vertical "FIN" structured silicon body on the silicon pedestal, the device is notorious for its name FinFET schematic shown in *figure 1*.

The primary goal of this paper would be to provide groundwork for the design of a Carry skip adder utilizing FinFET devices,

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as well as to examine compact versions using computer-aided circuit design (CAD) tools.

2. SYSTEM MODEL

Most full adder cores were realized with two- and three-input XOR and XNOR circuits. Raffaele De Rose et al [1]., suggested a Manchester carry skip chain employing domino logic using 45nm process technology with extra input buffers as well as a two level clock dependent buffer tree for achieving realistic input signals with a constraint domino circuit needs the most sophisticated clock distribution tree.

The High-Speed Carry Skip Adder from ref [13] is intended to work with a broad variety of source voltage levels. The biggest carry route was calculated faster for carry-out possibility pathways, at the expense of the challenges facing by the Brent–Kung adder as just a focus. However, the use of registers for the accumulation of operands and the carry mechanism used to compute the longest carry path turns a simple circuitry into a complex one. The reference [1] proposed a Delay Efficient based 32-Bit Carry-Skip Adder where the carry skip mechanism involves the use of OAI (Or and Invert) logic to realize Propagate (Pi) and Generate logic (Gi) at single stage involves the delay associated to acquire the result from the OAI gates. Reference [3] proposes an efficient carry skip mechanism using multiplexers However, the complete adder implementation employing the mirror adder principle results in complicated circuitry, with the transistor count necessary to accomplish the whole adder logic being 18 transistors. As per reference [2], developing a typical full adder topology involves the design of an XOR-MUX oriented full adder targeting communication systems applications. As ref [12], the design of a Carry-Skip Adder based on a normal complete adder using huge 14 MOS transistors as well as transmission logic has been presented. The carry-save adder as ref [17] 4-bit ALU has been developed for high-speed processors. The design methodology in the ref [21] discusses the design of 4-bit adders with hybrid CSAs in which the critical path will include three gates (AND, OR, XOR). Ref [21] discusses the Design for Fault-Tolerant Full adder, which necessitates the use of extra circuitry.

The full adder depicted in *figure 2* is implemented in this study utilizing FinFET 18nm technology. *Figure 4* depicts the gate level design of a full adder circuit using XNOR as well as MULTIPLEXER circuitry that are utilized to complete the SUM & Cout to decrease the logical effort when comparing to typical full adder circuits that need XOR as well as AOI (And Or Invert) gates. Because of the increased downsizing of technologies, minor differences in the features of intended equivalent devices might emerge during ASIC fabrication. This leads to the behavioral variations of the designed ASICs. Because of these mismatch flaws, predicting the analytical behavior of individual circuit pieces is very challenging.

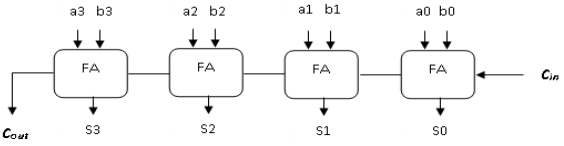

Figure 2: Conventional adder for 4 bit

As a consequence, the impact of process modifications on circuit behavior must be investigated using Monte Carlo by evaluating a simulation using the wide collection of circuitry configurations with randomly changed devices. The developed full adder with the least amount of logical work is analyzed using Monte Carlo simulations throughout this study to confirm that the suggested designs are more resilient towards global and regional process fluctuations than the previous designs [26] [25].

3D-IC solution provides 3D design planning, implementation and system analysis. The leakage can be suppressed by using a thin body [5] and it prevents the leakage of the top corner.

The CMOS based carry save adder basically consist of and gate and XOR gate that have low power consumption and the simulation was carried out using H-spice [6]. The simulation results were carried out.

The increased complexity and nano meter range of advanced integrated circuits make them permitting to performance and quality issues. In this paper proposed Pipelining architecture is also incorporated in the 4-bit Carry Skip Adder which is much useful in FIR filters where the basic element used is a full adder and the efforts are made to reduce the critical delay.

3. METHODOLOGY

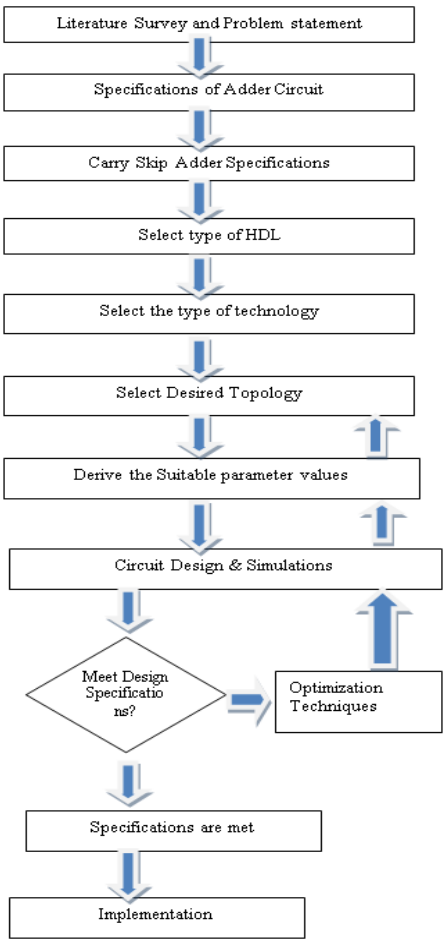

Figure 3: Proposed Full Adder Design Methodology

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The systematic approach for this research would indeed be a process procedure in implementing the issue under consideration. After that, depending on the literature survey, adder requirements must always be defined. The research of the literature revealed two types of approaches.

The first one is a technological solution, while the second would be a design approach. Current designs are made up of Simple techniques. Numerous modifications are required to the current architectures in the ideal design and the relevant adder has been built. Both architecture and methodologies are utilized to develop the adder throughout this study. The adder was chosen to replace the current conventional adder due to its low power as well as fast performance. The Proposed Full Adder Design Methodology is shown in *figure 3*.

The following formula for MOS transistor is used to compute the EKV configuration.

$$I_C = \frac{I_D}{I_S} \ldots\ldots\ldots\ldots\ldots \quad (1)$$

$$g_m = \frac{I_D}{\eta \Phi_t} \frac{1-\exp(-\sqrt{IC})}{\sqrt{IC}} \ldots \quad (2)$$

$$I_s = 2\mu C_{ox} \frac{W}{L} \emptyset_t^2 \ldots\ldots \quad (3)$$

Where,

I_S - normalization current.

I_D - drain Current

ŋ- Slope factor, normally taken as 1.

C_{ox}- Oxide Capacitance.

$$C_{ox} = \frac{\epsilon_0 \ \epsilon_{si}}{t_{ox}}$$

ϵ_0 -permittivity of free space

ϵ_{si} - Relative permittivity of Silicon

t_{ox}- Thickness of the oxide layer

ϕ_t - Thermal voltage at room temperature, taken as 25.6mv

I_C - Inversion Coefficient

Based on the EKV transistor model discussed in this chapter, the dimensions of the various transistors of the circuit operating in weak inversion region are tabulated as follows from ref [4].

Table 1 represents the dimensions of the various transistors involved in the proposed design. The channel length of the transistor can be chosen by the designer based on the required design considerations. The maximum length of the transistor may be chosen 10 to 13 times of the technology used in the designing process.

Table 1: Dimensions of the transistors

Device	Dimensions(W/L)
NMOS	1-Feb
PMOS	4.5/1

4. MONTECARLO ANALYSIS OF FULL ADDER

Figure 4 shows that architecture of the adder has originally chosen depending on a literature study. After that, the appropriate equipment technologies should be chosen depending on the requirements. The simulation would then be conducted to get the appropriate model parameters. These statistics are evaluated to the specifications to see whether they have been met. If indeed the requirements are not fulfilled, the suggested circuit would be developed using optimization algorithms to match the correct parameters; else, the circuit would be built with no optimization.

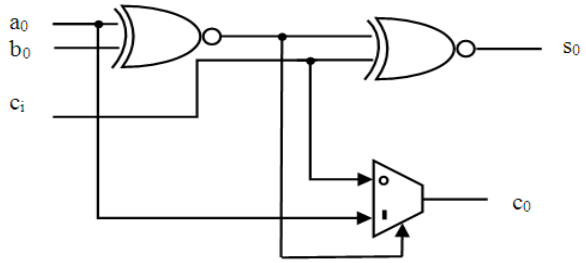

Figure 4: Gate Level modelling of Full Adder

In this paper the design adopts full swing XNOR and Multiplexers where multiplexer alleviate the critical delay introduced due to the application of conventional And Or Invert logic used to generate $C_{out.}$ The full adder shown in *figure 4* is implemented using FinFET 18nm technology which is shown in *figure 5* with minimum logical effort using XNOR and Multiplexer logic. The full adder circuit is implemented using only 10 FinFETs. As compared to the previous designs obtained from the literature, the suggested solutions use less power. The proposed full adder then investigated using Monte Carlo simulations that ensure he suggested designs are more resilient against domestic and global processing fluctuations than Current designs.

Monte Carlo simulation is often used to analyze the variability of the entire adder circuit. According to the findings of Monte Carlo simulation, the suggested FinFET-based adder is much more reliable and also has a greater tolerance to process fluctuation than that of the reported earlier adders with in literature. As a result, the suggested architecture may be appropriate for low-energy as well as high-speed Applications.

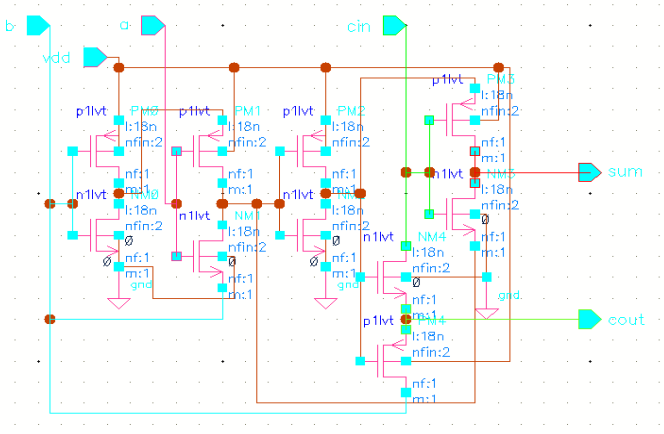

Figure 5: Implementation of Full Adder using FinFET 18nm

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After simulation and obtaining the results, the components of the schematic are placed on to the substrate to realize the layout of the physical circuit. Each component's layout is generated and placed from the schematic using Cadence Virtuoso Assura tools. The final layout with interconnects is verified using the Assura tool. The circuit is laid out using 18nm FinFET technology. The layout is designed in such a way that the isolation between components is provided based on the design rules and to avoid noise and signal coupling as the main concern. Apart from this interconnect between the components are made short to avoid parasitic effects. The layout of the simulated Full adder with met performance specifications are realized by DRC and LVS successfully. To make the designed layout ready for fabrication the circuit is verified based on the technology design rules and exact matching to the schematic.

The task of layout and DRC (Design Rule Check) and also LVS (Layout versus Schematic) are carried out successfully using Assura and the reports are depicted in *figure 6*, *figure 7* respectively. The Schematic design of AND gate and Mux using FinFET is depicted in *figure 8*.

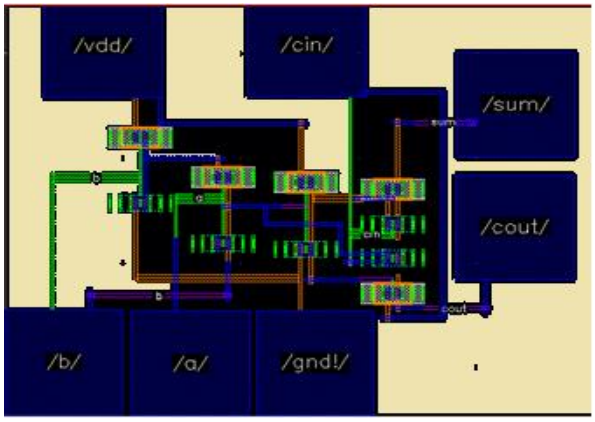

Figure 6: Layout of full adder using 18nm

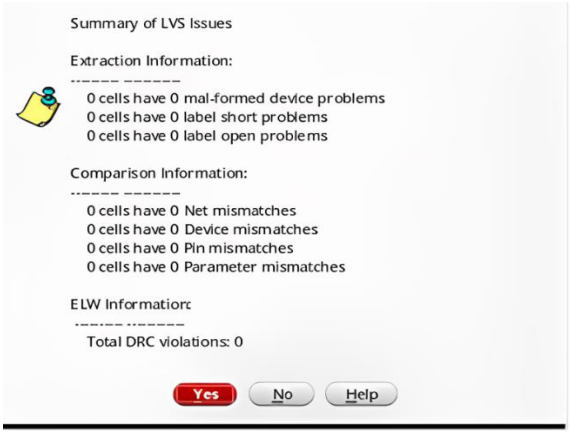

Figure 7: Layout versus Schematic reports

As indicated in *figure 9(a)*, a carry skip adder schematic diagram is developed using cadence virtuoso tool, and also the actual design is depicted in *figure 9(b)*. The design of inverter, and gate & multiplexer gate is implemented which are portrayed in *figure 8*. Performed simulations of the full adder is compared with the literature [18] & [24] which reveals the fact that the designed full adder is much more efficient in delay and power consumption.

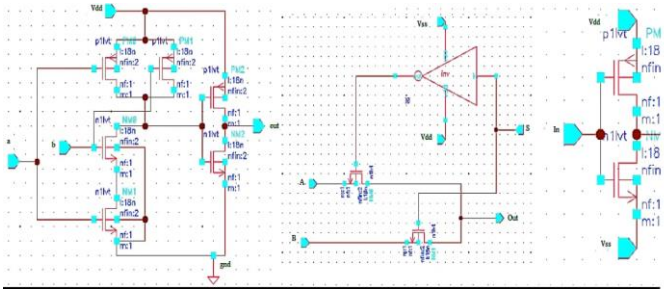

Figure 8: Schematic design of AND gate and Multiplexer using FinFET 18nm Technology

Table 2: Result Analysis with existing methods

	FinFET 18nm					
	Power Analysis		Delay Analysis		Area Analysis	
	Prop.	Exist.	Prop.	Exist.	Prop.	Exist.
Full adder	20.22nW	2.5mW [18]	1.2 psec	126.5 psec [24]	90.66msqm	-
		2360W[1]		183sec[1]		291sqm[1]
		-		1.15ns[11]		357.4μm^2 [11]
		78.0[5]		21.1psec		132msqm

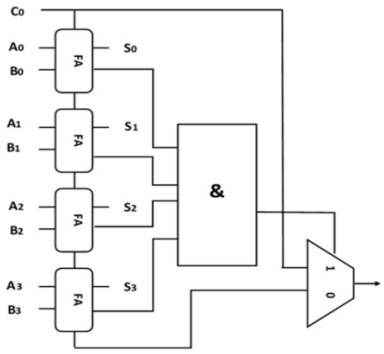

Figure 9 (a): Block Diagram of 4 bit Carry Skip Adder

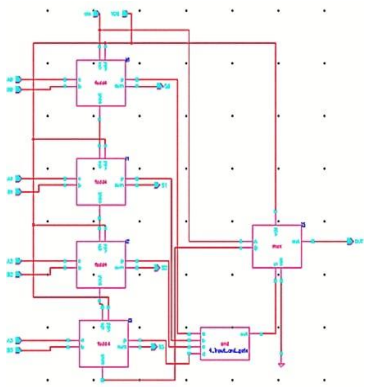

Figure 9 (b): Schematic design of 4 bit Carry Skip Adder

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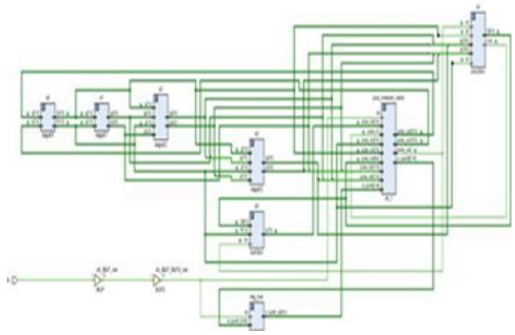

Figure 10: Synthesis of Carry Skip Adder

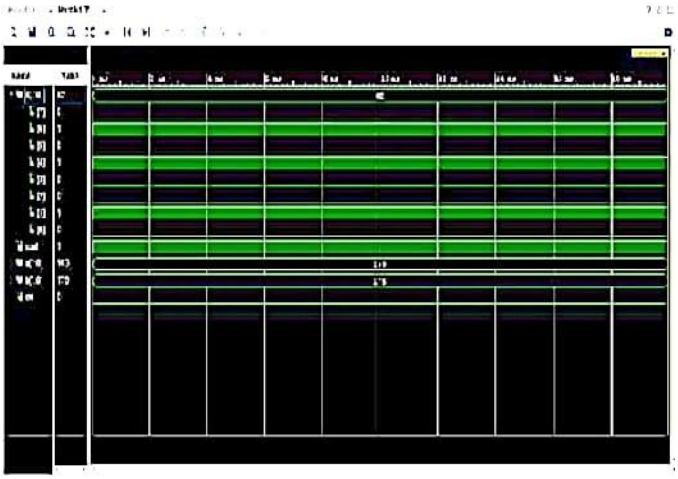

Figure 11: Simulation of 8-bit CSA

5. FPGA IMPLEMENTATION

The adder is designed in Verilog HDL and realized on a Xilinx 7000 series SOC utilizing Vivado Design Suite. Xilinx Spartan FPGAs as well as development boards are supplemented with hardware development tools design Suite and it yields dynamic and highly advanced self-contained platform. The suite meets the need for design processes and offers a tried-and-true technique for maximizing efficiency from idea through development and debugging. The synthesis of CS adder is depicted in *figure 10* followed by simulation representation in *figure 11*.

A carry skip adder design suited for FPGA implementation has been presented in the research. The suggested multiplier needs less logic resources. To validate the findings, FPGA synthesis methods are utilised.

6. CONCLUSION

The proposed 18 nm technology FinFET carry skip adder eliminates the complex XOR/XNOR functions for the generation of sum and carries. The critical delay is also addressed in the article which is reduced by employing pipeline architecture. The proposed paper outperforms the conventional adders by reducing the critical delay, area and power dissipation by 20% and 30% respectively. It is noted that there is a huge improvement in reducing force as well as area of the adiabatic reasoning circuits when compared to typical rationale circuits. This research provides a glimpse of the more distant possibilities which include atomic scale computational devices that is good enough even at room temperature.

7. FEATURE SCOPE

Proposed design has also been applied to machine learning, Artificial intelligence applications to perform the validity of the proposed adder design. This system introduces a new dimension for the optimization of Integrated circuits in which the arithmetic is directly customized. Future work will explore the new technology

8. ACKNOWLEDGMENTS

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