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Design and Characterization of a Novel FinFET based NCL Cell Library for High Performance Asynchronous Circuits

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ABSTRACT- In recent times, synchronous circuits are facing design related issues like clock skew, glitch power, EMI, leakage power, etc. The clock-less design paradigm – Asynchronous design challenges most of these issues and accepted as a better alternative to clocked circuits. QDI based Null Convention Logic (NCL) is such a clock-less design concept. However, NCL designs couldn't get wide spread acceptance due to unavailability of commercial CAD tools and design compatible NCL standard cell library. The proposed research work in this paper demonstrates design and characterization of FinFET based NCL cell library to facilitate QDI based asynchronous circuit design. The NCL cells are designed with ASAP 7nm PDK. A complete set of 27 NCL threshold gates are developed and characterized in cadence using ocean scripting. Various time and energy models are extracted for different process corners using EDA platform. The proposed work will help research scholars to implement NCL based asynchronous circuits. This paper also demonstrates comparative performance analysis of bulk-CMOS and multi-gate FinFET based NCL threshold gates in 16 nanometer technology. The analysis has concluded average 19% of improvement in power-delay produce for FinFET based cells compared to its CMOS counterparts. To showcase two-dimensional comparison, various static and semi-static NCL gate structures are also compared in term of their power and speed. Various arithmetic circuits are designed using these standard NCL cells to demonstrate its application. The results indicated substantial performance improvement in terms of power and speed.

Keywords: Clock-less Design; Null Convention Logic; Delay-Insensitive circuits; Multi-gate devices.

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1. INTRODUCTION

Recent industry trends in the sectors like communication, healthcare, infotainment, defense, etc., demands high end computing powers along with improvement in speed. These trends are majorly run by advancement in chip industry. Such advancement is possible with miniaturization of on-chip devices to atomic level. At lower technology nodes, designers are facing challenges like uncontrolled interconnect resistance, high mutual capacitance, PVT variations, and other reliability issues. Beyond 22 nm technology, the CMOS devices are even more prone to short/narrow channel effects, increased PVT variability, larger parasitic, etc. It will ultimately result in poor current control within the device. Also, proper threshold voltage is very difficult to achieve with reduced active area [1].

The limitations of CMOS device lead to a new era of multi-gate devices, FinFET. There are no major differences in fabrication process of FinFET device compared to bulk CMOS Technology [2]. However, FinFETs are the most viable substitute to bulk MOSFETs, as it supports better scalability, lower leakage power, negligible short channel effects, and most importantly its structural and functional similarity with bulk CMOS devices. Moreover, the latest trend in digital circuitry majorly targets on high throughput and improved performance with lower energy requirements. At the architecture level, there are two major design styles namely, Synchronous designs and Asynchronous designs [3]. From past many decades, synchronous design paradigm was predominantly used which is having a global clock to synchronize all events and state transitions within the design. However, increasing circuit complexity has raised many clock related issues like inefficient routing, unmanageable clock skew, jitter, strict setup and hold time requirements, etc., Synchronous designs with high clocking rate demands more power also. Such strict requirements pose a bigger challenge to the designers [4].

All such limitations of clocked design style leads to adoptions of asynchronous design paradigm, which removes dependencies on clock. In spite, it uses local handshaking to synchronize different events and state transitions. Elimination of the global clock removes complex clocking networks, which ultimately lower the power requirement. QDI based Null Conventional Logic - NCL is one of the clock-less design style. Its delay insensitive design concept makes it most promising Asynchronous design style offering high throughput [5].

Since many decades, clocked designs are matured with well-established and simple design flow. Availability of high end automated CAD tools reduces the overall design time [6, 7]. On

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the other hand, due to variety of design styles and larger design space, asynchronous designs are lacking with efficient CAD tools and testing methodologies [8].

The proposed research work includes comparison of NCL gate designs with FinFET and CMOS devices. For different NCL gates, area and PDP (power-delay product) of proposed structure is compared with its static and semi-static variants. Also, cell characterization of all 27 threshold gates is performed with Liberate tool. Various tools from cadence are used to facilitate translation from schematic to physical level layout of NCL gates. The proposed work combines benefits of FinFET and QDI based NCL design paradigm. This incorporation of two technologies can deal with current requirement of high-performance designs for semiconductor industry.

This research paper is divided into five different sections. *Section 2* will briefly focus on basics of Null convention logic and multi-gate FinFET device. *Section 3* provides simulation results with comparative analysis for different NCL gate structures. Result for cell characterization of NCL gates is analyzed in detail in *Section 4*. The research work is concluded with scope of future work in *Section 5*.

2. MATERIALS AND METHODS

2.1 Asynchronous Designs

Asynchronous circuits are becoming more widespread due to the rising constraints and complexity of synchronous design. Asynchronous systems rely on handshaking to exchange data between functional blocks in the absence of a global clock that drives register and state changes.

Bounded delay models and Quasi-Delay-Insensitive (QDI) models are the most common types for asynchronous circuits. They are differentiated based on the encoding scheme and various assumptions for the delay. Asynchronous data transmission channels usually require two additional signals in addition to data wires: Req and Ack. Whenever the data is available, the sender will transmit the Req signal, which will start the data transfer. The receiver will trigger an Ack signal after receiving and processing the data, signaling that more data can be sent [9].

The delay among all wires and gates is bounded in bounded-delay models. All gates and wires will be given a delay range, and it is anticipated that the delay will be within the limits of all operations. As a result, bounded delay model is typically structured using a bundled-data encoding technique as shown in *figure 1*, which uses localized worst-case timing constraints to govern data flow. The Request signal is delayed till that all data values have a genuine and stable state, and only then will the Acknowledgement signal be sent back once all data signals have been sampled. Bounded-delay model uses a synchronous design paradigm and offers efficient encoding, but they necessitate considerable worst-case delay analysis [10].

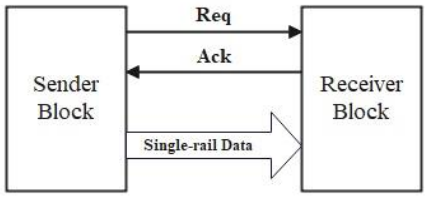

Figure 1: Bundled-data Encoding

To minimize unexpected hazards and glitches, quasi-delay-insensitive (QDI) designs enable arbitrary cell and interconnect delays while imposing isochronic fork assumptions. This assumption is that timing skews generated by interconnect delays are substantially smaller than timing skews caused by gate delays within fundamental components like complete adders, and hence delays to each end of forking wires are nearly similar. Further wire delays don't have to comply with this assumption at the component connection level, because completion detection circuits can influence the receipt of input data [11]. As a result, QDI circuits require very little timing analysis and, unlike Bounded-delay models, can attain average performance rather than worst-case performance. To convey data, QDI circuits commonly employ a multiple-rail encoding method. *Figure 2* shows a dual-rail encoding system, in which each binary signal is represented by two wires. The Req wire is deleted because the data itself reveals whether it is genuine or not.

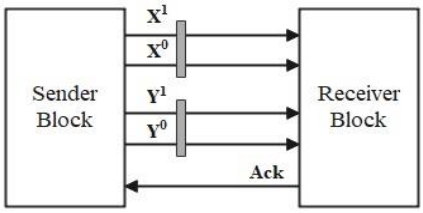

Figure 2: Dual-rail Encoding

2.2 Null Convention Logic Designs

NULL CONVENTIONAL LOGIC is a new design paradigm used to implement asynchronous logic. Here, “NULL” represents there is NO DATA between two subsequent DATA inputs. NCL designs are theoretically delay-insensitive circuits. NCL is not a complete Delay-Insensitive circuit but one of the types of DI called as Quasi-Delay-Insensitive (QDI) [12]. QDI is implemented using the Isochronic Fork assumption. This means such delays are considered completely identical. NULL Convention Logic effectively demonstrates all desired benefits of asynchronous designs like, Ease of Design, Reduced design efforts and potential risk, Low power consumption, Seamless technology migration [13].

NCL signal combines data-state along with control information to remove delay dependency. Positive or high voltage (asserted) for each logic rail is considered as DATA, whereas low or zero voltage (de-asserted) means NULL, which indicates "no data available". For each binary bit, typically a dual-rail encoding is used as shown in *table 1*.

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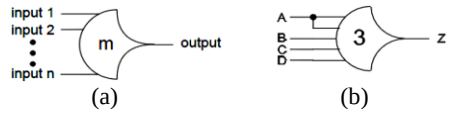
Table 1: Dual-Rail Logic

	DATA 0	DATA 1	NULL	INVALID
D0	1	0	0	1
D1	0	1	0	1

Threshold gates having state-holding capability are used for implementing NCL design. Such gates have multiple inputs and necessarily single output. Threshold gate output indicates DATA only when the number of inputs reaches or exceeds the gate threshold value [14]. The hysteresis behavior keeps the output the same as the previous until all its inputs return to "NULL". *Figure 3(a)* indicates symbol for THmn gate, where m = threshold value and n=No. of inputs. For example, TH34W2 gate has four inputs and 3 as gate threshold value with input A having weightage 2 as shown in *figure 3(b)*.



(a) (b)

Figure 3: (a) NCL Gate symbol (b) TH34w2 Gate

Table 2: Basic NCL Gates

Sr. No.	NCL Gate	Logic Function
1	TH12	X + Y
2	TH22	XY
3	TH13	X + Y + Z
4	TH23	XY + YZ + ZX
5	TH33	XYZ
6	TH23w2	X + YZ
7	TH33w2	XY + XZ
8	TH14	X + Y + Z + W
9	TH24	XY + XZ + XW + YZ + YW + ZW
10	TH34	XYZ + XYW + XZW + YZW
11	TH44	XYZW
12	TH24w2	X + YZ + YW + ZW
13	TH34w2	XY + XZ + XW + YZW
14	TH44w2	XYZ + XYW + XZW
15	TH34w3	X + YZW
16	TH44w3	XY + XZ + XW
17	TH24w22	X + Y + ZW
18	TH34w22	XY + XZ + XW + YZ + YW
19	TH44w22	XY + XZW + YZW
20	TH54w22	XYZ + XYW
21	TH34w32	X + YZ + YW
22	TH54w32	XY + XZW
23	TH44w322	XY + XZ + XW + YZ
24	TH54w322	XY + XZ + YZW
25	THXOR0	XY + ZW
26	THAND0	XY + YZ + XW
27	TH24COMP	XZ + YZ + XW + YW

As described in *table 2*, set of 27 basic NCL threshold gates gives superior flexibility to circuit level designs, compared to other delay-insensitive techniques where multiple Muller C-elements along with Boolean gates are used to synthesize clock-less designs [15].

2.3 FinFET Device

FinFET is a one of the multi-gate FET device in which the gate terminal encloses the elevated channel region and takes the shape of a fin. Unlike MOSFETs, FinFETs have a three-dimensional structure. The source and drain regions have been elevated. The gate surrounds the channel region on three sides, as shown in *figure 4.* The main benefit of this device is its similarity to MOSFETs with respect to its functionality and manufacturing process [16].

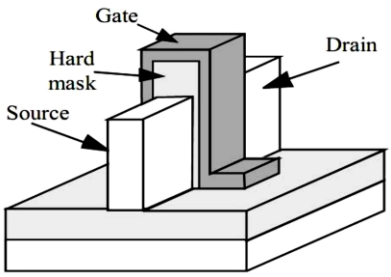


Figure 4: FinFET Structure

Conventional design techniques are applied directly to FinFET circuits with minor changes. The channel width W and channel length L are still the important design parameters. *Equation 1* defines the channel width *W* as,

$$W = 2 \times H_{fin} + W_{fin} \quad (1)$$

Where H_{fin} = Fin height and W_{fin} = Fin width. Number of fins can be increased to increase the channel width.

Different device level variants can be obtained by varying gate connections. As shown in *figure 5*, Double-gate FinFETs (DG) can be classified as, SG FinFETs (Shorted Gate) and IG FinFETs (Independent Gate). In SG-FinFETs, connecting both gates extends its current driving capability and provides better current control within channel region. An IG FinFET is functionally similar to two planner MOSFETs connected in parallel. This will reduce device level parasitic and improves timing performance.

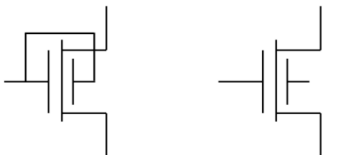

(a) (b)

Figure 5: Symbol of (a) SG-FinFET (b) IG-FinFET

3. COMPARITIVE ANALYSIS FOR DIFFERENT NCL GATE IMPLEMENTATION

A novel NCL gate structure is proposed as shown in Figure 6(c). In comparison to its static and semi-static versions [17],

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proposed structure achieved improvement in Power-delay product. Also, area utilization (No. of transistors) are less compared to static variant [18]. *Table 3* lists spice simulation results for various NCL gates with different implementation structures. *Figure 7* indicates graphical comparison of Power-Delay-Product (PDP) for various NCL structures.

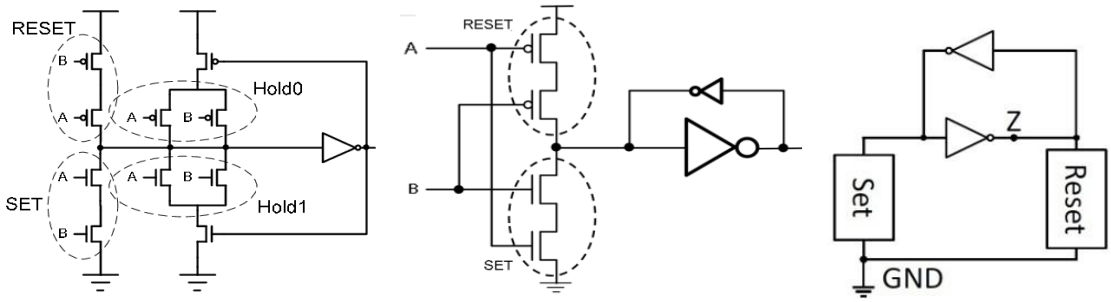
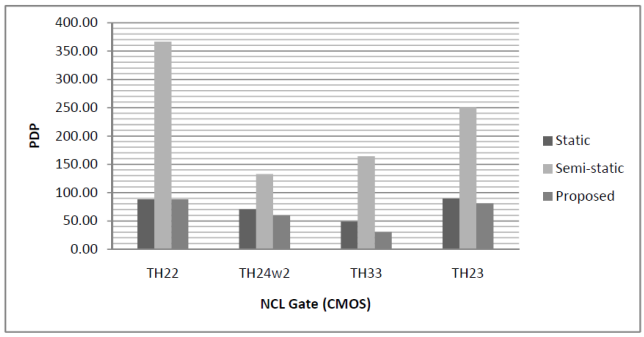


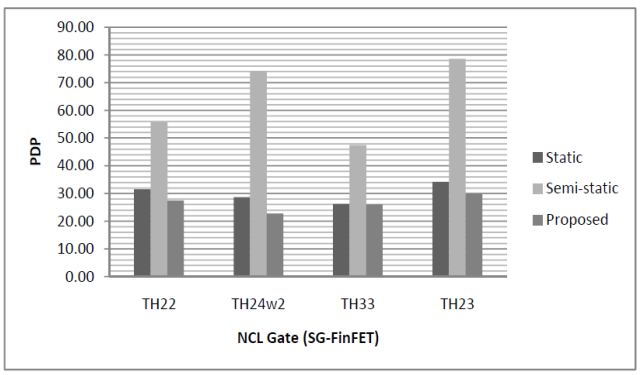
Figure 6: TH22 Gate (a) Static (b) Semi-static (c) Proposed

Table 3: Comparative simulation results for various NCL Gate structures

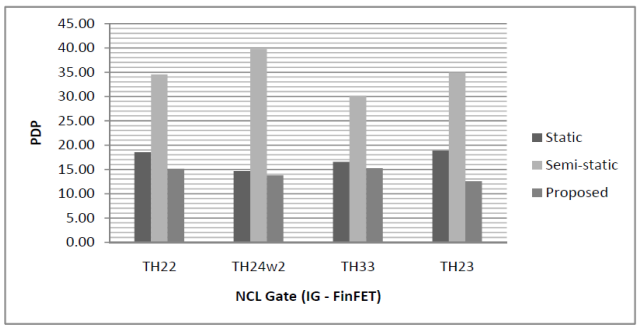
Device	NCL Gate	Power-Delay Product			No. of Transistor		
		Static	Semi-static	Proposed	Static	Semi-static	Proposed
CMOS	TH22	88.13	366.72	88.00	12	8	8
	TH24w2	70.51	132.60	59.80	20	14	14
	TH33	49.04	164.29	30.37	16	10	10
	TH23	89.21	251.39	80.94	20	12	12
SG-FinFET	TH22	31.44	55.65	27.44	12	8	8
	TH24w2	28.65	74.10	22.74	20	14	14
	TH33	26.15	47.48	26.00	16	10	10
	TH23	34.22	78.57	29.94	20	12	12
IG-FinFET	TH22	18.54	34.56	15.12	10	8	8
	TH24w2	14.65	39.78	13.80	18	12	12
	TH33	16.56	30.21	15.24	14	10	10
	TH23	18.90	35.01	12.59	16	10	10



(a)



(b)



(c)

Figure 7: Power-Delay Product Comparison of various NCL Gate structures

The SPICE level simulation is carried out with 16 nm PTM models [19]. For all other than semi-static implementation, the (W/L) for all FETs is fixed to one for fair comparison. In semi-static case, strong inverters with large (W/L) are used to hold previous state. The simulation setups for all implementations are kept uniform. By providing all inputs as DATA, Output DATA condition is achieved. NULL state is achieved between consecutive DATA state by providing reset to all inputs. For calculating the PDP, an average power and delay is obtained for all such DATA states of each NCL gate. As an example, for calculating PDP in TH34 gate, all four set conditions are

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achieved by setting specific inputs. Other technology parameters, common for all devices are: C_{Load} = 5fF, T = 25 ^{O}C, V_{Supply} = 0.9 V, t_{OX} = 1.5 nm [20].

The comparative analysis shows that the semi-static design requires more power and operates at a slower speed [23]. On the other hand, Semi-static structure demands fewer transistors compared to static variant. Also, these designs are capable to offer better noise susceptibility. The correct functionality and optimum performance of this design largely depends on correct sizing of the transistors. Bigger size transistors may be used for higher performance but at the cost of large area. Compared to CMOS, FinFET based NCL gates demonstrate 21% reduced power consumption. Furthermore, delay analysis reveals that FinFETs are 33% faster with respect to operating speed. The proposed structure is power efficient than its semi-static counterpart and has a shorter delay compared to static designs. With proper device sizing, designers can achieve even better performance [24].

4. NCL CELL LIBRARY CHARACTERIZATION

The SG-FinFET based NCL cell library is created with ASAP 7nm PDK [21,22]. Following tools from cadence are used for implementing and characterizing the 27 gate NCL cell library [25, 26].

- Virtuoso : Transistor Level Schematic design
- Spectre ADE : To simulate the design
- Layout XL : To prepare layout of the Design
- Virtuoso : To extract GDS
- Liberate : For Characterizing the NCL Cells

The library design task includes verification of the cell functionality, determining characteristics of the cell for different parametric variation across the range and creating different library files. Ocean scripting language has been used for parameter measurement. Different arithmetic circuits have been implemented using proposed cell library.

Two different adder structures are designed and synthesized using NCL library cells for proof of concept and compared with [23] to indicate improvement in performance parameters. Designs are synthesized with commercial tools and created NCL cell library.

Table 4: Simulation results for arithmetic circuits

Design	Area (No. of Transistors w/o registration)	Area (No. of Transistors with registration)	Power (mW)	Delay (ns)
[23]	216	602	20.44	10.58
Proposed 4-bit Ripple Carry Adder	176	582	0.081	0.96
Proposed 4 bit Kogge Stone Adder	142	540	0.076	0.90

Table 4 indicates improvement in power consumption and propagation delay compared to [23]. The area utilization in terms of No. of transistors is also less because, in [23] NCL cell were designed with semi-static structure, while in our design structure proposed in *figure 6(c)* is being used. The actual area utilization can even be improved with layout optimization. The proposed structure with FinFET devices demonstrate outstanding performance in terms of design parameters, which will help designers to indulge with less time and efforts to achieve design specifications.

5. CONCLUSION

In this paper, SG-FinFET based NCL cell library is designed and characterized with proposed structure. This library can be utilized for implementing various NCL based asynchronous circuits to achieve performance improvement in terms of power, delay and area. Further, this library can be enriched with different variants of low power and high speed NCL cells. Such developments will eliminate the issues related to lack of standard cell NCL libraries for researchers and designers.

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