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International Journal of
Electrical and Electronics Research (IJEER)
Research Article | Volume 11, Issue 2 | Pages 323-327 | e-ISSN: 2347-470X

Performance Analysis of Variable Threshold Voltage (ΔV_{th}) Model of Junction less FinTFET

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ABSTRACT- The work presented in this paper is a variable threshold voltage (ΔV_{th}) model of junction less fin gate tunnel FET (JL FinTFET) in which there is a shift in threshold voltage. As a result, to improve drive current and subthreshold slope among other devices. At the same time, gradually decrease the random dopant fluctuations (RDF) effects on Vth, ambipolar leakage current by using this design. The threshold voltage in the junction less fin gate TFET may be modified using 2D numerical simulations by supplying a voltage to the variable gate. The effects of the threshold voltage change on the device's overall performance investigate. A GaSb junction less fin gate TFET and AlGaSb junction less fin gate TFETs with variable threshold voltage characteristics compare. The ON state current is $1.5x10^{-3}$ A/m, the SS is 17.1 mV/decade, and the I_{amb} is $3.314x10^{-17}$ A/m.

Keywords: Variable threshold voltage (ΔV_{th}), JL Fin FET, drive current, ambipolar current.

ARTICLE INFORMATION

Author(s): Ajaykumar Dharmireddy and Sreenivasarao Ijjada;

Received: 13/03/2023; **Accepted**: 10/05/2023; **Published**: 30/05/2023;

e-ISSN: 2347-470X;

Paper Id: IJEER-1303-02;

Citation: 10.37391/IJEER.110211

Webpage-link:

https://ijeer.forexjournal.co.in/archive/volume-11/ijeer-110211.html

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1. INTRODUCTION

TFETs have been widely studied in recent years because of their 60 mV/dec subthreshold swing. Compared to MOSFETs, ION/IOFF ratios are better for TFETs since their OFF-state leakage current is more diminutive. Leakage from the reverse bias diode. To a certain extent, BTBT limits the ON-state driving current of Si TFETs using a high-k dielectric and low-band gap dopant Al, Ga, Sb, As, and InAs. TFET efficiency improved vertical architecture and fast doping junctions. The threshold voltage is an essential determinant in nanoscale devices (V_{th}). [1]. V_{th} is the threshold voltage required to transition from the off to the on the state. As the bias voltage (V_{DD}) in a MOSFET is lower, the threshold voltage must be common to maintain the same continuous driving current. Even while lowering the threshold voltage implies better leakage current (I_{OFF}) for the device [2], the amount of the voltage lower is inversely proportional to the improvement. This reduction in subthreshold swing (SS) repeat in these two device characteristics, which is more than the limit of 60 mV/decade [3].

Random dopant fluctuations (RDF) impacts on V_{th} variations are one of the barriers to ongoing improvement [4]. RDF is a severe issue in short-channel electronics, causing threshold voltage changes. Because the operating mechanism of a TFET differs from that of a MOS device, it is one of the alternatives. The bias voltage reduces in this device without enhancing the leakage current. Consequently, keeping SS below 60mV/decade is ideal for low-power device circuits [5]. The major challenge of this TFET device is maintaining a low driving current. In this work, the RDF issues address using a unique approach called "junction-less," which does not require doping the source or drain of the TFET. Uniform doping of the channel and narrow band gap materials (n+ drain and p+ source, high-k metal gate electrodes) results in an n-type doping-less tunnel field-effect transistor (FET). The suggested model has significant benefits over the standard TFET device. It eliminates the need for a p-n junction, making the junction-less fin gate TFET highly scalable and simple to construct.

1.1 Working Mechanism of TFET

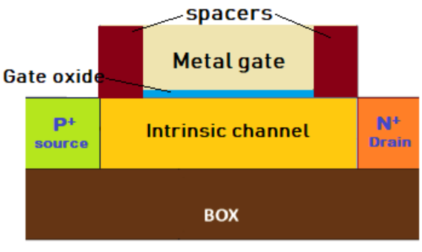

Figure 1: Cross section view of Tunnel FET [22]

A *p-i-n* junction channel design is used in the fundamental building blocks of a TFET [6]. The primary TFET device, as shown in *figure 1*, features a p-type source and an n-type drain. Additionally, it can function with a variety of gate biases. The heavily doped p+ area of the source, the lightly doped part of the n-type channel, and the heavily doped region of the n-type

drain are all parts of the same transistor. In most cases, the TFET present will comprise several parameters such as IGEN, IBTBT, and Is. IGEN is a reverse-biased voltage element determined by the formation of holes and electrons in depletion zones [7]. This process is reliant upon the flow of current through the device. IBTBT is the BTBT current dependent on this carrier tunnelling in the filled band of this origin to an unoccupied group at the station. It is more accurate to call it a reverse saturation current, which results from the current's diffusion component.

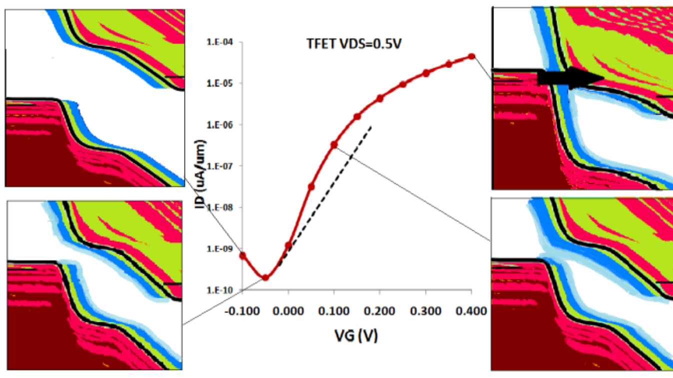

Figure 2: Energy band diagram TFET in ON and OFF state

The switching activity of a TFET may be in either the OFF or ON state. Both of these states are possible. The behavior of the TFET is related to that of a p-i-n diode when there is no field influence coming from the gate, and the tunnel space is ample and proportionate to the length of the intrinsic area, as seen in the energy band diagram of *figure 2*. The quantity of BTBT is meager, and the TFET has reached its off-condition state [8]. The TFETs have an extremely low leakage current, measured as I_{off}, much lower than the typical couple of pA/m. If the gate bias voltage is greater than the bandgap, there will be a route in the valence to the conduction band that emerges close to the source. The tunnel path is presently significantly shorter in comparison to the size of the intrinsic area, and an impacted rise in BTBT is occurring as a result. Also, increasing the gate bias reduces the tunnelling distance and makes the more conduction current (I_{ON}).

2. LITERATURE REVIEW

Ajaykumar Dharmireddy et al. [9] explain the engineered structure relies on substance variant with the usage of silicon substance for 3D Fin TFET structure by changing the fin-height as shown in *figure 3*.

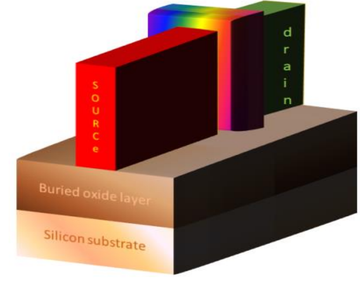

Figure 3: Rectangular Fin gate Tunnel FET[23]

The features are analyzed together with the version in bone elevation and substance variation at various areas of this arrangement [24-26]. The drive current (I_D) of 18×10^{-6}A using a minimal leakage current of 10^{-15}A and SS of 25mV/decade.

Kaishen Ou et al.[10] revealed the structure of a wrapped-around epitaxial layer in a p-type Ge-Fin TFET. Due to higher series resistance in the more significant undoped epitaxial layer behind the gate, excessive gate-source overlap may restrict drive current. Ge growth at low temperatures (330–400 C) is favoured.

W.Lee et al. [11] have shown GHGTFETs to advance the TFET switching activity. Thin bandgap materials are employed to improve the functioning of GHG TFET. Both silicon and SiGe TFETs have conduction currents of 3.8×10^{-8} A/m and 8.77×10^{-8} A/m, respectively. Triple-gate TFETs summarise with an Epitaxial layer. The effect that a Si fin's height (H_{fin}) and width (W_{fin}) have on the transport properties of the epitaxial layer TFETs the vertical BTBT cross-sectional area is proportional to H_{fin} because the EL creat on the top and sidewall of a fin. A rise in H_{fin} results in an increase in boost in the case of EL TFETs.

Jang Hyun Kim and colleagues [12] proposed that TFETs have a SiGe channel, a fin arrangement, and a raised drain to improve the efficiency of their electrical functioning. The ON-state present (I_{ON}) increased by a factor of 24 times higher than that of the Si control set and six times higher than the SiGe management team. Compared to the SiGe control group, the ambipolar current, denoted by I_{AMB}, may be reduced by a factor of up to 900.

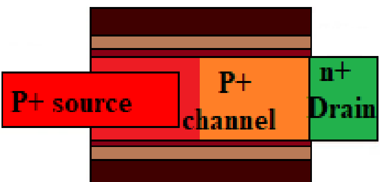

Figure 4: 2D view of Gate overlapped Source Hetro junction Tunnel Tri-gate FinFET[13]

P.Kumar et al.,[13], It has been shown in *figure 4* that this Ge Source hetero setup is applicable for the n-type GoS-HTT FinFET. Considerable increase in tunnelling rate as a result of a more significant overlapped zone with the whole of the channel, and as a consequence, a higher tunnelling rate is achieved. The I_{ON} of 120 A/m and SS of 39 mV/decade utilising an I_{ON}/I_{OFF} of two 10^2 A/ m achieved V_{DD} of 0.5 V. The use of dual-k compounds, which improve noise margins and delay performances while concurrently increasing I_{ON}, is recommended.

3. DEVICE STRUCTURE AND SPECIFICATIONS

The simulation model device structure is a GaSb-AlGaSb JL Fin TFET shown in *figure 5*. AlGaSb material is used for the channel, and Darin, GaSb material is used for the source Control-Gate (CG).

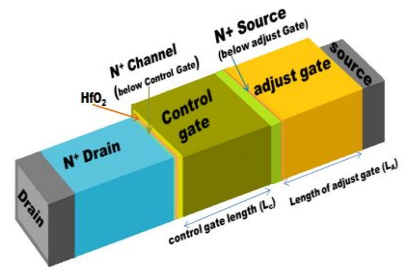

Figure 5: Schematic diagram of a JL FinTFET

Adjust Gate (AG) separation is 5 nm, the silicon film thickness is 5 nm, gate oxide (HfO_2) thickness is 2 nm, and the channel width and source/drain extension width are all 20 nm. This device is a strongly n-type-doped ($1x10^{19}$ cm^{-3}) JL Fin TFET (AG). A layer of native oxide may form on semiconductor materials during high-k dielectric deposition, affecting the interface's electrical properties. The fin-gate technique is employed to enhance channel controllability. The control gate work function is 4.3 eV, and the adjust gate work function is 5.9 eV. The adjust gate is used to modify the device's threshold voltage and, by extension, ON-current. The fundamental premise is to turn the JL Fin TFET's (N+-N+-N+) drain, channel, and source into an (N+-I-P+) architecture without physical doping. In this small bandgap material, *GaSb-AlGaSb JL* Fin TFET is employed. On the source side, *GaSb* is utilised on the source, while *Al GaSb* is used on the drain and the channel.

The *AlGaSb- GaSb* abrupt junction in the JL Fin TFET is created below the control gate, which makes fabrication simpler and eliminates the need to precisely regulate the location of the heterojunction. Similarly, to a p-i-n TFET, the control gate in a JL fin TFET controls electron tunnelling from source to drain by adjusting the tunnelling barrier. A secondary gate (also known as an abrupt gate used to deplete the area underneath it and boost the energy bands, similar to a p-type source. For common mode operations, the p-gate is typically set to zero potential. However, JL-fin TFETs with various channel lengths, thicknesses, carrier concentrations, and source/drain extensions size would necessitate multiple combinations of work functions for Control-Gate and adjust-Gate to get the best possible outcome, i.e., the requisite SS and I_{ON}/I_{OFF} values.

Silvaco Atlas was used for all simulations. Non-local BTBT model to forecast TFET performance [14]. In the simulation, the non-local BTBT model accounts for lateral tunnelling. High channel doping enables the BGN model [15]. The high-k metal gate stack offers the most negligible gate leakage current provided. An SRH recombination model [16] was included due to excessive impurity atoms in the channel and an interface trap effect [17]. The QC and TAT models help explain quantum confinement and interface trap effects on BTBT in TFETs work.

4. SIMULATION RESULTS AND DISCUSSION

Low band gap (Al_XGaSb_{1-X}) materials used in the proposed device decrease the tunnelling energy barrier, as a result, improves the I_{on}/I_{off} ratio. *Figures 6 and 7* show ON and OFF-state band diagrams of $Al_{0.7}GaSb_{0.3}$-Gasb source JL Fin TFET. The proposed device operated in normal mode and direct tunnelling model.

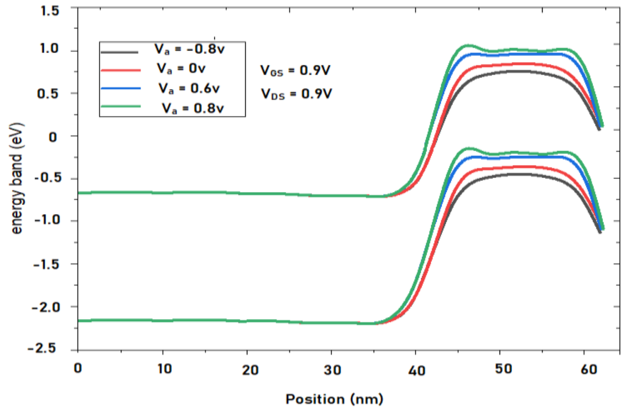

Figure 6. Energy-band of OFF-state (V_{DS} = 0.9 V and V_{GS} = 0 V) at V_{Adj} = -0.8v, 0v, 0.6v, 0.8v

In this normal mode of operation, control and adjust metal gate work functions are changed to optimize performance. The fundamental operation of a Fin TFET device constructed on BTB tunnelling mechanism. Tunnelling barrier height and width mainly considered parameters are in the BTBT mechanism. The input voltage (V_{GS}=0V) of the BTBT is not possible, and also the device is in the off state. When the control gate voltage (V_{Ctrl_Gate}) increased BTBT, the device changed in ON- state based on improved tunnelling barrier height and decreased the tunnel barrier width.

In Direct tunnelling mode, energy band structure and characteristics change by adjusting gate voltage (V_a). *Figure 6* shows that the energy bands below the adjust gate moved by varying the bias voltage (V_{adj}). Negative bias raises the change gate's valence band over the control gate's conduction band. BTB tunnelling starts earlier (at a lower control gate voltage), which is consequential in improving the drive current and ambipolar current is impaired.

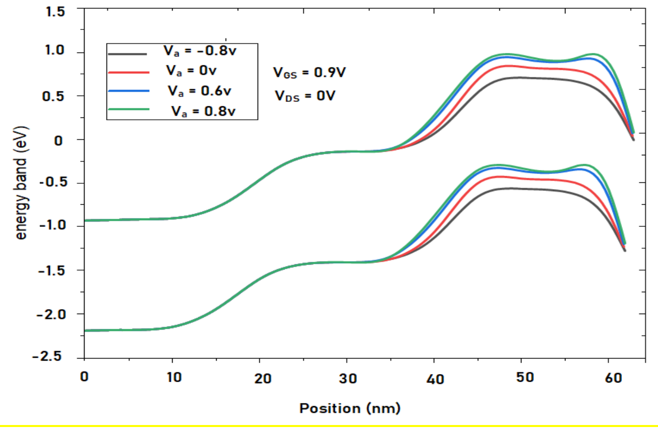

Figure 7: Energy-band of ON-state (VDS = VGS = 0.9 V) at Vadj = -0.8v, 0v, 0.6v, 0.8v)

When the V_{adj} is positive, BTB tunnelling is delayed, resulting in optimum OFF-current but lower ON-current. *Figure 7* demonstrates that for V_a = -0.8 V, the tunnelling energy range (t_h) is more comprehensive, and the energy barrier (t_w) is shorter than for V_{adj} > 0 V. Using the device in direct tunnelling mode enhances the ON-state driving current because of these characteristics. Consequently, improve the magnitude of on-state current by two orders when the V_{adj} is changed from -0.8V to 0.8V.but, off-state draft is slightly altered. Compared to Gasb JL Fin TFET attains better on-state current in AlGasb- Gasb source JL Fin TFET.

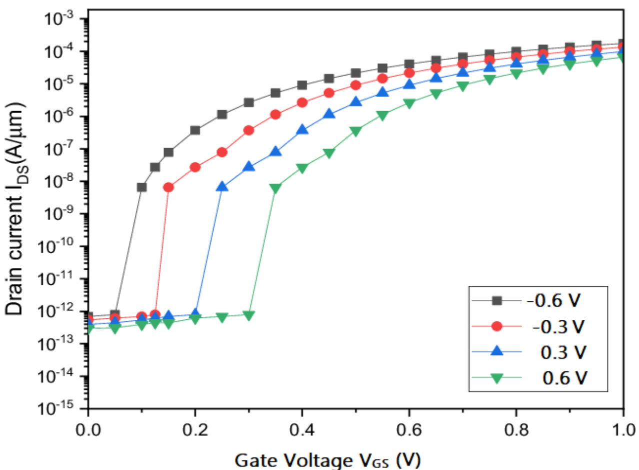

Figure 8: Output current characteristics of Al GaSb- GaSb source JL FinTFET at different adjust voltages(V_{Adj} = -0.6v, -0.3v, 0.3v, 0.6v)

Figure 8 exhibits Si JLTFET and Al0.7GaSb0.3 source hetero junction JL Fin gate TFET transfer characteristics. The graph demonstrates adjusting gate voltage (V_{adj}) affects threshold voltage. Increasing the V_{adj} from -0.6 to 0.6 V approximately doubles the ON-current for conventional JLTFETs. The OFF current hasn't changed much $Al_{0.7}GaSb_{0.3}$-GaSb source JLTFET has a higher ON-current than traditional source JL fin TFET.$Al_{0.7}GaSb_{0.3}$ source JL Fin TFET I_d-V_g characteristics are atypical. When V_{adj} increased from 0.3 to 0.6 V, OFF-current practically doubled. Conventional JL Fin TFET's elements don't show this disparity

4.1 Comparison of GaSb JL Fin TFET and AlGaSb-GaSb JL in FinTFET

The I_{ON} and I_{OFF} currents are shown to be variable through the adjust gate. The design of circuits requiring such dynamic power management may benefit from this. Increases in V_{adj} are recommended for ultra-low power applications since they decrease the OFF-current to negligible levels. V_{adj} may be linked to a negative supply whenever a more significant driving current is required.

The most significant slope of the I_d-V_g curve is the inverse of the point subthreshold swing (SS_{PT}). Since JLTFET's performance is estimated in part by varying V_g, measuring only the SS_{PT} is insufficient. The average subthreshold swing (SS_{AVG}) is a better way to describe the steep curve in a tunnel device.

$$SS_{Avg} = \frac{V_T - V_{OFF}}{I(V_T) - I(V_{OFF})} \quad (1)$$

In Eq. (1), where V_{OFF} is the gate voltage after which the drain current begins to increase abruptly (significant BTBT begins), $I(V_T)$ and $I(V_{OFF})$ are the drain current at $V_{GS} = V_T$, and $V_{GS} = V_{OFF}$, SS_{AVG} calculated.

Extraction of the V_T was performed using the constant current technique with a current of 10^{-7} A/um. Consistent with predictions, both devices show that SS_{PT} is smaller than SS_{AVG} in *figures 9*. Compared to the Si JL FinTFET, the $Al_{0.7}GaSb_{0.3}$ source JL FinTFET exhibits a more minor subthreshold swing. For V_{adj} = 0 V, the SS_{AVG} of the $Al_{0.7}GaSb_{0.3}$ source JL FinTFET was determined to be more than double that of the Si JL Fin TFET. By shifting the adjustable gate voltage from 0 to -0.8v, the SS_{AVG} lowered by 20% in the Si JLTFET and 28% in the $Al_{0.7}GaSb_{0.3}$ source JL Fin TFET. As shown in *figure 10*, applying a negative voltage to the adjust gate causes the slope of the I_d-V_g characteristics to steepen. Enhanced ON-current is the consequence of a more significant subthreshold swing. Privileged OFF-current owing to leakage is to blame for the Al0.7GaSb0.3 source JL Fin TFET's weak SS at higher adjusted gate voltage.

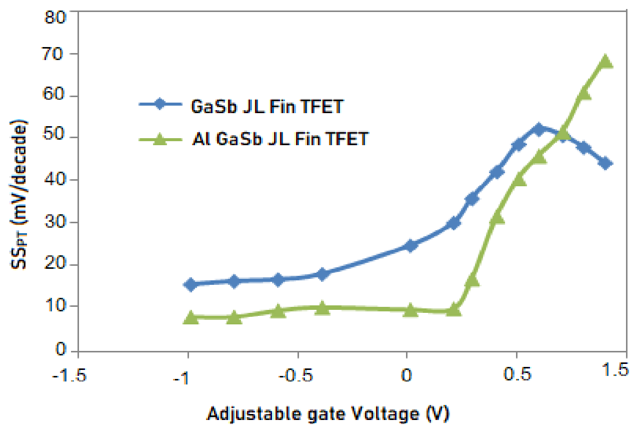

Figure 9: SSPT vs. VAdj for both GaSb and AlGaSb– GaSb Source Junction Less Fin TFETs

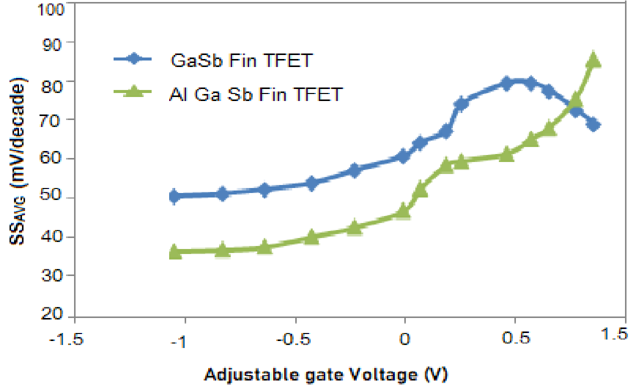

Figure 10: SSAVG vs. VAdj for both GaSb and AlGaSb– GaSb Source Junction less Fin TFETs

5. CONCLUSION

The JL Fin TFET has less OFF current at higher VT to reduce power consumption. The adjustable gate bias affects the JL Fin TFET device performance. Adjusting the drain voltage results in the energy band levels raising or lowering on the drain side at V_{ds}=0V.The ON-current shifts the tunnelling energy range between the source and the channel. Adjusting the VT and other performance factors is as simple as applying a bias V_{adj} to the adjust gate to move back or forward at the start of BTBT. V_{adj} is to be used as a strobe, allowing the device to be used with both minimal standby power consumption and high driving current. The proposed device uses the terminal V_{adj} to optimise its operation for V_{ds} = 0.6 V. When adjusting the threshold voltage of the proposed JL FinTFET, and the adjustable gate acts similarly to the body. Applying a negative gate bias improves the I_{ON}. Leakage in $Al_{0.7}GaSb_{0.3}$ source JL Fin TFETs stopped by using a gate bias of (V_{adj}) less than 0.3 V. By increasing the amounts of x, Al, and III-V in the source area; I_{ON} increased significantly. A GaSb junction less fin gate TFET and an AlGaSb junction less fin gate TFET with variable threshold voltage characteristics are compared. The ON state current is $1.5x10^{-3}$ A/m, the SS is 17.1 mV/dec, and the Iamb is $3.314x10^{-17}$ A/m.

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