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Design of Three-valued Logic Based Adder and Multiplier Circuits using Pseudo N-type CNTFETs

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ABSTRACT- This work presents a novel technique to develop the three-valued logic (TVL) circuit schematics for very large-scale integration (VLSI) applications. The TVL is better alternative technology over the two-valued logic because it provides decreased interconnect connections, fast computation speed and decreases the chip complexity. The TVL based complicated designs such as half-adder and multiplier circuits are designed utilizing the Pseudo N-type carbon nanotube field effect transistors (CNTFETs). The proposed TVL half adder multiplier schematics are developed in HSPICE tool. Additionally, the delay and circuit area for the half- adder and multiplier circuits are investigated and compared to the complementary circuits. The memory usage and CPU time for the proposed circuits are also analyzed. It is observed that the proposed circuit designs show the improved performance up to 43.03% on an average over the complementary designs.

Keywords: VLSI, Ternary logic, CNTFET, Pseudo N-type CNTFET, and HSPICE.

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1. INTRODUCTION

Conventionally, the VLSI digital systems are performed with the conventional logic in Boolean space [1]. Recently, the TVL is used to design the digital circuits because it offers reduced chip-area, low interconnect complexity, reduced digits needed to represent a number, low power dissipation, *etc.* over the conventional logic. The TVL designs using the traditional complementary metal oxide semiconductor (CMOS) technology requires multi-threshold transistors [2]. However, the multi-threshold voltage CMOS transistors are acquired by biasing the bulk terminal. Using the bulk biasing technique to design the TVL circuits is time consuming and complex task. Hence, the researchers looked for alternative technologies such as quantum-dot FETs, reversible logics, single-electron transistors and CNTFETs [3-8]. Out of them, using CNTFET technology is optimistic way to develop the TVL digital logic circuits because the multi-threshold CNTFETs can be obtained by changing the diameter of CNT [2]. Moreover, the CNTFET technology offers 10 times more energy efficiency compared to CMOS technology while designing the circuits.

Using CNTFETs, various TVL digital logic circuits such as basic gates, universal gates, adders, multipliers are presented in existing literatures [7-18]. All these existing designs are developed using complementary CNTFETs. The complementary designs utilize additional transistors that increase the chip complexity [7]. Hence, in this work, the Pseudo N-type CNTFETs are utilized to design TVL circuit schematics. Using Pseudo N-CNTFETs, various TVL circuits are developed in [19]. In [19], only the basic gates and MIN circuit designs are presented. From the analysis, it is noticed that the Pseudo N-type CNTFET TVL circuits shows up to 40% improvement in area with a similar delay on average over the complementary designs. It is worth noting that there are no complicated designs presented. Thus, in this work, the complicated designs such as TVL half-adder and multiplier are presented utilizing Pseudo NCNTFETs. The HSPICE tool is used for verifying functionality and analyzing the performance. Additionally, our proposed TVL adder and multiplier circuit performance are examined with complementary designs.

The major efforts of this work are four namely:

- A technique is presented to design TVL circuit schematic using Pseudo NCNTFETs.
- The numerical equations are stated to calculate CNTFET chirality vectors, diameter, band gap, and threshold value.
- The complex circuits such TVL adder and multiplier circuits are designed.
- Finally, the half-adder and multiplier designs are compared with complementary CNTFET designs.

Rest of the study is arranged as follow: the background of TVL logic and CNTFETs are presented in *Section 2. Section 3* presents the TVL half-adder and multiplier architectures, design, and functionality. *Section 4* describes the performances

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of proposed circuits and its comparison with complementary circuits and the *Section 5* discuss the conclusions of the study.

2. SYSTEM MODEL

2.1 CNTFET based TVL Logic

TVL logic consists of three logic states represented by *logic 0*, *logic 1* and *logic 2* that corresponds to voltage values 0, $0.5V_{DD}$ and V_{DD}, respectively. A TVL function is F(y) mapped from {logic 0, logic 1, logic 2}^{n} to {1ogic 0, logic 1, logic 2}, where y is given as $\{y_1, y_2, y_3, \ldots\ldots\ldots\ldots, y_n\}$. The two-input basic and universal gate functions in TVL y_i and y_j are expressed in *equation (1)*. The detailed discussion on ternary inverter circuits, basic gates and universal gates are discussed in the specialized writings of [7-9].

$$\begin{aligned}
&\overline{y_i} = -y_i + 2 \rightarrow \text{Inverter}\\
&y_i.y_j = min\{y_i, y_j\} \rightarrow \text{AND}\\
&y_i + y_j = max\{y_i, y_j\} \rightarrow \text{OR}\\
&\overline{y_i.y_j} = \overline{min\{y_i, y_j\}} \rightarrow \text{NAND}\\
&\overline{y_i + y_j} = \overline{max\{y_i, y_j\}} \rightarrow \text{NOR}
\end{aligned} \quad (1)$$

Table 1: Calculated CNT diameters and threshold voltages for various chirality vectors

Chirality Vector (p, q)	CNT Diameter (nm)	Threshold Voltage (V)	
		N-CNTFET	P-CNTFET
(8, 0)	0.63	0.69	-0.69
(10, 0)	0.78	0.55	-0.55
(16, 0)	1.25	0.34	-0.34
(19, 0)	1.48	0.29	-0.29

In recent days, the CNTFET technology is widely used to design the TVL circuit because the threshold value of transistor is altered by varying CNT diameter. This excellent property makes the CNTFET compatible for implementing TVL circuits. The CNTFET is different from the CMOSFET in a way the drain region and source region in the FETs are connected. In CMOSFETs, the silicon substrate is connecting the channel, whereas in CNTFETs, the CNT creates the channel. A CNT is rolled graphene layer with a vector $Ch = pi+qj$ where, i and j are the unit lattices. Where p and q define the chirality values of CNT. The CNT acts as a metal when $p = q$ or $p - q = 3i_g$, where i_g is integer, else the CNT is semiconductor. The chiral vectors which are utilized for developing the TVL circuits are placed in *table 1*. This table also provides the relation among the vectors, CNT diameter, threshold values for *p*- and *n*- CNTFETs. The structure of CNTFET and its I-V characteristics for different chiralities are shown in *figure 1* and *figure 2*, respectively.

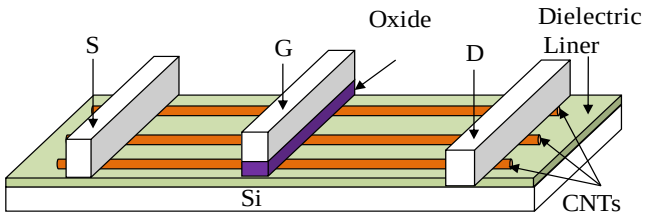

Figure 1. Physical structure of CNTFET

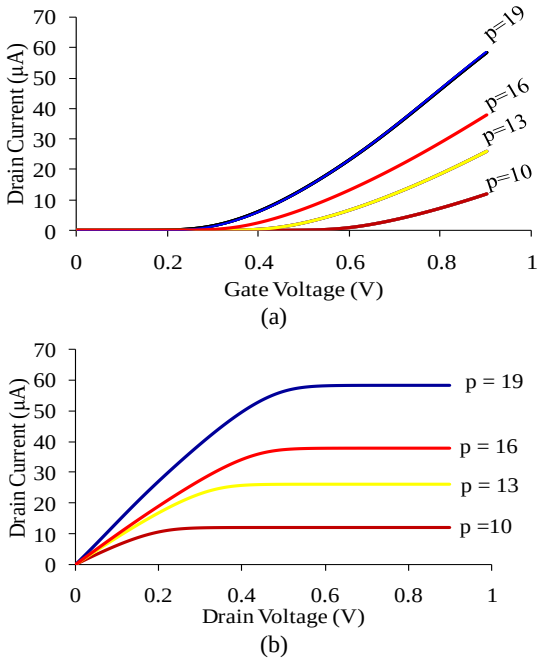

Figure 2. I-V curves (a) IDS vs VGS and (b) IDS vs VDS

2.2 Survey on Existing CNTFET TVL Circuits

Using CNTFETs, the various TVL circuits are developed and presented in [7-19]. In [7], the TVL gates, half adder and multiplier designs are presented. From the performance investigations, it is noticed that the presented designs provide reduced power and delay compared to resistive-load CNTFET designs. The TVL memory cell using CNTFETs are discussed in [8]. The presented TVL memory shows a significant improvement in area up to 41.6% over the CMOS memory cell. In [9], a technique provided to develop the TVL half adder and multiplier circuits. From the results, it is investigated that the half adder improvement of 19.2% and 74.07%, and multiplier shows 24.67% and 81.12% in terms of transistor count and PDP over the existing circuits. The TVL full adder circuit is presented in [10]. The TVL full adder improved the PDP compared to the previous circuits. In [11], the CNTFET based TVL flip-flop is designed using Schmitt trigger. It is noticed that the flip-flop functions correctly and provides high performance over those existing flip-flops. The TVL inverter using CNTFET is designed in [12] and compared its PDP with the resistive load CNTFET inverter. The presented inverter improved the PDP up to 300% over the resistive load CNTFET inverter. The pair of TVL half adder circuits is presented in [13]. One half adder circuit is designed with the conventional technique (*i.e.*, Design 1) and other is developed using the ternary to binary decoder (*i.e.*, Design 2), respectively. It is noticed that the design 2 shows the PDP, power, and delay up to 66%, 63% and 09%, respectively over conventional design techniques. In [14], the 3trit and 9trit adders are designed and compared their performance with the direct realization techniques. Form the results, it is investigated that the 3trit adder shows 79% improvement and 9trit adder shows 88% improvement in PDP compared to the direct realization techniques. In [15], the various TVL logic circuits such as inverter, NAND gate, decoder, adder and multiplier circuits

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developed and compared with existing 15 design techniques. Furthermore, 180 simulations are performed to improve the performance. It is noticed that the proposed designs reduced the PDP and transistor count compared to existing designs. The TVL prefix adders using CNTFET are designed in [16]. Five CNFET TVL adders that utilize different prefix circuits in carry are developed. The result shows that the prefix-adders improved up to 58% of power, 50% of delay and 80% of PDP compared to existing TVL adder circuits. In [17], the complex designs such as half-adder, full-adder, half-subtractor and full-subtractor are developed using CNTFETs. The proposed designs show high-performance over the existing designs. The TVL full adder design is implemented and presented in [18]. The proposed full-adder has improved the power and PDP up to 86.92% and 97% in comparison with two recent existing designs. It is noticed that all these designed using the complementary CNTFETs and only few works are presented on Pseudo N-CNTFETs. In [19], the TVL circuits are presented using Pseudo N-CNTFETs are presented. In this paper, only the basic gates are presented and no complex circuits are designed. Hence, in this paper, we developed the complex designs such as half-adder and multiplier using Pseudo N-CNTFETs.

3. PSEUDO N-CNTFET BASED TVL ADDER AND MULTIPLIER CIRCUITS

The TVL gates presented in literature paper [19] is used to develop the various complex circuits such as adders, multipliers, subtractors and so on. In this work, we developed the TVL half-adder and multiplier as complex circuits. To design theses complex circuits, a TVL decoder shown in *figure 3* is utilized. The output of TVL decoder is stated by

$$y_r = \begin{cases} 0, \text{if } y = r \\ 2, \text{if } y \neq r \end{cases} \quad (2)$$

Where r is TVL states. This decoder is designed using the one positive TVL NOT gate, two negative TVL gates NOT and a universal NOR gate.

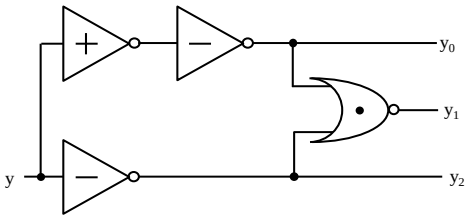

Figure 3. Circuit schematic of TVL decoder

Table 2: Truth table of half-adder and multiplier

Input x	Input y	Half-Adder		Multiplier	
		Sum	Carry	Product	Carry
0	0	0	0	0	0
0	1	1	0	0	0
0	2	2	0	0	0
1	0	1	0	0	0
1	1	2	0	1	0
1	2	0	1	2	0
2	0	2	0	0	0
2	1	0	1	2	0
2	2	1	1	1	1

The major advantage of TVL is to speed up the computations. Since the TVL consists of three logic states, the number of digits needed for TVL family is $\log_3 2$ which less than the binary logic. Thus, N bit is considered for binary logic, whereas the $\log_3 2$ is considered for TVL logic.

3.1. Pseudo N-CNTFET based TVL Half Adder Design

A TVL half adder is developed to validate the correctness of the Pseudo N-CNTFET design. *Table 2* shows the TVL half adder truth table. The transient response equation for TVL adder is expressed as

$$\text{Sum} = 2 \cdot (x_2y_0 + x_0y_2 + x_1y_1) + 1 \cdot (x_2y_2 + x_1y_0 + x_0y_1) \quad (3)$$

$$\text{Carry} = 1 \cdot (x_1y_2 + x_2y_2 + x_1y_2) \quad (4)$$

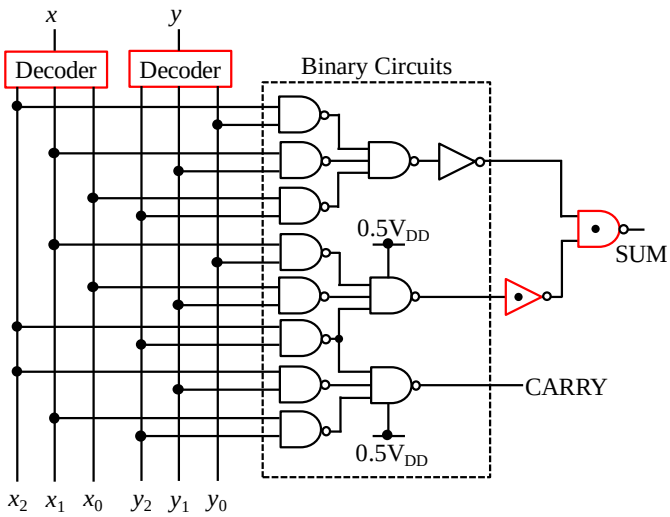

Figure 4. Proposed TVL half adder

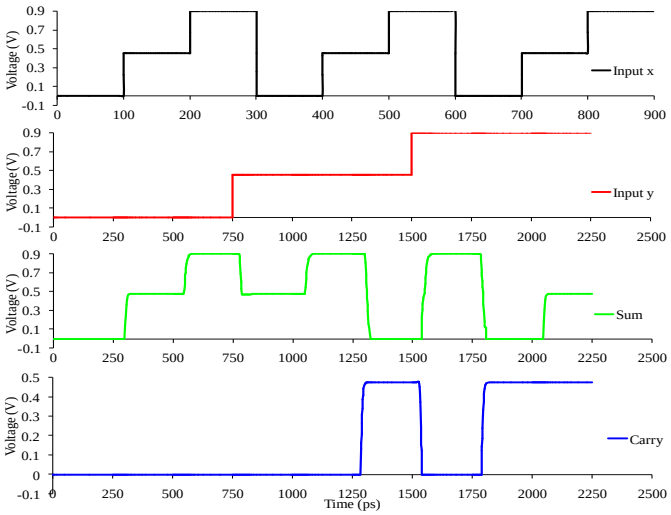

Figure 5. Transient response of TVL half adder

The circuit schematic of TVL half adder using Pseudo N-CNTFETs is shown in *figure 4*. In *figure 4*, the decoder provides the unary outputs for the inputs and the logic gates computes

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the functions of *equations (3) and (4)*, respectively. The industry standard HSPICE simulator is used to develop the proposed Pseudo N-CNTFET based circuits using CNTFET SPICE model presented in [20-21]. This model conceives a real and circuit-compatible CNTFET for SPICE simulations and considers realistic device non-idealities. *Figure 5* shows the response of TVL half-adder. It is noticed that the TVL adder operates correctly according to *table 2*. Furthermore, the performance of TVL adder is also noticed in terms of propagation delay and circuit area. The obtained delay and circuit area for the proposed Pseudo N-CNTFET based half adder are 102.2ps and 4.1fm^2, respectively.

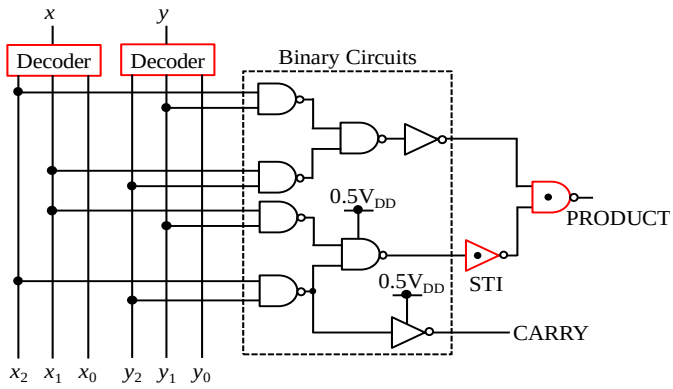

Figure 6. Propose TVL Pseudo NCNTFET based Multiplier

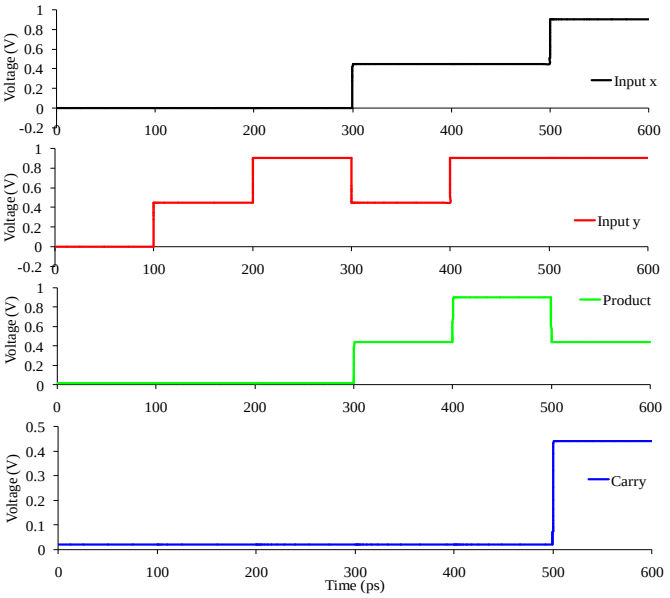

Figure 7. Output response of proposed TVL based multiplier

3.2 Pseudo N-CNTFET based TVL Multiplier Design

A TVL multiplier circuit is also developed and validated the correctness with its truth table presented in *table 2*. The transient response equation for TVL multiplier is stated as

$$\text{Product} = 2 \cdot (x_1 y_2 + x_2 y_1) + 1 \cdot (x_1 y_1 + x_2 y_2) \quad (5)$$

$$Carry = 1 \cdot x_2 y_2 \quad (6)$$

The circuit schematic of TVL multiplier using Pseudo N-CNTFETs is shown in *figure 6*. The output of multiplier is shown in *figure 7*. It is noticed that the proposed multiplier operates correctly according to truth table given in *table 2*. Furthermore, the performance of multiplier is also evaluated in terms of propagation delay and circuit area. The obtained delay and circuit area for the proposed Pseudo N-CNTFET based multiplier are 95.2ps and 3.4fm^2, respectively.

4. PERFORMANCE STUDY OF PROPOSED CIRBUITS WITH COMPLEMENTARY CIRCUITS

The performance such as delay and circuit area of Pseudo N-CNTFET designs are examined with complementary designs to show the efficaciousness of proposed method. For complementary, the CNTFET diameters 1.48nm, 1.01nm and 0.78nm are used and their threshold voltages are 0.28V, 0.42V and 0.55V, respectively. The TVL half-adder and multiplier are developed by CNTFETs. *Figure 8* shows comparisons of proposed and complementary designs. The proposed designs improved the delay, and circuit area up to 34.73% and 25.04%, respectively for half adder 30.30% and 20.18% for multiplier over the complementary designs. Moreover, the memory usage and CPU time for the proposed circuits are investigated. Using the I7–2600 processor with 3.4 GHz frequency and 8 GB RAM, the CPU time and memory usage are investigated and shown in *figure 9*. The Pseudo NCNTFETs based TVL circuits shows reduced memory and CPU time compared to the complementary based CNTFET designs. Hence, the utilizing Pseudo CNTFET designs for TVL applications provide high performance compared to complementary designs.

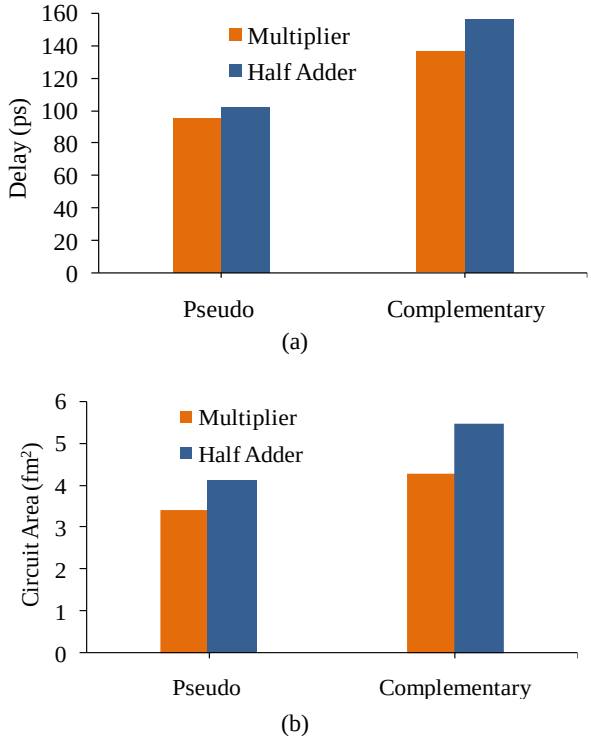

Figure 8. Performance comparison of multiplier and half adder (a) Delay and (b) Circuit area

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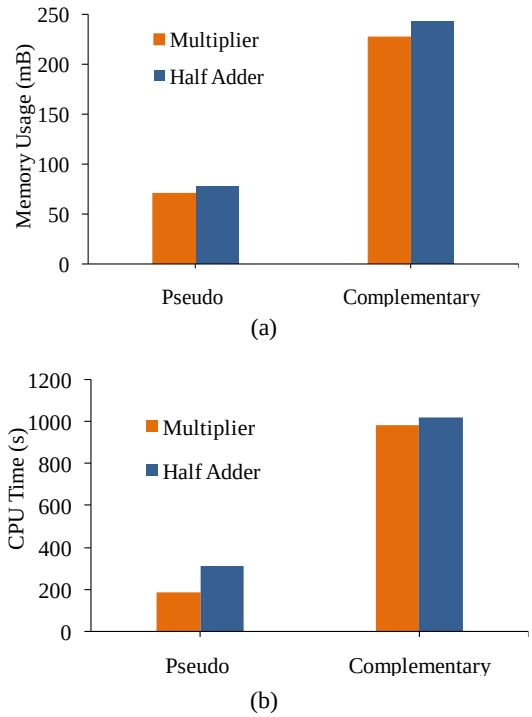

Figure 9. Pseudo N-CNTFET based TVL multiplier and half adder (a) Memory and (b) CPU Time

5. CONCLUSION

A novel TVL circuit schematics are presented in this work. The TVL based half adder and multiplier circuits are developed utilizing Pseudo N-CNTFETs because the CNTFET threshold voltage values are altered by the CNT chirality vector. All the proposed circuit designs are developed and simulated in HSPICE. The performance parameters such as circuit area and delay of the proposed designs are also analyzed and improved up to 32.5% and 22.6%, respectively compared to the complementary CNTFET circuit schematics. Furthermore, the memory usage and CPU time consumed for the proposed designs are investigated and improved up to 68.4% and 75.13%, respectively over the complementary designs. Thus, using the proposed technique is a best solution for designing TVL logic applications.

Conflicts of Interest: No conflict of interest

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