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High Switching Speed and Low Power Applications of Hetro Junction Double Gate (HJDG) TFET

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ABSTRACT- Tunnel field effect transistor (TFET) technology is unique of the prominent devices in low power applications. The band-to-band tunnel switching mechanism is sets TFET apart from traditional MOSFET technology. It helps to reduce leakage currents. The major advantage is the Sub threshold slope smaller than 60mv/decade. Newer technologies are expected to change the gate, architectures, channel materials and transport mechanisms. In this point of view tunnel FET has to play the most imminent role in the least leakage current and also need to overcome limitations of drive current in TFET. The proposed model of hetero junction double gate TFET has attain superior ON state current, low off-state current and better steeper slope i.e., 4.94 x10^{-5}A/µm, 32.3 x10^{-17A}/µm 28.3mv/decade as compared with single gate hetero junction TFET and conventional device. This proposed design suitable for high switching speed and low power application.

Keywords: TFET, Band to band tunnel, Sub-threshold slope, Hetero Junction Double Gate (HJDG), ON-sate current.

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1. INTRODUCTION

The current state of the art of VLSI design proposes a new transistor technology that can function with a low voltage and power budget, improved performance, and enhanced logic density. For the past decade, the steep transistors used in VLSI circuits have switched on and off at extremely low voltages is shown in *figure 1*. As per the industry standards, the voltage has been reduced to 0.3V-0.5V and the switch current level by a factor of 6. Technology scaling in conventional MOS devices causes short-channel effects (SCEs). The subthreshold slope is the reciprocal value of the subthreshold swing [1]. The device structures are decreasing beyond the limitations as a consequence of huge developments in nanotechnology. This cause insufficient gate control over the channel at 300 K, which leads to the progressive growth of SCEs in the device [2]. Using a TFET is one of the options that have gained the greatest notoriety in recent years. The switching mechanism of TFETs is entirely distinct from that of conventional MOSFETs [3]; specifically, in TFETs, the current flow operation is based on gate-induced BTB tunnelling. This is compared to conventional MOSFETs, which use a mechanism that is based on channel tunnelling. The development toward nano-scale technologies is seen in *figure 1*. The subthreshold slope (SS) of TFETs may be made to be less than 60mV/decade at room temperature [4], which is one of the key technical barrier criteria that must be met, and these results in a lower off current [5].

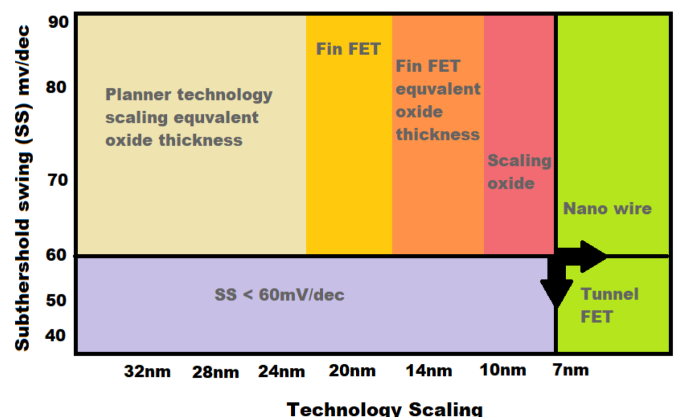

Figure 1: Correlation between technology scaling and SS

In this paper organized as: *section I* examines introduction of different technology scaling and steeper slope transistor and also compared conventional device. *Section II* explains literature survey on improving ON-state current in various tunnel FETs based on gate structures and materials. *Section III* explains design parameters and simulation models. *Section IV* section explains the results and discussion of hetero junction DGTFET design. *Section IV* section explains conclusion of the proposed device.

2. LITERATURE REVIEW

2.1 Based on Tunneling Mechanism

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Extensive and detailed speculative revisions have been conducted to investigate the speed of turn-on of line TFETs in demand on source doping, gate alignment pocket doping, oxide thickness, and materials. Whenever it comes to the performance of silicon TFETs, as reported by Sandow et al. [6], the gate is commonly linked with either the P-type to intrinsic or the N-type to intrinsic tunnelling interface. The distinctive tunnelling process that Matthias Schmidt et al.,[7] describe as being dependent on gate orientation.

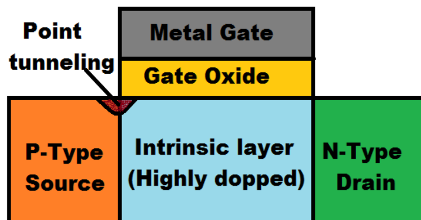

Figure 2: Point tunneling

In *figure 2*, it is illustrated that the low-charge carrier BTBT generation rate shown in the tiny (point) tunnelling region of the source to channel junction is referred to as "point tunnelling".

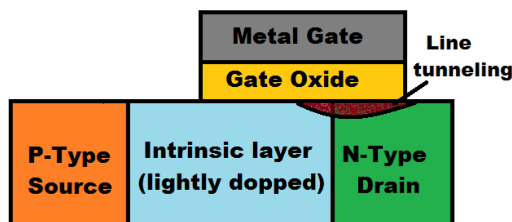

Figure 3: Line tunneling

In *figure 3*, it is shown that the gate in this device is overlapping the source, which affects higher charge carriers. The rate of BTBT generation that occurs in a large (line) tunnelling region from the gate overlap source section to the channel junction is referred to as "line tunnelling" The key benefit is that LTFETs provide more tunnelling current. It was suggested that using LTFETs might increase device performance [8].

2.2 Related the Source Location and Gate Edge

E.-H. Toh and G. H. Wang [9] addressed the necessity of the LTFET appearing as a source edge operation. Change the placement of the source limit such that it is now at the overlapped source gate rather than the under lapped source gate. The significance of where the source hetero junction I_{ON} and I_{OFF} are located in the system. The I_{ON} current of the hetero dielectric structure is strongly influenced by the source position, in contrast to the Low Spacer and Low Gate dielectric structures and the High Spacer and High Gate dielectric structures. The findings show an improvement in the I_{ON} current by 3 nanometres, under lapping the source dialectic with the gate dielectic. The source doping spreads out till it reaches the gate-managed channel area. During this time, the source's p-type continuous doping tail restricts the gate's ability to affect the area of n-type organized inside the channel that is located on the source side.

2.2.1 Silicon thickness

Costin Anghel, Hraziia [10] *et al.*, demonstrated that the increase in the I_{ON} current in response to the thickness decrease of the silicon layer t_{Si} is a necessity for long-term stability between the currents of conduction I_{ON} and t_{Si}. The maximum possible value for the thickness of silicon silicon denotes the notation $t_{Si\ MAX}$.

2.2.2 Decrease the ambipolar currents

One way is called "under lapping," and it involves the gate and the drain working together. In addition to reducing the amount of undesirable ambipolar tunnelling current, this also cumulatively expands the tunnelling space. Another one is going to be made up by reducing the amount of doping that is in the drain. Both the source and the drain have the same level of doping in their respective concentrations. As a consequence of this, the number of ways for establishing current may be reduced in the construction of LSHG opposing circuits, and the number of masks that need to be reduced is required to be reduced to a minimum. The drain side fringing capacity goes down when the LSHG is used, which also has consequences.

2.3 Based on Structure and Material in TFET

In [11] K. H. Kao *et al.*, The fully overlapped device manufactures the utmost ON-currents; however, the non-overlapping device on the channel differs from further potential barriers. ON-current distinction for the three types of LTFET. It main depends on two style factors to decrease tunnel path. One is supplying concentration, that result smallest tunnel methods area unit shrivelled as a result of the improved electrical field and another one is Equivalent compound thickness (EOT) of gate-insulators with ever-changing insulator constant to remember the matching fringing field capacitance result, The leakage (OFF) current is freelance of the EOT as a effect of its directed by the minority drift current.

In [12] Woojin Park *et al.*, explains that the 3 nm tunnel gap LTFET shows it has improved the drive current of the standard TFET. Due to improve in drive current of LTFET, it has the extra electron producing area. These total tunnel-gap-line increases provide seven times improvement in the drive current. During OFF-state, the LTFET has large potential barrier and has less subsequent OFF-current. During ON-state, there is increase in the gate voltage results in fall of barrier potential and barrier height, results in subsequent injection of carriers. There are mainly two different benefits of BTBT fragments. One of them is, the point tunnelling fragment, *i.e.*, tunnelling occurs at the point of central and the entire drive current is moderately contributed. Another one is, the line tunnelling fragment *i.e.*, each sideline in the schematic of the point tunnelling portion, it is the critical factor that can establish the working device.

In [13] Xiangzhan Wang *et al.*, Used as a gate to extend the TFET tunnelling field strength. This sometimes bases the reduction of the fringe-induced barrier (FIBL) and the decrease of its sub-threshold features gate field plate TFET is planned to increase the driving current and conquer the FIBL-induced present.

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In [14] Jyi-Tsong Lin *et al.*, a recessed-gate TFET is determined to expand the present of TFETs by extending the tunnel region with line tunnelling. In this exploring the impacts on device efficiency of recessed-body density and doping level. This ideal device structure, here recommended n-TFET influences $1.44\text{x}10^{-6}$ A/µm present and $3.22\text{x}10^{9} I_{ON}$ / I_{OFF} ratio.SS_{min} = 28.3 mV/dec and SS_{avg} = 59.8 mV/decade over drain current are generated.

The tunnelling occurred in LTFET is homogeneously besides of the gate length in the channel that defines in the improvement in the SS and ON-state of the device in this region. In pocket tunnelling traps are located near end of the source that low tunnelling traps cause to reduce SS [15]. Based on mechanism the pocket tunnelling traps are situated into two regions. Among those regions One is near the interface of channel substrate–gate oxide region and second one is bulk pockets region.

In [16] Muhammad Elgamal *et al.*, proposed that the primary objective of a design is the gate contact has tight-fitting to accommodate channel controlling. In order to efficiently increase I_{ON} through cumulative tunnelling, another extra technique for such control is to either diminution the dielectric thickness of the gate, use HfO_2 material for high dielectric constant. Inverse, the direct tunnelling via the gate constrains the dielectric thickness decrease of the gate. The two distinct gate materials are indicated to be used to develop the control of I_{ON} and I_{OFF} [17]. The better performance of device in both SiO_2 and HfO_2 overlaps. Based on these measurements, achieving an ON / OFF ratio of 5.5 times and a SiO_2 SS of 49.5 mV/decade is higher as a dielectric overlap source than HfO2 when the dielectric gate is HfO_2.

The InGaN HTFET is a source-side channel transistor used for I_{ON} development and SS reduction. This work is described in reference [18]. The channel length (L_{ch}) and channel thickness (t) are 50 and 10 nm, respectively. The drain metal and the gate (LDG) are both 100 nm in size. Al_2O_3 with a thickness (t_{ox}) of 3nm is used as the gate dielectric material. The doping quantities in the source are $p+$ type $9.9\text{x}10^{19}$ cm3, in the channel are n type $1\text{x}10^{15}$ cm3, and in the drain area are $1.2\text{x}10^{19}$ cm3 for the n+ type.

In [19] Chun-Hsing Shih et al, proposed that the design of line TFETs using low- band gap materials (*i.e*. Ga, InSb and InAs) to solve the ON current disputes. The V_{out} is fewer than the voltage of the bandgap to obtain low OFF (leakage) current. Line tunnelling arise the overlapping of the gate into source region, the gate terminal is triggered by conduction current normal to the channel. The line-tunnelling phenomena used in device architecture to rise the I_{ON}. The generation-recombination model Shockley–Read–Hall (SRH) is used to reduce leakage current [20].

In [21] Paula Ghedini Der Agopian et al, describe that the LTFET demonstrate that improvement of intrinsic voltage gain (A_V) and on-current compared with both FinFET and GAAFET technology. A number of research works is done through different combination of materials and geometries are used in a device to reduce the problems of low on-current and high subthreshold swing [22]

3. DEVICE STRUCTURE AND SIMULATION SETUP

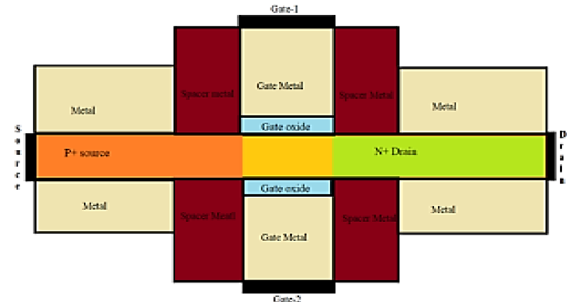

Figure 4: Double gate Hetero junction TFET

The simulation setup of an n-channel DGHJTFET is illustrated in *figure 4*, with doping concentrations of 10^{19} cm^{-3} for the P-source and 10^{17} cm^{-3} for the n-drain, and 4.6 eV for the metal gates, length of the SiO_2 layer and spacer (HfO_2) is 3 nm a 7 nm. Channel length and width 100nm and 5nm. Low band gap materials (*i.e*. AlGasb/InAs) are used in the proposed device. The front gate is normally linked to the device's top side, while the rear gate is often attached to the device's bottom side. There is dual-gate control at exactly the same time on two channels where current may flow, the I_{ON}/I_{OFF} ratio and SS are improved. The BTB tunnelling model was used in the proposed structure. In constant mobility, auger recombination models are used the device.

4. RESULTS AND DISCUSSION

Figure 5 illustrated, based on the simulation parameters and models generated 2D view of Hetro junction double gate TFET in TCAD visual output. *Figure 6*, Compares of I_d-V_{gs} characteristics of TFET, hetro junction TFET and proposed device at V_{DS} = 0.5 V. Non-local BTB tunnelling (NL BTBT) across the tunnel barrier is visible, as is the general bipolar character of the current flow. proposed DGHJ TFET has perform better electrical characteristics *i.e.*, low off state current, high drive current and steeper slope as compared to other two devices.

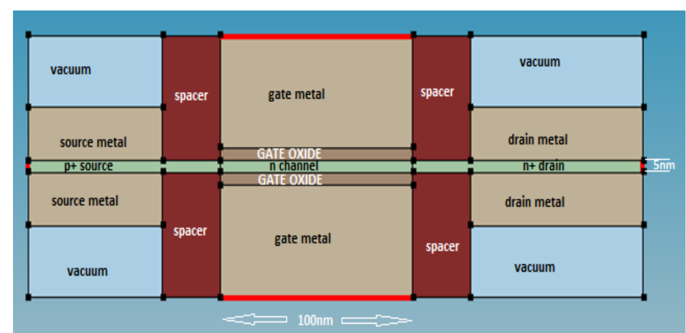

Figure 5: 2D view DG Hetero junction TFET in sentaurus TCAD Visual

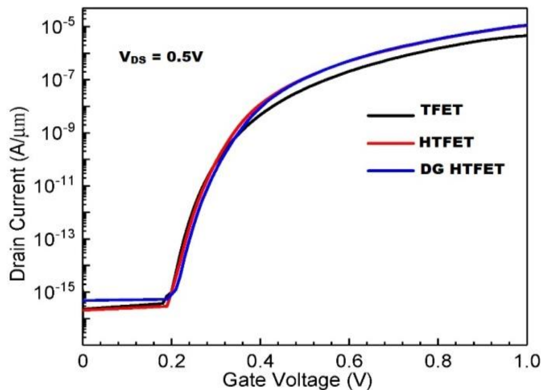

Figure 6: I_D-V_{GS} characteristics of DG Hetero junction TFET at V_{DS}=0.5V

The energy barrier is narrow enough in this state for electrons to tunnel from the valance band of the p+ area to the intrinsic region's conduction band and gate controlling, tunnelling area of the proposed device large.

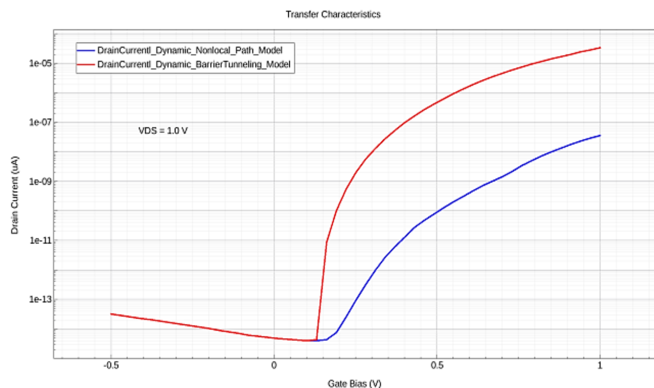

Figure 7: I_D versus V_{GS} characteristics comparison of TCAD simulation models for DG HTFET at V_{gs}=0.1V

Figure 7 compares the I_D versus V_{GS} characteristics of DGTFETs using the drain current dynamic nonlocal path model and the drain current dynamic barrier tunnel model. Because the barrier height varies with the applied voltage, the dynamic barrier tunnel model outperforms the dynamic nonlocal path model. The energy barrier is narrow enough in this state for electrons to tunnel from the valance band of the p+ area to the intrinsic region's conduction band. V_{DS} = 1.0 V. NL BTBT across the tunnel barrier is visible, as is the general bipolar character of the current flow.

4.1 Device Performance Comparison

Table 1: Electrical parameters of TFET, HJ SGTFET and HJ-DGTFET

Parameter	Conventional TFET	HJ SGTFET	HJ DGTFET
SS [mv/dec]	43.9	33.5	28.3
I_{on} [µA/µm]	33.8	42.6	49.4
I_{off}[PA/µm]	40.3	35.2	32.3

Table 1 shows in Comparison of performance of TFET, HJ SGTFET and HJ DGTFET devices. The device performance characteristics of both TFET, HJ-SGTFET devices are compared with DG-HTFET devices. The findings show that when high-k gate materials are used instead of typical SiO2, the drain current performance improves. Because of the better electrostatic field within the tunnelling zone, the threshold voltage (V_{th}) of HJ-DTFET decreases with a high-k gate. This is also a scientific indicator that the power supply should be reduced. The output characteristic improves with increasing drain voltage and reaches its optimal value for drain voltage V_{DS} of 1.0 V. High-k enhances output characteristics at low gate voltages on the order of 0.5 V. An increase in the V_{DS} boosted the I_{ON} current significantly but had no impact on the threshold voltage.

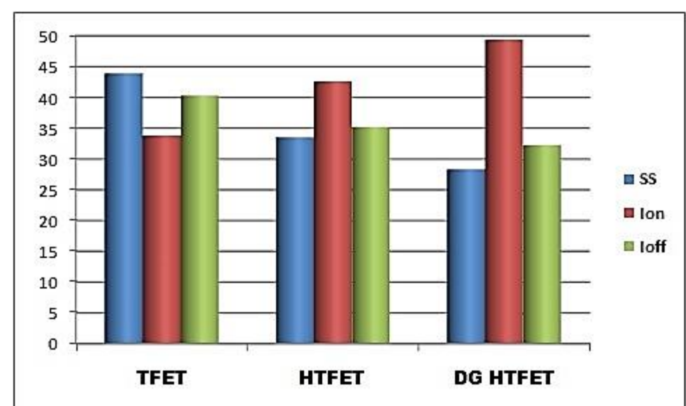

Figure 8: Performance comparison of TFET, HJ SGTFET and HJ-DG TFET

Figure 8 illustrated the high drive current (Ion) in proposed device has 4.94 $x10^{-5}$A/µm and single-gate-hetro-junction TFET has 4.26 $x10^{-5}$A/µm as compared with conventional device. The increased SS value of the DG-HTFET device is 28.3mv/dec ascribed to the expanded tunnelling area and greater gate control in the overlap zone, which results in an increase in drive current.

5. CONCLUSION

In this work, the proposed device has attained superior ON state current, low off-state current and better steeper slope i.e., 4.94 $x10^{-5}$A/µm, 32.3 $x10^{-17}$A/µm 28.3mv/dec as compared with single gate hetro junction SGTFET and conventional device. This proposed design suitable for high switching speed and low power application.

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