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Design and Implementation of a Bootstrap-based Sample and Hold Circuit for SAR ADC Applications

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ABSTRACT- The resolution and conversion speed of an Analog to Digital converter (ADCs) strongly depends on how efficiently Sampling and Hold (S&H) circuit handles the amplitude skewing of the input analog signal. In this article, a novel S&H circuit has been proposed to handle the errors produced because of amplitude skewing. This circuit has two different paths for sampling and holds process and avoids the non-ideal effects seen in most of the recent literature. In portable applications, the restrictions on the available power and the importance of the quality of digital data are taken as a challenge. To make SAR-ADC more power efficient, all blocks should be designed with low-power techniques. Here, the sample and hold block need to be designed to the optimized power level, operate supply of 3.3V, implemented with SCL 0.18µm process, operating at a sampling rate of 10MHz with the power of 0.425mW.

Keywords: Analog to Digital Converter (ADC); Digital to Analog Converter (DAC); Successive Approximation Register SAR, Mega Sample Per Second (MSPS); Signal to Noise Distortion Ratio (SNDR).

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1. INTRODUCTION

Simple audio devices to the Internet of Things use ADCs as their interface between the real analog world and the digitalizing world (IoT) [1]. The complete block diagram of SAR-ADC works on the binary search algorithm shown in *figure 1*. These core blocks include a comparator, a successive approximation logic register (SAR), a digital-to-analog converter (DAC), and a sample-and-hold circuit. The input analog signal is supplied directly to the S&H block, and one of the comparator inputs receives the output signal of the sampled and hold operation. The DAC block is the comparator's other source of input. After the comparison process, the comparator output at either logic '0' or logic '1'. It will go to SAR Logic, and in the SAR register, the operation will be done based on the binary search operation basis. Here initially keeping MSB as logic '1', then, it starts the comparison process concerning the output bit of a comparator. If the comparator output bit is coming as logic'1', then the current bit will be left as it is, and the comparison will move on by making the next bit in the register to logic '1'. If not, the current bit will be masked to logic '0', and the comparison will be made with the next bit, and so on this way, the complete conversion process will be completed, and the final conversion output will be obtained at the final step.

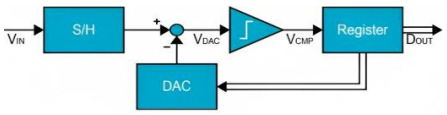

Figure 1: SAR converter basic Diagram

Analog non-DC signal is applied to the converter to digitalize, and converter conversion time is finite. Over this finite conversion period, the input analog signal amplitude changes. Due to this rapid and large amplitude skewing, the resolution of the ADC is quite disturbing.

Hence the S&H should be designed to properly sample the input signal and hold it over the conversion period. In the design of the sample and hold, switch and circuit noise and nonlinearities should be suppressed enough. Low-power designs also need to be included, as converters are very popular in battery-operated IoT applications [7]. The state-of-the-art of S&H circuits has been discussed here.

The remainder of the essay is structured as follows. *Section 2* is a review of the literature. *Section 3* Represents the basic operation of the sampler circuit; *Section 4* represents the issues in the parameters of the S&H block; *Section 5* represents the results and discussion. The conclusions are presented in *Section 6*.

2. LITERATURE REVIEW

ADCs Architectural changes unveiled many circuits like low-gain two-stage amplifiers, reducing mismatch and settling

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errors in the first SAR stage by using a sub-binary DAC. A prototype model 1V-12-bit, 160MS/s streamed SAR-ADC demonstrated in a 40nm Complementary MOS process. Low gain two-stage amplifier produced gain errors [2]. The dual-phase bootstrap technique was used in a pipelined- SAR-ADC and improved the sampling and conversion linearity. This had a small wide area, wide coverage, and excellent accuracy of 0.068 mm2. Implemented in 65nm CMOS technology, operated at a supply of 1.2V, and achieved SNDR of 60.9 dB and 6mW of power dissipation [3]. A 9-bit ADC architecture was discussed in [4]. MOS capacitors were used in DAC capacitive elements and fabricated with 0.13µm technology, operated at 0.6V supply. The achieved ENOB was 7.9 and a power of 228µW. The concept is based on the statistical behavior of the low-activity signals, and the difference between two adjacent sample points is around zero. Designed a 1.8V, 10-bit SAR-ADC. Hence, the power saving was boosted by concentrating on the difference between two adjacent sample points rather than the sample point itself [5]. A significant amount of design area was reduced by employing a split type of DAC employed in SAR-ADC designed in 0.13µm operated at 5.5V. This scheme reduced the capacitors count nearly 14 times the conventional CDAC [6]. A 10-bit SAR-ADC has decreased average switching energy in CDAC by 90% since it was introduced with an adaptive reset switching strategy. The linearity was also improved by employing near-threshold voltage and bootstrapped techniques in S&H. The achieved ENOB was 8.7 ENOB [8]. To enhance the accuracy, Energy-saving techniques such as DAC switching and a comparator with dynamically adjustable current have been used in 0.13um,1.2V SAR-ADCs. The linearity also improved here without adding capacitors or calibration logic [9]. To enhance the speed, a two-stage dynamic latch comparator with adaptive power control (APC) technique was designed. Common mode charge redistribution algorithm and synchronous SAR logics blocks were employed [10].

A 1.2V,10MHz digital sub-ranging ADC architecture was proposed in [11]. A FET-based S&H was proposed to eliminate the different types of distortions at a sampling rate of 6 MHz; MKV FET dominates the distortions like second order. This configuration showed improved speed, power consumption was 16mW at 1.2V supply, and achieved SNR =46 dB and SFDR= 55 dB. A 9-bit SAR-ADC with 700Ms/s has been designed at 65nm process and obtained ENOB of 8.3 bits @10MHz frequency along with power consumption in 5.9mW [12].

3. CIRCUIT FOR SAMPLING AND HOLDING

S&H is the first block in any kind of ADC. It involves achieving high-speed, high-resolution ADCs Converters, which sample a particular Analog signal and holds it for a predetermined amount of time while it is processed by a following circuit. A basic sampler circuit consists of a switch and a capacitor, as shown in *figure 2*. S&H's main function is the sampling of the input analog signal and holds this value across the sampling capacitor. This produces different non-ideal effects in the conversion process. The S&H circuit's three primary features are acquisition time, aperture time, and settling time.

The time between the circuit enters the sampling mode until it starts the input signal tracking is the acquisition time. This is a result of the hold capacitor's value, the switch's series resistance, and the signal path. The small interval between the circuit exits hold mode and stops following the input signal; the value being held is the aperture time. This is the function of drivers and switches in the circuit propagation delay. The jitter or uncertainty in this time duration is mainly due to the variations in the clock and the noise produced by the signal and switch. The time necessary for the circuit to enter and remain within the permitted error band about the hold value after entering the hold mode is defined as the settling or hold settling time. The holding step, also known as the pedestal error, is a potentially undesirable charge transfer that occurs between the switch driver and the hold capacitor during the settling phase. The simple operation of the circuit is that when $C_K=V_{DD}$, the NMOS device is ON, the input signal is allowed to pass to the output side, and the capacitor C_1 starts charging towards Vin, called sampling mode. When $C_K=0$, the NMOS device is OFF, and the voltage across C_1 starts discharge is called hold mode. M1 switching speed strongly depends on its ON resistance and is given by the *equation 1*.

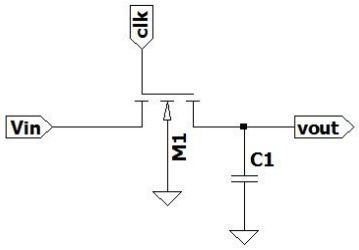

Figure 2: Basic sampling circuit

$$R_{on} = \frac{V_{DS}}{I_D} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{DD} - V_{in} - V_{TH})} \quad (1)$$

The equation shows that device ON resistance is a function of an input signal. When Vin ≈ V_{DD}-V_{TH}; Ron → ∞. This tells the input range is quite limited and is a very critical issue considered in nanometer designs [13]. To reduce the input range limit effect, a transmission gate switch was used [14]. Here, the PMOS type M_2 switch is connected in parallel with M_1, which is wider than M_1, hence ON resistance dependency on input voltage red. Due to mobility degradation with the vertical field in the channel, the net ON resistance of the switch still varies concerning Vin. Capacitive feedback type S&H presented in [15] has three switches to regulate the sampling and amplification process. During the sampling period, switches= 2=ON &3=OFF. The potential at the node 'X' is set to a value of 0, hence the potential at the other side of capacitor=Vin. When the switch 3=ON, the switches 1= 2 =OFF, the feedback forms, and the potential Vout is the same as the input voltage Vin and this voltage is held till the end of the sampling period. To minimize the influence of the charge injection during the switch closed, a short delay between the switches is to be maintained during the case of 1= 2=ON& 3=OFF. Usually hold step magnitude is in the millivolt (mV) range, and the non-linear effects are minimized by keeping a full-scale range of the signals. To enhance the linearities in the converter with reduced

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power consumption, a bootstrap technique has been presented in the open literature, and its concept is presented in *figure 3*.

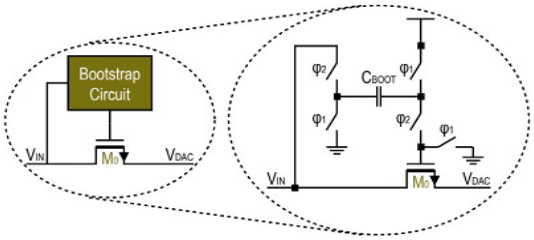

Figure 3: Bootstrap switch concept

Here, the NMOS device acts as the switch [16]; it should be open during the hold phase and close during the sampling period. The bootstrap control circuit is formed with five switches; it regulates the transistor gate potential by providing a fixed potential between the gate and the source. Where φ1=nMOS and φ2=nMOS type switches, as shown in *figure 4*.

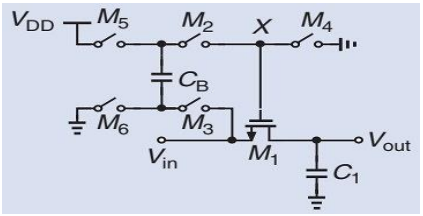

Figure 4: Bootstrap switch [14]

Design CB to provide the constant gate potential to M1 and make a smooth switching action, and the charge across CB should be periodically refreshed. During the sampling period (track mode), M_2 & M_3 should be turned ON, and the charge across CB should make M_1 to ON. During the hold mode, M_4 & M6 should turn ON, and M_3 &M_2 should disconnect CB from M_1. Hence CB should research V_{DD} *via* M_5 & M_6 [16]. Since M_4 is ON, the M_1 gate is grounded. To increase bootstrap switch linearity, the switch should provide stable ON conductance; for this, the sampling transistor, M_{10} gate, to source voltage should be constant and independent of the V_{in}. Two path bootstrap circuits are presented in [17]. M_2 and C_2 constitute the main path, and M_1&C_1 form the auxiliary path. Bulk terminals of M1, M_2 &M_4 devices are connected to the node V_x to avoid forward biasing. With this technique, non-linear capacitance would drive through the auxiliary path, and Non-linear capacitance won't directly arrive on the main path because the sampling switch gate will be spreading the input signal. Here, the input signal travels along the main path while the non-linear capacitance drives travel through the auxiliary path [18].

4. PROPOSED CONTROL LOGIC CIRCUIT

In ADC, the noise-contributing elements are the sample switch, comparator, and DAC. Hence, the noise of complete ADC should have a standard deviation of 0.64LSB. The nonlinearities are due to the injected charge into the DAC when the sampling switch is ON. Therefore, it shows the impact on the ADC's SFDR. We can keep the nonlinearities produced by DAC and sample switch small enough by setting the SFDR value is > 70dB. The speed of ADC is influenced by the ON resistance of the switch. The proposed bootstrap switch for achieving the fore mentioned targets is shown in *figure 5*. For the ADC operation, the characteristics of M_1 are most important. It decides the switch-ON resistance. In the existing circuit [18]. During the sampling period, M_3 will connect the CB bottom plate to the input Vin. The gate of M_1 is connected-ed to the top plate of CB by the M_2 device and creates an unwanted offset with input. In the existing circuits, the stress on M_2 and M_4 occurs in track mode, with drain-source or gate-source voltage>1V; this reduces the device's progress in performance. when M_1 is off, maxi- mum voltage at M_4 drain source is $V_{in}+V_{DD}$ > 4V. Similarly, the V_{GS} of M_2 also has the same voltage; hence it's stressed. M8 device is used to protect the gate oxide of M_4. By connecting a cascade device M_8 in series M_4, its drain peak voltage can be < V_{DD}. In hold mode, devices M_4 and M_8 reduced the gate potential of M_1 to zero. Stress on M_2 can be decreased by allowing the gate voltage to fluctuate in harmony with Vin and VX. Additionally, this gate needs to be connected to V_{DD} and Vin in track mode. In the hold mode, this is done by Ma and M_b, respectively. M_5 and M_6 will serve to pre-charge the CB capacitor. M_b device was used to close the gate of M_2 during the hold phase. Similarly, M_a and M_c are used to opening the gate of M_2. During sampling startup, M_a helps. M_c, with Vin as the gate voltage bootstrapped, provides a small resistance connected in series with the gate of M_2. Although appearing redundant, M_a is still required for the circuit to start up properly.

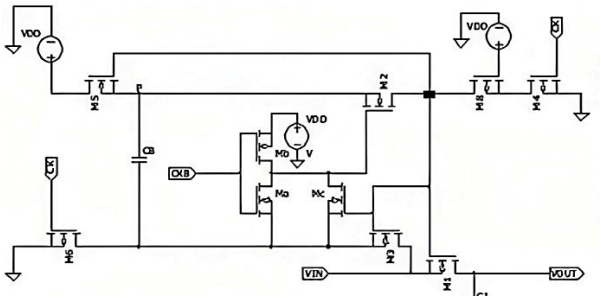

Figure 5. The modified proposed model of the control circuit

Design: The input voltage, Vin=A$cos\ \omega_{in}t$, and the worst-case supply voltage= A=0.5V@ 5%= 0.95V, the range =0.25-0.75V.

Then the size of LSB $= \frac{2A}{2N} = \frac{1V}{1024} = 1mV$. Bootstrapped sampler accommodates larger swings, although the period before it usually, a buffer might not. ADC for N bits sensing a signal of A cos ωint, the ideal SNR value is =(A2/2)/(δ2/12). Where δ=LSB=1mV, SNR in dB=(6.02N+1.76) dB=62dB for N=10.

The harmonic distortion (HD) must remain <–62 dB. Targeted HD to achieve is about -65 dB at its worst, *i.e.*, A = 0.5V and fin=ωin/2π=5MHz (@ Nyquist rate). The noise introduced by the sampler, *i.e.*, the kT/C noise associated with M_1, and C_1, must barely affect the overall SNR. The SNR of the sampler-ADC is a cascade and is given by the equation.

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$$\text{SNR} = \frac{A^2/2}{\frac{\delta^2}{12} + \frac{KT'}{C_1}} \quad (2)$$

The target of 1 dB penalty imposed by the kT/C noise term, split the above equation with the ideal SNR equation, take 10log of the result, and equate to –1 dB, and with δ=1mV and T=750C= 348K,

$$-1\text{dB} = 10\log_{10}\left(\frac{1}{1 + \frac{75}{384c_1} * \frac{12}{10^{-6}}}\right) \quad (3)$$

Then C_1 =222.5fF, which we increase by 0.2 pF. The input signal in the track mode must only be slightly attenuated by the low-pass filter created by M_1 and C_1. The output amplitude is equal to

Where Ron1 is the M_1 ON-resistance, the aim is to have attenuation< 0.5 dB @ the Nyquist rate.

$$10\log_{10}\left(\frac{0.5}{\sqrt{1 + (2\pi * 5 * 10^6 * R_{on1} * 0.2 * 10^{-12})^2}}\right) \quad (4)$$

Ron1=111.5n, with this M_1 aspect ratio, is calculated by maintaining the Ron1 measured.

$$R_{on1} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{DD} - V_{in} - V_{TH})} \quad (5)$$

For the SCL process $\mu_n C_{ox} = 56.8\mu V_{DD} = 3.3V$, V_{TH}=0.35V, L=0.18µm, and Obtain W1=900µm.

All the MOS switches W/L ratios are calculated based on the voltages of the terminals and the parameters used above and are listed in *table 1*.

Table 1: Modified control logic circuit articulated component values

Parameter	Value	Type
W_1	900µm	NMOS
C_1	0.2pF	Capacitor
W_2	125 µm	NMOS
W_4	450 µm	PMOS
W_3	225 µm	NMOS
W_6	125 µm	NMOS
W_5	225 µm	PMOS
CB	0.1pF	Capacitor
W_8	450 µm	NMOS
W_a	12 µm	NMOS
W_b	45 µm	PMOS
W_c	225 µm	NMOS
W_1	900µm	NMOS

The intransigence of the proposed switch is shown in the *figure 6*, it's observed that the on-resistance of the proposed circuit is more stable.

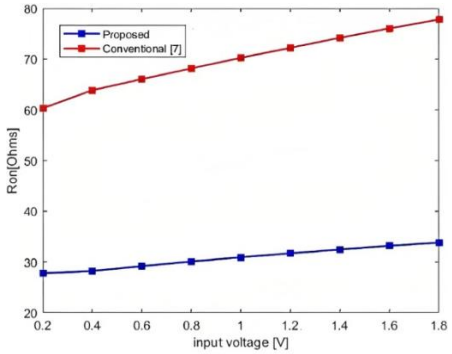

Figure 6: On resistance of Proposed circuit graph

5. RESULTS AND DISCUSSION

The proposed circuit is put into practice in the cadence is presented in *figure 7*. Then its symbol created as in *figure 8*.

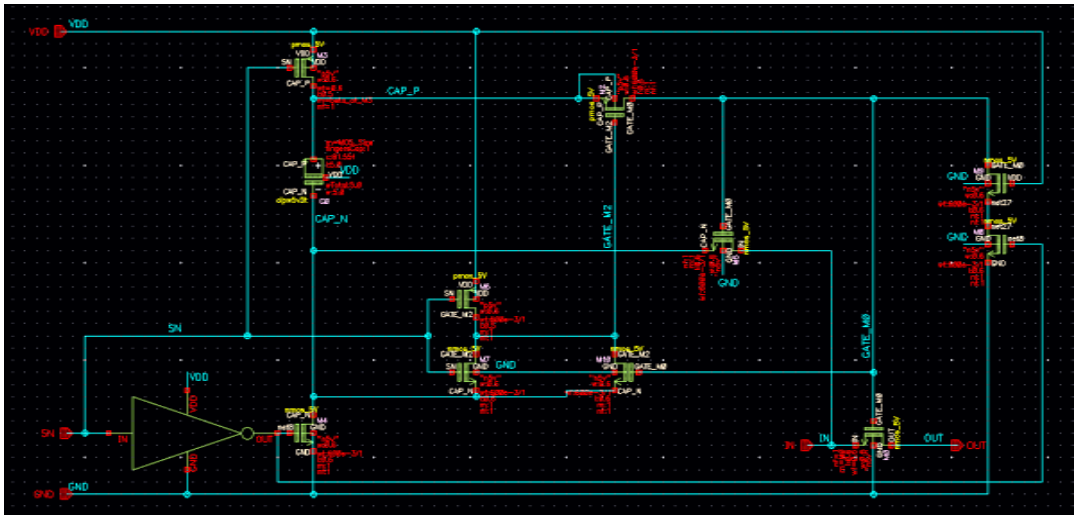

Figure 7: Schematic of S&H in cadence

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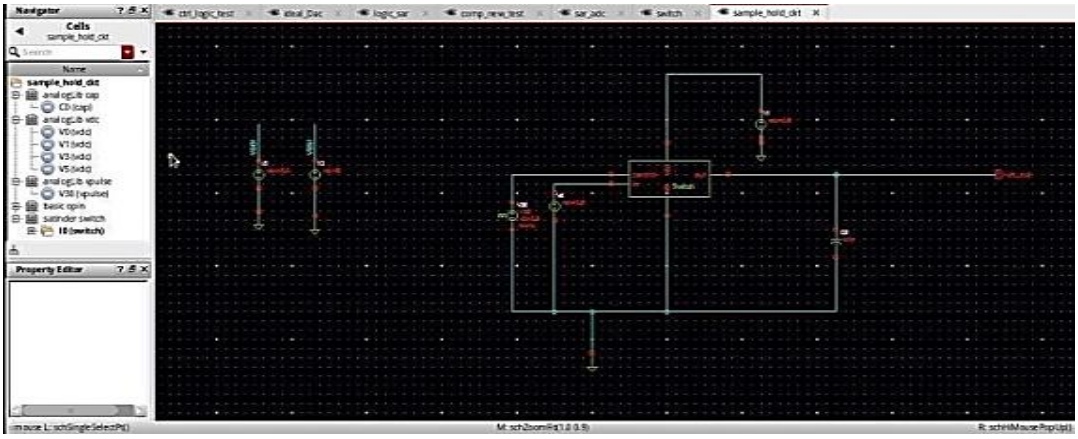

Figure 8: Symbol Creation of S&H in cadence

the output of the block, which consists of an input signal output signal, and a control input signal as well. Here shout is an output signal in the output waveform and a ctrl signal is applied, and an input signal has seen the *figure9*.

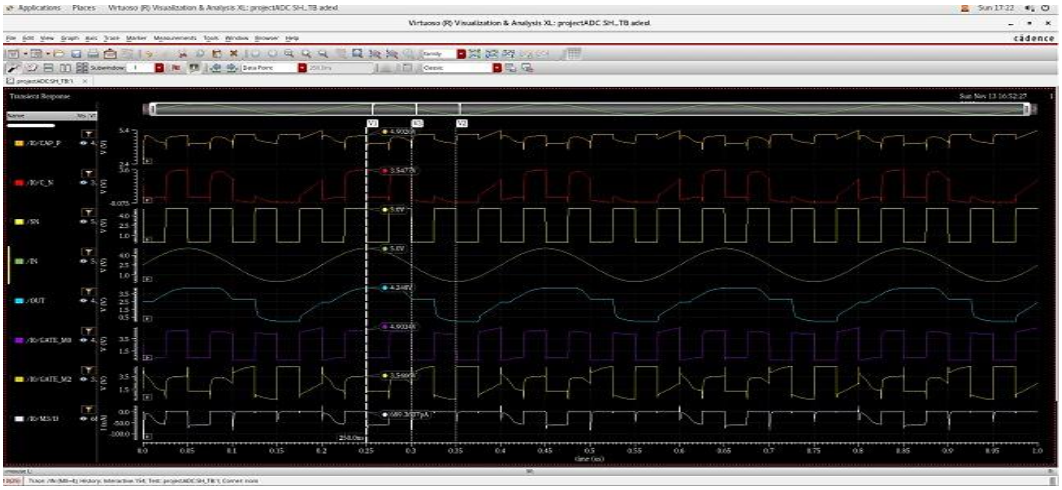

Figure 9: Signals and Transient Response of S&H in cadence

Bootstrap switch & Op-Amp were designed using 0.18µm SCL CMOS Technology. And the output waveform is shown in *figure 10*. S&H testing is per- formed with 3.3V supply voltage, two differential 10MHz sinusoid signals as inputs, and two 200fF capacitors as load.

The output is sent to compare it with the reference signal of the DAC block. In the design process of the sample and hold main concentration is to consider the switching mechanism and the ON resistance of the switch. The problems which arise in the design of the sample and hold block are that charge sharing; clock feeds through. A sample and hold block is designed with the targeted SCL 180 nanometer CMOS technology and simulated and tested.

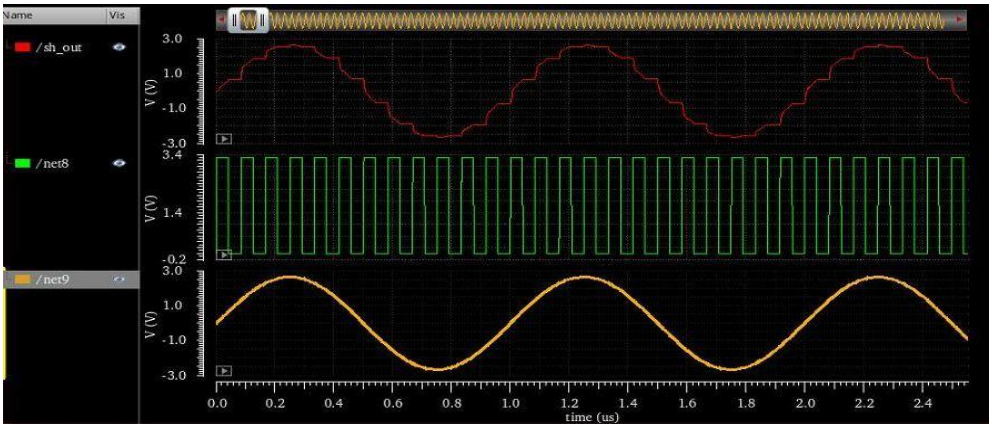

Figure 10: Sample and Hold output

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The results are tabulated and compared with previous literature in the table, where the power consumption is far better than other circuits, and the designed S/H circuit is for higher resolution ADC of 10-bit. In the comparison table, we have tabulated and compared the parameters of the design, such as the technology, supply voltage at which the design is operating and the power consumption in Mill watts and the number of samples per second as well as the resolution and signal to noise ratio and effective bit count for existing works and the current modified proposed work we have obtained 0.425mW of power consumption and ENOB as 9.7 and SNR as 72 dB at the rate of 10 MSPS. Operating at 3.3V and 180 Nanometer SCL CMOS Technology.

Table 2: Comparison of proposed Modified control logic circuit with existing work

	Process (µm)	Supply (V)	Power (mW)	SPS/ fin (M)	Resolution	ENOB	SNR
Target	0.18	3.3	< 10	10/5	10	10	>62dB
[8]	0.35	3.3	13.6	50/2.5	10	7.8	62/67@5M
[9]	0.18	1.8	28	100	14	9.2	94@48.9M
[10]	0.18	3.3	15.4	50	14	8.8	94.6@5M
[11]	0.18	3.3	7.6	100	10	8.7	85.4@10M
[12]	0.35	3.3	15.4	50	10	8.1	67@25M
Proposed	0.18	3.3	0.425	10/5	10	9.7	72@10M

6. CONCLUSION

Overall, the described S&H circuit design, as part of the SAR-ADC system, shows excellent performance in terms of high-resolution digitization, low power consumption, and superior signal-to-noise and distortion characteristics. sample-and-hold (S&H) circuit design specifically tailored for a 10-bit Successive Approximation Register Analog-to-Digital Converter, operating with a power supply of 3.3V. Designs have been carried out with SCL 0.18µm CMOS process. The sampling rate at which it operates is 10Msps. A novel bootstrap switch has been employed; the power consumption is 0.425mW, which is 4.5% of total ADC power. S&H simulation results show that the SNDR is 88 dB, and the SFDR is 73 dB at a 10 MHz input signal frequency with a 10 MHz sampling rate. The results are tabulated and compared with previous literature in the table, where the power consumption is far better than other circuits These features make it a compelling choice for applications that demand high-precision analog-to-digital conversion.

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