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International Journal of
Electrical and Electronics Research (IJEER)
Research Article | Volume 11, Issue 3 | Pages 696-704 | e-ISSN: 2347-470X

A Solution to VLSI: Digital Circuits Design in Quantum Dot Cellular Automata Technology

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ABSTRACT- Quantum Dot Cellular Automata is a Nano device efficient than other devices in nanotechnology for the last two decades. It is beneficial over Complementary Metal Oxide Semiconductor technology like high speed, low energy dissipation, high device density and high computation efficiency. To achieve further optimization different methods like simplifications in Boolean expressions, tile method, clocking scheme, cell placement, cell arrangement, novel input techniques, etc., are in use. These methods improve the performance metrics in terms of QCA Cells, total circuit area, delay in output, power consumption, and coplanar or multilayer layout. This paper is about the novel NOT gate layout designed with efficient parameters compared to existing NOT gates except area parameters with analysis and XOR gate and multiplexer circuits. The novel gate provides an improvement of 55% in the number of cells, polarization raised by 0.33, and an 80.77% improvement in total area. These circuits illustrate further scope in QCA circuit design efficiently. XOR circuit shows area reduction up to 0.006 μm2 with 0.5 clock cycle delay. Further optimization in XOR parameters and with this novel NOT gate researchers can optimize parameters to bring revolution and digitalization.

General Terms: Nanotechnology, Quantum Dot Cellular Automata, Digital Circuits, CMOS, VLSI, Electronics
Keywords: QCA (Quantum Dot Cellular Automata); ITRS (International Technology Roadmap for Semiconductors); MG (Majority Gate); SDN (Signal Distribution Network); Inverter.

ARTICLE INFORMATION
Author(s): Madhavi Repe and Dr. Sanjay Koli;
Received: 08/02/2023; **Accepted**: 13/07/2023; **Published**: 10/08/2023;
e-ISSN: 2347-470X;
Paper Id: IJEER230202;
Citation: 10.37391/IJEER.110309
Webpage-link:
https://ijeer.forexjournal.co.in/archive/volume-11/ijeer-110309.html

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1. INTRODUCTION

Quantum Dot Cellular Automata (QCA), Resonant Tunneling Devices (RTD), Single Electron Transistors (SET), Tunneling Phase Logic (TPL), Carbon Nano Tube Transistors (CNT) are Nanodevices given by International Technology Roadmap for Semiconductors (ITRS). The best nanotechnology device among all these Nanodevices is QCA. It overcomes the drawbacks of CMOS technology [2]. QCA is transistor-less and efficient technology. It has high device density and low power consumption. It operates at Terahertz (THz) range. In QCA information is transferred by columbic repulsion and in CMOS technology current switching takes place.

The workflow shows the basics of QCA in *section II*. Different design layouts of XOR gates are given in *section III* and multiplexers are investigated and compared in *section IV*. *Section V* gives simulation software used in designing QCA circuits is described. It is used to compute the various parameters in the design. *Section VI* illustrates the experimentation for the implementation of a novel gate to achieve efficient circuit design in the field of nanotechnology. One such novel NOT gate with the best parameters achieved is elaborated. Section VII states the scope to design digital circuits towards digitalization in the field of QCA and the concluding remark which gives ideas for new researchers in the future for miniaturizing processors in an embedded system.

2. BASICS OF QCA

2.1 QCA Cells

QCA is formed by the term's quantum dot and cellular automata. Quantum dots are nanometer-scaled devices containing tiny droplets of free electrons. These dots are in the range of 2nm-10nm and are constructed from Aluminum using electron beam lithography techniques. Cellular automata consist of grid of cells. Four quantum dots are present at the four corners of the cell. Cells have a finite number of states at a discrete time. Cell state can be found by using its previous state and its immediate adjacent cells. When the cells are charged with two additional electrons, due to columbic repulsion between electrons they take either of the two opposite positions of the quantum dots. The placement of the electrons gives two possible states of cells that are termed cell polarizations or states of cells. These two possibilities are represented with two binary

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numbers i.e., 0 and 1. Thus the cell encodes the data as binary '0' and binary '1'. The cell structure is shown in *figure 1* and *figure 2* shows the states of a cell.

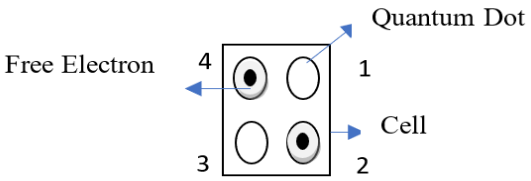

Figure 1: Cell Structure

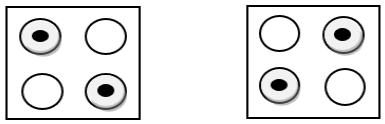

Figure 2: States of a Cell

To find the polarization of a cell [2] use equation 1 as shown below. Refer to *figure 1* for the numbering of dots [3] to find the states of cells.

$$P = \frac{(P1 + P3) - (P2 + P4)}{P1 + P2 + P3 + P4} \quad (1)$$

2.2 Basic Components of QCA

Gate (MG), and inverter are the main components. Cells can be rotated or normal cells. Normal cells are nothing but (90^0 QCA wire) and rotated cells are (45^0 QCA wire). QCA wire is formed by an array of cells and is depicted in *figures 3(a) and 3(b)*.

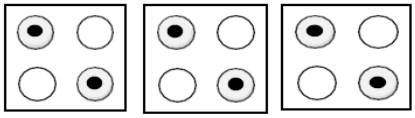

Figure 3(a): 90^0 QCA Wire

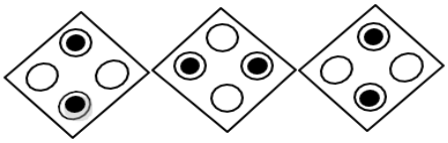

Figure 3(b): 45^0 QCA Wire

In QCA, the inverter gate with two or four cells or nine cells with a fork shape is used to get an inversion of the input signal. It can be constructed as shown in *figure 4(a) and figure 4(b)*.

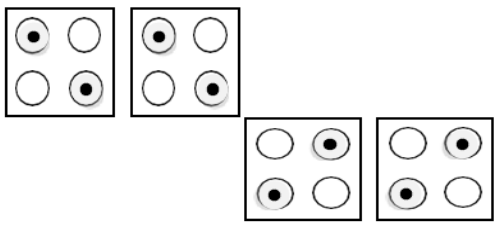

Figure 4(a): Simple QCA Inverter

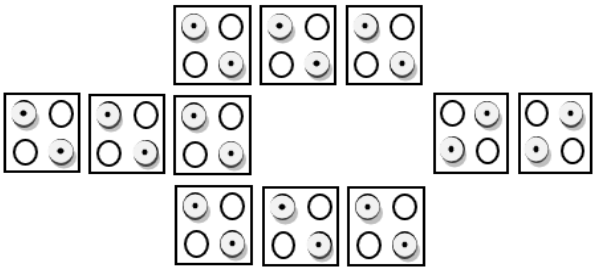

Figure 4(b): Fork shaped QCA Inverter

One of the main components in QCA is a MG gate. As per the name, majority gate, it always gives the output for the majority of the input combinations. It has five cells in which three of them are input cells, one is device cell and one cell is the output cell (F). Device cell is placed at the center of the gate and it decides the output based on the inputs. MG gate is as shown in 5. Figure shows if a,b,c as the inputs then the logical function of a MG gate is M(a,b,c) = ab+bc+ac. Using MG, AND gate and OR gate can be implemented by giving one of the inputs of MG as either polarized to -1 or +1. If the input C is polarized with +1, MG gate can be used as OR gate and used as AND gate if input C is polarized with -1.

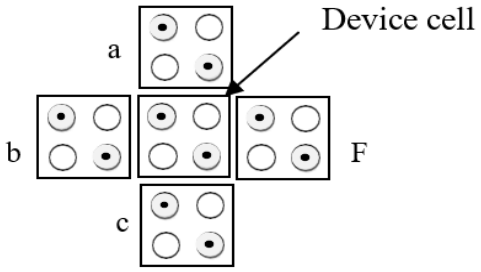

Figure 5: Majority Gate (MG)

2.3 Crossovers in QCA

Different wire crossovers in QCA are coplanar crossover, Signal Distribution Network and Multilayer crossover. Each crossover has its own advantages and disadvantages. Coplanar crossover uses both 90^0 and 45^0 QCA wires which results in the possibility of cross-coupling [6]. Also, the coplanar crossover has very less excitation energy which leads to stray charges and temperature effects [7]. These problems can be resolved with SDN (Signal Distribution network) which relies on nearest-neighbor interactions which help in the rise of excitation energy, improvement in thermal effects. Multilayer crossover increases the complexity and cost of fabrication but can give the best device package density.

2.4 QCA Clocking

QCA clocking is different from the CMOS clock. CMOS uses a clock to control the timing. In QCA, the clock is used to direct the flow of data [6] *i.e.*, switching and providing power gain to the circuits. In QCA, a clock is required for sequential circuits as well as combinational circuits. The electric field is used to generate Clock signals. Basically, the clock can be a continuous clocking or a zone clock. Continuous clocking creates

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Research Article | Volume 11, Issue 3 | Pages 696-704 | e-ISSN: 2347-470X

metastability problems and so adiabatic clocking is used. Researchers have used different clocking schemes like, 1D, 2D, and 2D wave clocking schemes [6] to design and improve the speed parameter of the different digital circuits.

Zone clocking with four phases is used in a QCA Designer tool. Switch, Hold, Release and Relax are the four phases as shown in *figure 6(a)* [6]. *Figure 6(b)* [5] indicates the representation of clock zone signals. The switch phase determines the state of the cell according to adjacent cells [6] and is an important phase. Each clocking zone has a phase shift of 90^0.

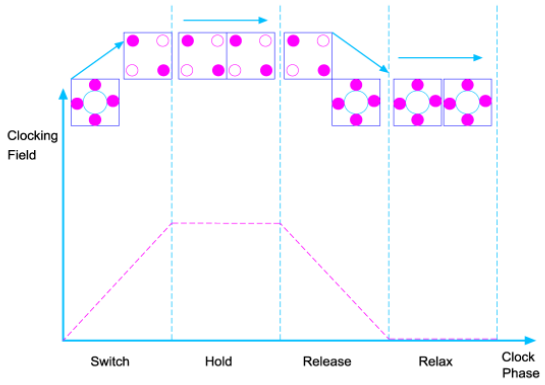

Figure 6(a): QCA Clock with phases

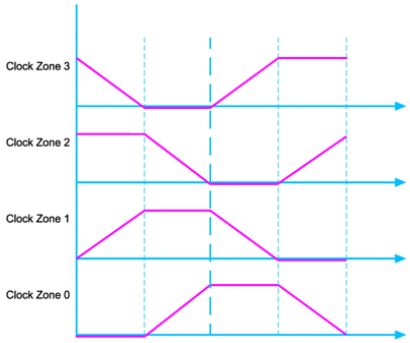

Figure 6(b): QCA Clock Zones

3. METHODOLOGY USED FOR XOR CIRCUITS

Designing digital circuits in QCA is of much attention in recent eras to achieve better performance metrics. Researchers have designed and proposed many XOR gate implementations. *Table 1* gives the different designs implemented along with the parameters in consideration.

Table 1 shows performance parameters such as the number of cells, total area in µm2, and delay. Designs are considered with different methodologies used.

Moustafa A et al [4] have prepared a basic building block of 27 cells using MG and NOT gate. Out of 27 cells, they used 11 cells as configuration cells. These cells can be customized as per the design need. M. R. Beigh et al presented the layouts with fewer crossovers and less cell count compared to previous designs [9]. S. Santra and U. Roy [10], proposed the XOR gate implementation with Boolean expression and by using basic gates which reduces cell count compared to previous designs. Authors in the paper [11] presented the XOR gate layout with proper arrangement of cells and clock delay. From these, we can say that, it's the modification in the Boolean expression of the XOR gate, the basic gates used to implement the XOR gate, the clocking scheme used and the number of crossovers used, etc. to design an XOR gate. If the number of cells required to implement a gate is less it automatically reduces the space requirement and improves the device density. The delay column indicates the number of clock phases the gate takes to give the output from the input. A value of 0.5 indicates that the output is delayed just by 1 clock phase and a value of 1 indicates that the output is delayed by 4 clock phases or 1 complete clock cycle. The star mark indicates that this XOR gate implementation has less space requirement due to just 8 cells 0.006µm2 area and 0.5 delay giving maximum speed compared to all other implementations. Section IV elaborates on the software used for these circuit implementations and the performance parameters to be set during the layout and simulation.

Table 1: XOR design comparison

References	No. of cells	Cell Area (µm^2)	Delay
[4]	28		0
[9]	34	0.06	1
[10]	30		4
[11]	30		0.5
[12]	87	0.08	1
[13]	36	0.03	0.75
[14]	13	0.02	0.5
[15]	13	0.012	0.5
[16]	18	0.01	0.75
[17]	14	0.01	0.5
[18]	29	0.02	0.75
[19]	29	0.02	0.75
[22]*	8*	0.006*	0.5*

Comparative results are given in *table 1*. *Figure 7* shows the representation of variation in the number of cells. *Figure 8* shows the area utilized in the design of XOR gates whereas *figure 9* indicates the delay encountered in getting the output.

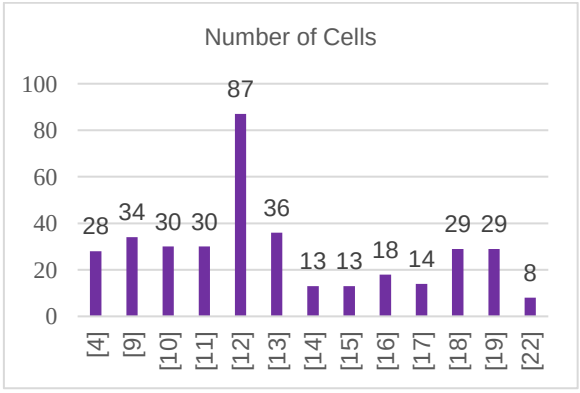

Figure 7: Number of Cells

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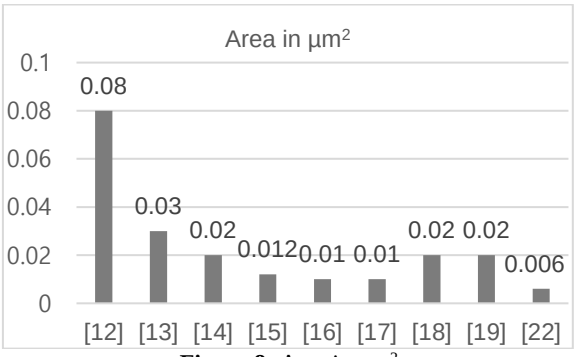

Figure 8: Area in µm²

XOR gate implementation in *QCADesigner* is illustrated with results for two of the layouts in the following section. First, the layout is to be drawn in *QCADesigner* and then it is to be saved with extension .qca . In order to get the layout in the form of image format save the file with an extension .eps [23]. The simulation results once observed can also be saved with the same .eps extension to get it in image format. To view .eps image make use of Corel Draw software or Adobe Illustrator.
For comparative analysis refer to *figure 10* and *figure 11* for the design mentioned in [13], *figure 12* and *figure 13* for the design mentioned in [22]. The layout of the XOR gate and its simulation from these two references is considered.

Observations from the layout show that the number of cells in *figure 13* is very less, which is 8 whereas in *figure 10*, the number of cells is 36 and so the area requirement also, is observable. The simulation result indicates the difference in delay in achieving the output. Delay is more in the simulation indicated in *figure 11* compared with the simulation in *figure 13*.

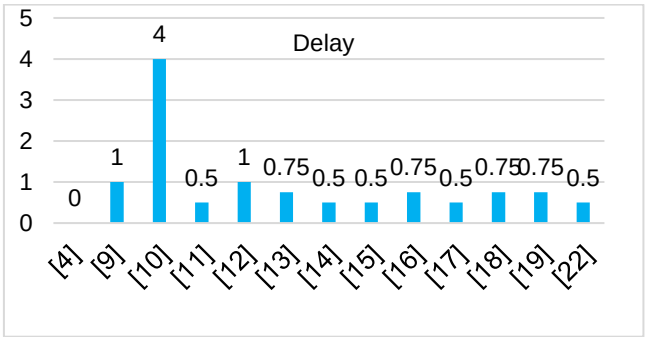

Figure 9: Delay in terms of clock phases

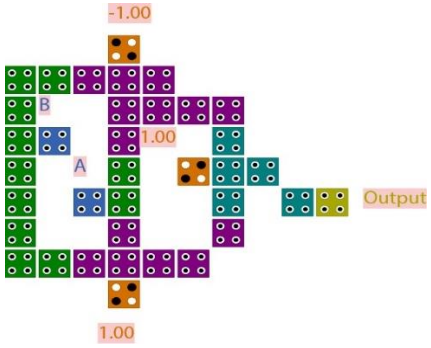

Figure 10: XOR Gate Implementation [13]

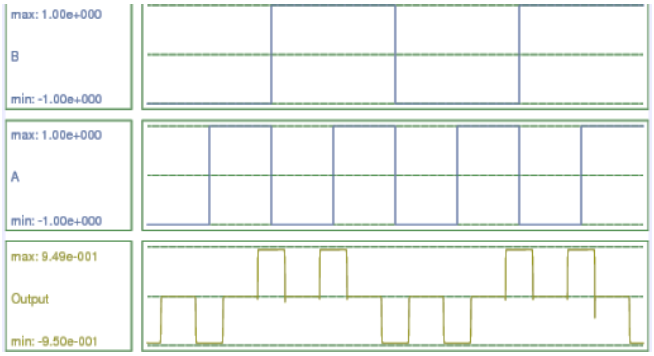

Figure 11: Simulation Result of XOR Gate [13]

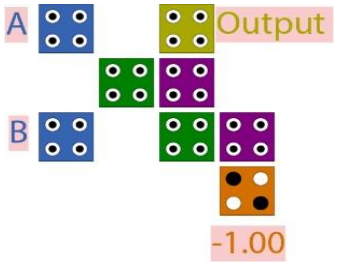

Figure 12: XOR Gate Implementation [22]

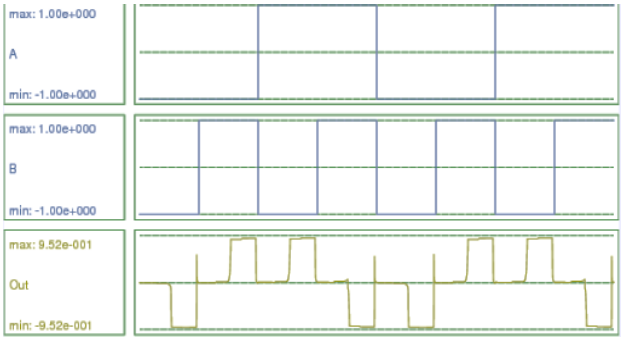

Figure 13: Simulation Result of XOR Gate [22]

4. METHODOLOGY USED FOR MULTIPLEXER CIRCUITS

Multiplexer or Mux has many applications in digital circuits and hence in any embedded system circuits. Also, in the near future, it will be used in digital Nano communications for signal encoding [24]. Researchers have implemented different types of mux circuits in QCA technology with different methodologies. Observations drawn from the earlier implementations for 2:1 Mux and 4:1 Mux are depicted in the following *table 2*. This table gives the minimum requirement and latest designs for multiplexers.

Table 2: Latest multiplexer design parameters

Type of Mux	MGs Required	Clock Zone	Minimum no of QCA Cells used	Minimum Total Area Used (µm²)
2:1 Mux	3	3	21	15552
4:1 mux	9	4	118	87388

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Research Article | Volume 11, Issue 3 | Pages 696-704 | e-ISSN: 2347-470X

Table 2 shows that a 2:1 multiplexer circuit is designed with 3 MGs and a 4:1 Multiplexer circuit is designed using 9 MGs. The number of clocking zones required for 2:1 mux is 3 and for 4:1 it is 4. This table also shows the minimum number of QCA cells and the area used by cells in layout implementation. This clears the idea of further need in optimization to achieve miniaturization in the mux circuit and ultimately towards the application building using Mux. This further optimization requires different methodologies to be designed by researchers and will lead to optimized revolution in the field of Nanotechnology.

Table 3 lists the earlier designs with various parameter considerations for 2:1 mux and 4:1 mux. The latest design for mux saves 63.15% number of QCA cell and 66% of area as compared to previous design approaches.

Table 3: **Multiplexer design Comparison**

Design	MGs Used	Nos of QCA Cells	Cell Area (μm^2)	Total Area (μm^2)	Clock Zone Used
2:1 Mux					
Latest	3	21	6804	24164	3
Existing 1	3	23	7452	18144	3
Existing 2	3	25	10000	21600	3
Existing 3	3	26	8424	15552	2
Existing 4	3	27	8748	23328	3
4:1 Mux					
Latest	9	118	38232	202104	4
Existing 1	9	130	41874	101952	4
Existing 2	9	141	56191	121372	4
Existing 3	9	146	47335	87388	4
Existing 4	9	152	49156	131082	4

In the design of the multiplexer circuit, the authors have arranged cells as per the Boolean expression reduction technique with a common way of clock. The design of 2:1 mux in [25] has used a layout generator tool which is more complex and requires more area. S. Hashemi, M. R et al have presented the design of a 2:1 mux using a single and multilayer structure [26]. Cells need to be arranged in a way that leads to reduction in complexity, cell area and ultimately total area of the circuit layout.

Figure 14 shows the layout of the 2:1 mux and its simulation result in *figure 15*.

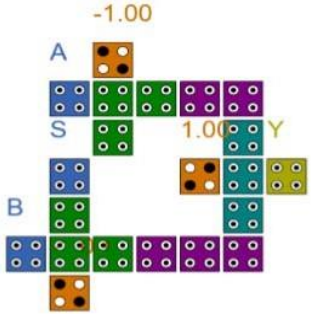

Figure 14: QCA Layout of 2:1 Mux [24]

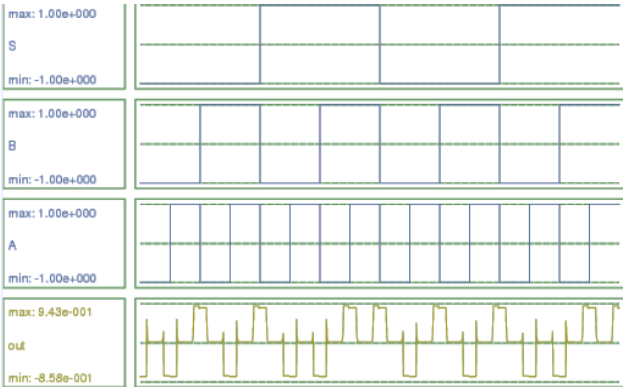

Figure 15: Simulation Result of 2:1 Mux [24]

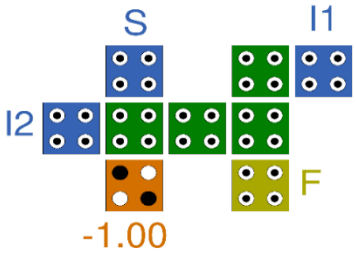

Figure 16: QCA Layout of 2:1 Mux [33]

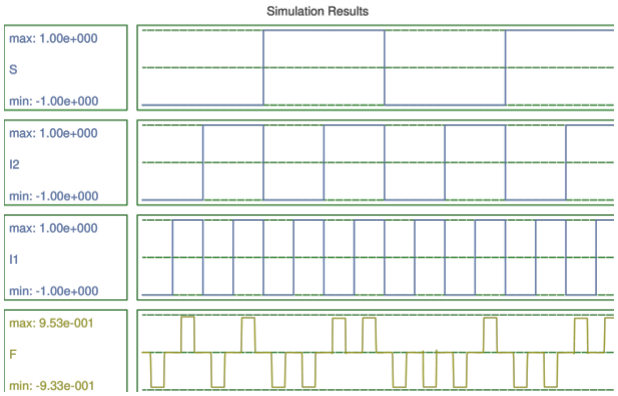

Figure 17: Simulation Result of 2:1 Mux [33]

This is an efficient 2:1 multiplexer. It gives the best results in comparison to previously completed work. It uses only nice cells. This is implemented using a cell interaction method and a single majority voter gate to achieve efficient performance parameters. It makes use of only 9 cells. The polarization achieved is +0.953 and -0.933.

5. SIMULATION SOFTWARE

Circuit implementation is done using *QCADesigner V2.0.3* and *QCADesigner-E*. The extension of the *QCADesigner (version 2.0.3)* is *QCADesigner-E* [20]. It has been developed at the University of Bremen. This tool [21], estimates the power dissipation of QCA circuits. It uses the Coherence Vector Simulation Engine (CVSE). Further, it is fully compatible with QCA designs generated with the *QCADesigner* version 2.0.3. Standard parameters used in the *QCADesigner* tool are listed in *table 4* [20].

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Table 4: Parameters used in the *QCADesigner* tool

Parameter	Description	Standard Value
QD size	Quantum-Dot size	5nm
Cell Area	Each cell dimensions	18nmx18nm
Cell Distance	Distance between two cells	20nm
Layer Distance	QCA Layers separation in case of multilayer crossing	11.5nm
r	Relaxation Time	1E-15s
γ H	Maximum Saturation energy of clock signal	9.8E-22J
γ L	Minimum Saturation energy of clock signal	3.8E-23J
Є r	Relative permittivity of material for QCA	12.9*
Temp	Operating Temperature	1 K
Reffect	Distance between cells considered	80nm[†]

*Relative permittivity of GaAs and AlGaAs
[†]Interaction effects between two cells decays inversely with the fifth power of its distance.

Table 5 lists the additional parameters used in *QCADesigner-E* tool [20]

Table 5: Parameters used in *QCADesigner-E* tool

Inverter Model	Cell Count	Total Area in nm2	Polarization achieved
Tougaw et al Inverter Model [30]	8	5684	0.775
Farazkish et al Inverter Model[31]	6	3724	0.486
FNZ Inverter Model [31]	8	6084.00	0.931
Navi et al Inverter two-layer design Model [32]	6	1764	0588
Navi et al Inverter Three layer design Model [32]	8	1764	0.842
AOI (And-Or-Inverter) Inverter Model [33]	7	12744	+0.525 and -0.629
Standard NOT gate with two cells	2	2318	0.562
Standard NOT gate with fork shape	9	7198	0.951
Novel NOT Gate Proposed	5	5814	0.984

Analysis of power consumption in various designs is achieved using the QCA Pro tool. Here, energy dissipation levels by the cell can be observed. Power dissipation analysis for various kink energy values is calculated in QCA Pro. Various parameters like maximum, minimum, and average energy dissipation of the circuit, average leakage energy dissipation, and average switching energy dissipation of the circuit are obtained [27].

6. EXPERIMENTATION

This section gives the novel NOT gate design which can be used in building different circuits efficiently in the field of nanotechnology using QCA. *Figure 18a* shows a NOT gate with only 5 cells with a total area equal to 5814 nm^2 using normal cells. This gate provides an output polarization of 9.84 as depicted in *figure 18b*. This is one of the best gates in comparison with standard NOT gates in terms of best polarization and the number of cell count and hence total size. Standard NOT gate with fork shape has 9 cells, polarization of 9.51 with an area of 7198 nm^2. Thus, this novel gate provides an improvement of 55% in the number of cells, polarization raised by 0.33, and an 80.77% improvement in total area with respect to the fork shaped NOT gate.

Figure 18 (a): Novel NOT Gate Layout

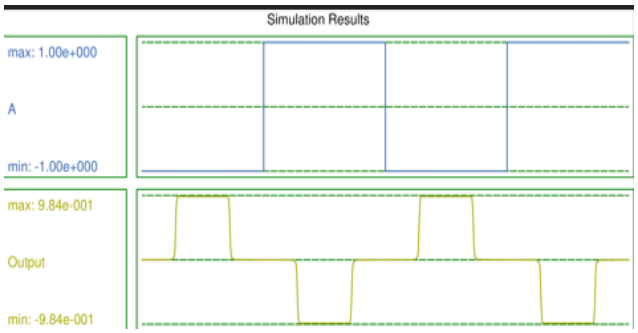

Figure 18 (b): Simulation Result of Novel NOT gate

Table 6 below gives a comparison of NOT gates implemented to date.

Table 6: Comparison of Inverters

Parameter	Description	Standard Value
T	Clock signal period	10E-12s
slope	Rise and fall time of the clock signal slopes	1E-12s
shape	Shape of clock signal slopes [RAMP/GAUSSIAN]	GAUSSIAN
Tin	Input signals period	10E-12s
Tsim	Total simulation time	80E-12s
Tstep	Time interval of each iteration step	1E-17s

An inverter with two cells is area efficient but is not robust and the polarization achieved is also very poor. *Table 6* concludes that the standard NOT gate with fork shape is robust but it requires 9 cells with an area of 7198nm^2 and a polarization of 0.951. The proposed inverter is the best in comparison with the rest of the inverters. It gives the best results in the number of cell counts, total area and polarization. This inverter is possible with proper cell arrangement methodology.

6.1 Analysis

The analysis shows that the output is an inversion of the input. This inversion is due to the arrangement of cells to achieve more

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Research Article | Volume 11, Issue 3 | Pages 696-704 | e-ISSN: 2347-470X

stability and their potential energy at the minimum level. Cell size is assumed as 18x18 nm and the separation between the neighbor cells is 2nm. As shown in *figures 19 (a) and 19 (b)*, the square represents the QCA cell and the position of electrons inside that cell is represented by the filled circles.

To calculate the potential energy between two electron charges equation 2 is used. In this equation, U is the potential energy, k is the Boltz constant (9×10^9), q1 and q2 are charges of electrons (1.602×10^{-19}) and r represents the distance between two electric charges [28-29].

$$U = k\,\frac{q1.q2}{r} \qquad (2)$$

By using the values of q1, q2 and k in equation 2, the potential energy in simplified form is represented in equation 3.

$$U = \frac{23.04 \text{ x } 10\ \hat{}(-29)}{r} \qquad (3)$$

Potential energy between two cells is computed by rounding up over the entire dots in each cell and is given by equation 4.

$$UT = \sum_{i=1}^{n} Ui \qquad (4)$$

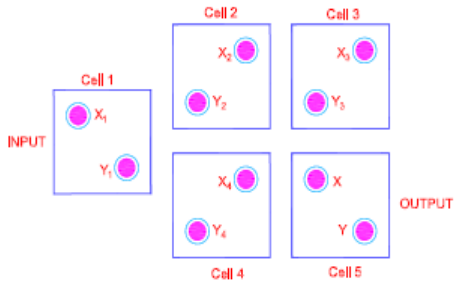

Figure 19(a): NOT gate for logic '0' in cell 5

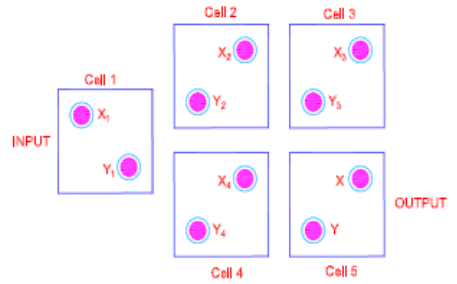

Figure 19(b): NOT gate for logic '1' in cell 5

If logic '0' is applied at the input side to cell 1, then cell 2, cell 3 and cell 4 will follow the opposite logic of input due to cross-section to cell 1. Let us find the position of electrons in the output cell. The potential energy at cell 5 is calculated with the state (a) and state (b) as shown in *Figure 19(a)* and *19b* respectively. The one which gives minimum potential energy is the most stable state.

As indicated in *Figure 19 (a)* the potential energy of electron 'X' of cell 5 with respect to X1, X2, X3, X4 and Y1, Y2, Y3, Y4 of cells 1, 2, 3 and 4 is calculated. Similarly, the potential energy of electron 'Y' of cell 5 with respect to X1, X2, X3, X4 and Y1, Y2, Y3, Y4 of cells 1, 2, 3 and 4 is calculated. The total potential energy of electron 'X' with respect to all other cells is added using equation 4 to get $U_{T^{11}}$ and the potential energy of electron 'Y' with respect to all other cells is added using equation 4 to get $U_{T^{12}}$. Total energy UT_1 for 19(a) representation is the addition of $U_{T^{11}}$ and $U_{T^{12}}$. This is indicated in Assumption 1. In a similar way, assumption 2 shows total energy UT_1 for 19(b).

Assumption 1: If cell-5 is logic '0' as shown in Figure 19(a)

Figure 19(a) (Electron x)

$$U_1 = \frac{A}{r_1} = \frac{23.04\,X\,10^{-29}}{41\,X\,10^{-9}} = 0.561\,X10^{-20}J$$
$$U_2 = \frac{A}{r_2} = \frac{23.04\,X\,10^{-29}}{31\,X\,10^{-9}} = 0.743\,X10^{-20}J$$
$$U_3 = \frac{A}{r_3} = \frac{23.04\,X\,10^{-29}}{22.825\,X\,10^{-9}} = 1.009\,X10^{-20}J$$
$$U_4 = \frac{A}{r_4} = \frac{23.04\,X\,10^{-29}}{22.825\,X\,10^{-9}} = 1.009\,X10^{-20}J$$
$$U_5 = \frac{A}{r_5} = \frac{23.04\,X\,10^{-29}}{21.931\,X\,10^{-9}} = 1.050\,X10^{-20}J$$
$$U_6 = \frac{A}{r_6} = \frac{23.04\,X\,10^{-29}}{11X\,10^{-9}} = 2.094\,X10^{-20}J$$
$$U_7 = \frac{A}{r_7} = \frac{23.04\,X\,10^{-29}}{11\,X\,10^{-9}} = 2.094\,X10^{-20}J$$
$$U_8 = \frac{A}{r_8} = \frac{23.04\,X\,10^{-29}}{21.931\,X\,10^{-9}} = 1.050\,X10^{-20}J$$

$$U_{T^{11}} = \sum_{i=1}^{8} U_i = 9.61X10^{-20}J$$

Figure 19(a) (Electron y)

$$U_1 = \frac{A}{r_1} = \frac{23.04\,X\,10^{-29}}{52.201\,X\,10^{-9}} = 0.441\,X10^{-20}J$$
$$U_2 = \frac{A}{r_2} = \frac{23.04\,X\,10^{-29}}{41\,X\,10^{-9}} = 0.561\,X10^{-20}J$$
$$U_3 = \frac{A}{r_3} = \frac{23.04\,X\,10^{-29}}{35.227\,X\,10^{-9}} = 0.654\,X10^{-20}J$$
$$U_4 = \frac{A}{r_4} = \frac{23.04\,X\,10^{-29}}{35.227\,X\,10^{-9}} = 0.654\,X10^{-20}J$$
$$U_5 = \frac{A}{r_5} = \frac{23.04\,X\,10^{-29}}{29\,X\,10^{-9}} = 0.794\,X10^{-20}J$$
$$U_6 = \frac{A}{r_6} = \frac{23.04\,X\,10^{-29}}{21.931\,X\,10^{-9}} = 1.050\,X10^{-20}J$$
$$U_7 = \frac{A}{r_7} = \frac{23.04\,X\,10^{-29}}{21.931\,X\,10^{-9}} = 1.050\,X10^{-20}J$$
$$U_8 = \frac{A}{r_8} = \frac{23.04\,X\,10^{-29}}{29\,X\,10^{-9}} = 0.794\,X10^{-20}J$$

$$U_{T^{12}} = \sum_{i=1}^{8} U_i = 5.998X10^{-20}J$$

$$U_{T1} = 15.608\,X10^{-20}J$$

The analysis shows that the potential energy of cell 5 in *figure 19(b)* is lower. So, cell 5 is at logic '1'. It shows the inversion of input at the output. Similarly, if cell 1 is at logic '1', cell 5 will give logic '0'.

Assumption 2: If cell-5 is logic '1' as shown in Figure 19 (b)

Figure 19(b) (Electron x)

$$U_1 = \frac{A}{r_1} = \frac{23.04\,X\,10^{-29}}{49.81\,X\,10^{-9}} = 0.462\,X10^{-20}J$$
$$U_2 = \frac{A}{r_2} = \frac{23.04\,X\,10^{-29}}{40\,X\,10^{-9}} = 0.576\,X10^{-20}J$$
$$U_3 = \frac{A}{r_3} = \frac{23.04\,X\,10^{-29}}{28.28\,X\,10^{-9}} = 0.814\,X10^{-20}J$$
$$U_4 = \frac{A}{r_4} = \frac{23.04\,X\,10^{-29}}{31.016\,X\,10^{-9}} = 0.742\,X10^{-20}J$$
$$U_5 = \frac{A}{r_5} = \frac{23.04\,X\,10^{-29}}{20\,X\,10^{-9}} = 1.152\,X10^{-20}J$$
$$U_6 = \frac{A}{r_6} = \frac{23.04\,X\,10^{-29}}{14.212\,X\,10^{-9}} = 1.621\,X10^{-20}J$$
$$U_7 = \frac{A}{r_7} = \frac{23.04\,X\,10^{-29}}{20\,X\,10^{-9}} = 1.152\,X10^{-20}J$$
$$U_8 = \frac{A}{r_8} = \frac{23.04\,X\,10^{-29}}{30.364\,X\,10^{-9}} = 0.758\,X10^{-20}J$$

$$U_{T^{11}} = \sum_{i=1}^{8} U_i = 7.277X10^{-20}J$$

Figure 19(b) (Electron y)

$$U_1 = \frac{A}{r_1} = \frac{23.04\,X\,10^{-29}}{43.863\,X\,10^{-9}} = 0.525\,X10^{-20}J$$
$$U_2 = \frac{A}{r_2} = \frac{23.04\,X\,10^{-29}}{32.280\,X\,10^{-9}} = 0.713\,X10^{-20}J$$
$$U_3 = \frac{A}{r_3} = \frac{23.04\,X\,10^{-29}}{31.016\,X\,10^{-9}} = 0.742\,X10^{-20}J$$
$$U_4 = \frac{A}{r_4} = \frac{23.04\,X\,10^{-29}}{28.284\,X\,10^{-9}} = 0.814\,X10^{-20}J$$
$$U_5 = \frac{A}{r_5} = \frac{23.04\,X\,10^{-29}}{30.364\,X\,10^{-9}} = 0.758\,X10^{-20}J$$
$$U_6 = \frac{A}{r_6} = \frac{23.04\,X\,10^{-29}}{20\,X\,10^{-9}} = 1.152\,X10^{-20}J$$
$$U_7 = \frac{A}{r_7} = \frac{23.04\,X\,10^{-29}}{14.212\,X\,10^{-9}} = 1.621\,X10^{-20}J$$
$$U_8 = \frac{A}{r_8} = \frac{23.04\,X\,10^{-29}}{20\,X\,10^{-9}} = 1.152\,X10^{-20}J$$

$$U_{T^{12}} = \sum_{i=1}^{8} U_i = 7.477X10^{-20}J$$

$$U_{T1} = 14.754\,X10^{-20}J$$

7. CONCLUSION AND FUTURE SCOPE

It is clear from the observations that, XOR gate design can be optimized from 36 cells,0.03 μm2 area and 0.75 clock cycles to

8 cells and 0.006 μm2 area and delay of just 0.5 clock cycle. We can design an XOR gate further in order to optimize these parameters like the number of cells (Package density), area and delay (Speed). Modification in the Boolean expression of the XOR gate in an innovative way or a different methodology of placement of cells can be used to achieve the best result. In the multiplexer circuit as per the latest achievement in 2:1 mux and 4:1 mux, a saving of 63.15% number of QCA cells and 66% of the area as compared to previous design approaches is achieved. The same holds as the thumb rule for implementing any digital circuitry in QCA. Researchers can make further optimization in such digital circuits for digitalization and revolution in the field of QCA.

The generation of a novel clocking scheme is needed. Power and thermal analysis is also one of the major areas to be considered for improvement and optimization. New tools can be designed to optimize quantum devices. New software for quantum dot cellular automata will be a future work that can combine parameter estimation like power, thermal analysis, and number of cells, delay and total area of the circuit layout. This will help the researchers to get the details of the circuit all at one place. Further, this will make data analysis available to the fabrication industry in an easy and faster way. QCA has applications in almost every field with miniaturization to make global digitalization. One such novel NOT gate with analysis is indicated. Standard NOT gate with fork shape has 9 cells, polarization of 9.51 with an area of 7198 $nm^{2.}$ Thus, the novel gate provides an improvement of 55% in the number of cells, polarization raised by 0.33 and 80.77% improvement in total area.

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International Journal of
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