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Performance Enhancement of CNFET-based Approximate Compressor for Error Resilient Image Processing

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ABSTRACT- The approximate computing has emerged as an appealing approach to minimize energy consumption. By implementing inexact circuits at the transistor level, significant enhancements in various performance metrics such as power consumption, delay, energy, and area can be achieved. Consequently, researchers worldwide have been actively exploring the application of inexact techniques in circuit design. This paper introduces a novel technique for designing low-power digital circuits called extremely low power modified gate diffusion input (ELP-MGDI). This technique combines the principles of Modified Gate Diffusion Input with the utilization of Carbon Nano Tube Field-Effect Transistors (CNTFETs). The Objective of this paper is to enhance the power, delay, and area characteristics of a 4:2 compressor and multiplier by employing ELP-MGDI approach. To achieve this, we conducted thorough analysis and simulations using the Verilog-A simulator 32 nm CNFET technology Stanford University within the Cadence Virtuoso Tool. The results show extremely power, delay reduction and power-delay-product (PDP) of approximate multiplier has been improved by over 99%, and the circuit area has been reduced by 55%. The proposed processing module demonstrates superior performance compared to their conventional counterparts.

Keywords: MGDI, ELP-MGDI, Approximate Compressor, Approximate multiplier, CNFET, CMOS.

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1. INTRODUCTION

The objective of approximate computing is to achieve better performance, energy efficiency, or cost by sacrificing accuracy or precision, particularly in VLSI (very large-scale integration) systems. Instead of always aiming for 100% accuracy, approximation techniques allow for a certain level of error or imprecision in computations. In the context of arithmetic circuits, the focus is often on hardware multipliers, which are complex and power-intensive units. This approach can be beneficial in applications where small inaccuracies or errors in the output do not significantly impact the system's functionality or quality. Approximate computing offers the potential to improve the performance, energy efficiency, and cost of VLSI systems, especially in scenarios where minor errors can be tolerated. However, it is crucial to carefully consider the specific needs of the application and the trade-offs between accuracy and performance. By relaxing the requirements for application accuracy, approximate computing has gained attention as a practical option for high-performance calculations. The popularity of applications that utilize data like big data analytics, machine learning, and image/video processing has increased the level of tolerance for output variances. These programmes give managing a lot of data a higher priority, and they are more accepting of allowable output variances. Another area where approximation techniques have gained prominence is approximate communication, which focuses on relaxed accuracy for energy-efficient Networks-on-Chip (NoC). As the demand for on-chip communication continues to rise, and the optimization of NoC performance and energy consumption becomes a bottleneck, approximate communication has become the standard method for connecting many on-chip components. Approximate multipliers play a crucial role in image processing due to the inherent trade-off between accuracy and computational complexity [1-2]. Image processing algorithms often involve computationally intensive operations, such as convolutions and filtering, which can benefit from approximate computing. By allowing small errors or approximations in the multiplication operations, approximate multipliers can significantly reduce computational complexity and memory requirements, leading to faster and more efficient image processing. Furthermore, in certain applications where slight inaccuracies in the image result [3-4] are tolerable, approximate multipliers offer a practical solution to achieve real-time processing, energy efficiency, and cost-effectiveness. Their importance lies in enabling high-performance image processing systems that strike a balance between computational accuracy and efficiency.

In this paper, we introduce ELPMGDI (Extremely Low Power Modified Gate Diffusion Input), a combination of Modified Gate Diffusion Input (MGDI) and Carbon Nano Tube Field-Effect Transistor (CNTFET) technologies. The main objective is to enhance the performance of an inexact multiplier [5] proposed by leveraging CNFET technology and proposed ELP-

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MGDI Full adder. This integration aims to achieve further improvements in power consumption, transistor count, and delay.

The remaining part of the paper is organized as follows. Section 2 provides a discussion of the current state-of-the-art multipliers and compressors. In Section 3, we present and compare the results of our proposed work through simulations. Finally, Section 4 concludes the paper by summarizing the findings and highlighting potential future research directions.

2. LITERATURE SURVEY

To reduce the power-delay product (PDP), designers have used a variety of techniques, including transmission gate (TG) [6], pass transistor logic (PTL) [7], gate diffusion input (GDI) [8], and Modified Gate Diffusion Input (MGDI) [9]. To address the issues in the field of deep submicron VLSI circuits, designers have used a variety of technologies. These include both established technology like complementary metal-oxide semiconductors (CMOS) and cutting-edge ones like single electron transistors, fin field effect transistors, and carbon nanotube field effect transistors. The nano-scale region presents major difficulties for conventional Metal-Oxide Semiconductor Field Effect Transistors (MOSFETs), including problems like high leakage current, short-channel effects, and process-corner fluctuations [7]. As a result, several innovative technologies have emerged in recent years to address these limitations in Nano electronics. Among these technologies, the Carbon Nano Tube Field Effect Transistor (CNTFET) has gained prominence as a promising alternative to MOSFET devices [11]. CNTFETs offer remarkable design flexibility for developing low-power and high-performance circuits, and they exhibit minimal off-current as well. The FinFET GDI logic adder demonstrates substantial reductions [3] in dynamic power when compared to other logic designs.

In comparison to [7] a Si FinFET, the CNT FinFET offers clear advantages in terms of speed and energy-delay product (EDP) due to its significantly higher current density. However, it also results in higher overall power dissipation, particularly when operating at a low threshold voltage (Vth = 1/3 V_{dd}). Among the various designs discussed, the CNTFET technology [9] stands out as a promising device with potential beyond CMOS. This is due to its device structure, which closely resembles MOSFET technology. Additionally, CNTFETs offer advantages such as higher current drive capability, improved thermal stability, and the potential for ballistic transport. These characteristics make CNTFETs a suitable candidate for future technological advancements.

A comparative analysis [12] is done on 28-transistor full adder using CMOS and CNFET Further to design low power compressors a new 4-2 compressor [13] with XOR-XNOR module and the new fast 5-2 compressor architecture is proposed. A novel full adder [10] cell utilizing a combination of gate diffusion input (GDI) and transmission gate (TG) techniques was successfully implemented using 32 nm CNTFET technology. With a total of 23 transistors, this approach effectively addressed the challenges of minimizing area occupation while achieving full swing outputs. Two complete adders connected in parallel constitute the traditional 4-2 compressor implementation, as seen in *fig. 1*, High input compressors are dissected [23] into XOR gates at the gate level and carry generators that are often implemented by multiplexers (MUX). The output Sum and the four inputs x1, x2, x3, and x4 all have the same weight. One bit orders more weight is added to the Carry output. The 4:2 compressor delivers an output Cout to the following compressor module of higher importance after receiving an input Cin from the preceding module that is one binary bit order lower in significance, the 4:2 compressor's output equations are provided in *equations (1-3)*.

$$\text{Sum}=x1 \oplus x2 \oplus x3 \oplus x4 \oplus Cin, \quad (1)$$

$$C_{out}=(x1 \oplus x2)x3 + \overline{(x1 \oplus x2)x1} \quad (2)$$

$$\text{Carry}= x1 \oplus x2 \oplus x3 \oplus x4 \oplus Cin + \overline{(x1 \oplus x2 \oplus x3 \oplus x4)x4} \quad (3)$$

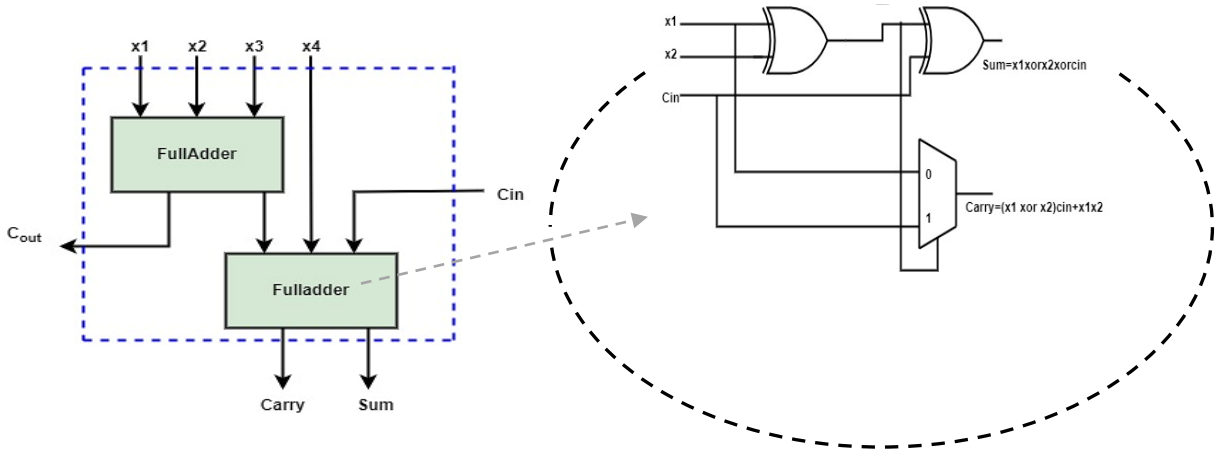

Figure 1: General Schematic of Exact 4:2 Compressor with optimized full adder schematic

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Given that Δis the unitary delay via any gate in the design, this architecture has a lengthy critical path delay of 4Δ. Numerous architectural enhancements have been suggested in the literature to enhance the functionality of the 4:2 exact compressors [14-15]. Recognizing the substantial influence of compressor cells on multiplier performance and power consumption, various approximate compressors have been introduced in previous research [16-20]. Moreover, there are alternative methodologies, such as the introduction of an efficient multiplexer-based approximate adder, which has showcased superior performance relative to existing adder architectures [24]. Additionally, Sayadi et.al have pioneered the development of approximate compressors that tactically synchronize positive and negative approximations for input patterns with matching probability distributions [25]. Reference [5] presents a hybrid approximate 4:2 compressor and an error-tolerant multiplier implemented using FinFET 7nm technology. To further improve performance, a novel technique called ELP-MGDI is proposed to achieve minimal energy consumption and high-speed operation.

3. PROPOSED WORK

The suggested ultra-compact mixed imprecise 4:2 compressor achieves a great balance between the accuracy and energy efficiency parameters. Following that, a highly effective inaccurate multiplier is created using the rough compressor as a basis. The suggested circuit is a novel version of [10] employing ELPMGDI. The main advantage of CNFET-based MGDI (ELPMGDI) is its extremely low power dissipation, area and delay efficient. CNFETs consume significantly less power than CMOS-based MGDI due to their inherent low-leakage and low-voltage operation. Maintaining a precise degree of precision appropriate for a particular set of applications while simultaneously reducing energy consumption and transistor count is the goal of an approximation compressor.

3.1 Basic Building Blocks using ELP-MGDI

The building blocks of a multiplier can be constructed using Modified Gate Diffusion Input (MGDI) technology combined with Carbon Nanotube (CNT) technology, present a promising avenue for designing high-performance and low-power multipliers. A comparison between the proposed design and conventional CMOS method is presented in *table 1*. Here, MGDI-CNFET shows on an average 99% improvement in power and 95% in delay compared to CMOS-CNFET technology and its corresponding results graph shown in Fig.3.

Table 1. Power, Delay and Transistor Count of basic blocks of Compressor

Basic blocks	Technology	Power(nW)	Delay(psec)	Transistor Count
AND	CMOS -CNTFET	58.84	50.5	6
	ELP-MGDI (proposed)	0.235	99.96	2
OR	CMOS -CNTFET	74.24	0.00917	6
	ELP-MGDI (proposed)	0.44333	0.00023	2
XOR	CMOS -CNTFET	202.4	0.00404	12
	ELP-MGDI (proposed)	0.798	99.96	4
HA	CMOS -CNTFET	261.8	0.00167	18
	ELP-MGDI (proposed)	1.158	99.96	6
FA	CMOS -CNTFET	2.584	3.814	12
	ELP-MGDI (proposed)	0.00439	182	8

By harnessing the advantages of MGDI-CNFETs based such as reduced power consumption, improved speed. Notably, the proposed compressor makes use of only two transistors using MGDI technology, which differs from conventional design methods as shown in *fig.2*.

3.2 Approximate 4:2 compressors using ELPMGDI

The objective of an approximation compressor is to strike a balance between maintaining a specific level of precision for a defined range of applications and simultaneously reducing energy consumption and the transistor count in the circuit. Author [22] designed the approximate multipliers using 4:2 and 5:2 compressors. *Figure 3* illustrates a 4:2 compressor that utilizes inputs x1, x3, and x4 to generate a Carry output using a majority gate. In this system, the Sum signal is considered constant and set to "1". By implementing a design with 12 transistors, as described in reference [18], the energy consumption and delay are significantly reduced. However, an improved design with only 9 transistors was achieved, as mentioned in reference [10]. Now, there is a further reduction in the transistor count to only 5 transistors with the implementation of the ELP-MGDI technology, which offers additional improvements in power, area, and delay, as demonstrated in *table 2.*

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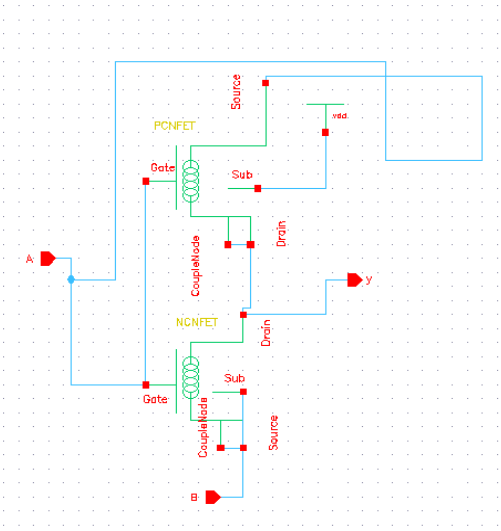
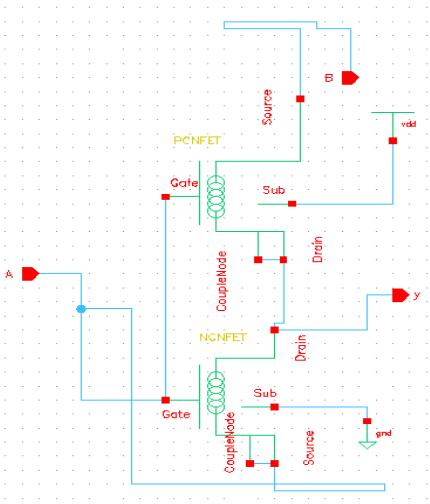
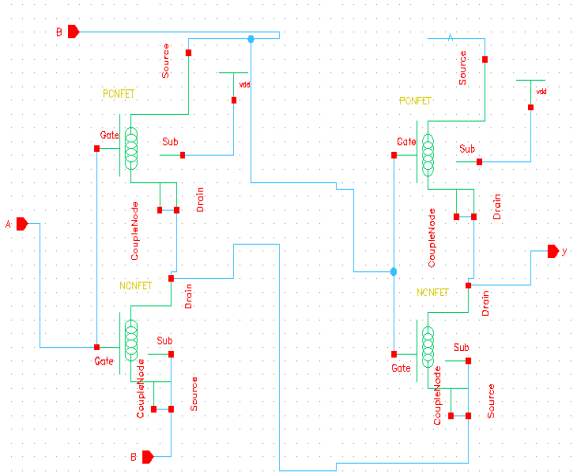


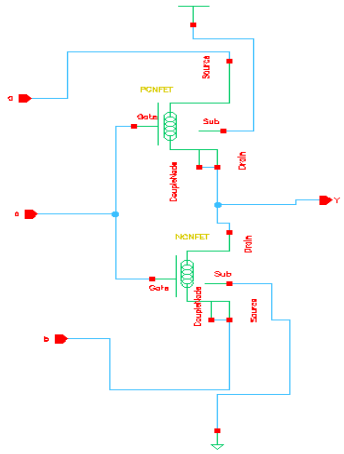
(a)ELPMGDI-AND Gate



(b) ELPMGDI-OR Gate

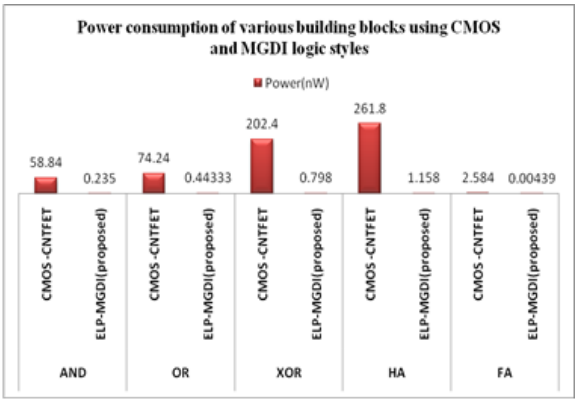


(c) ELPMGDI-XOR Gate

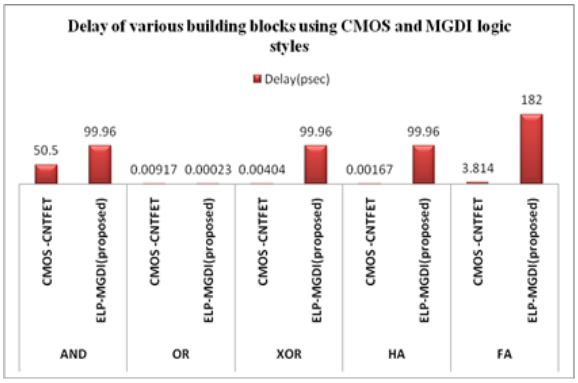


(d) ELPMGDI-MUX

Figure 2: Basic blocks of compressor using ELP-MGDI



(a) Power consumption



(b)Delay

Figure 3. Power and Delay comparison of basic blocks using CMOS- CNTFET and ELP-MGDI

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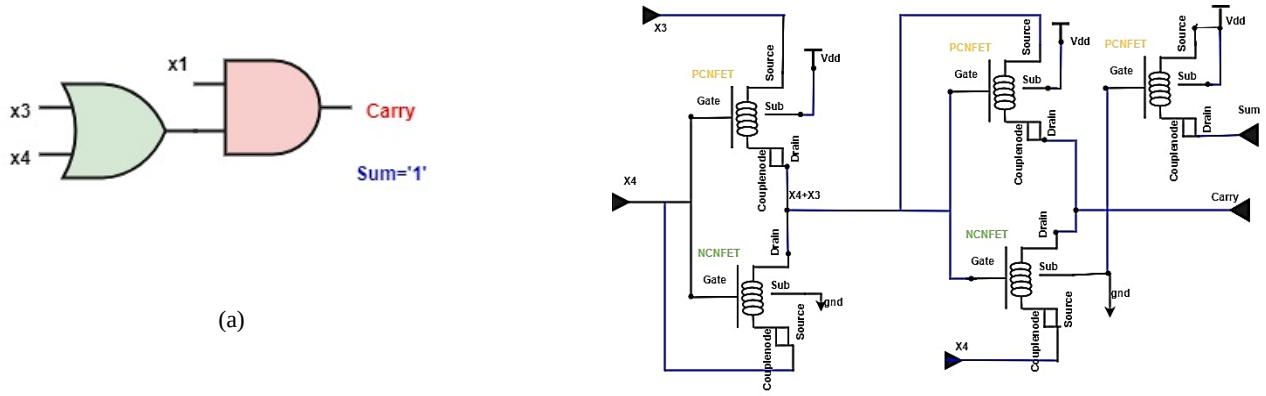
Table 2. Power, Delay and transistor count Comparison of the different approximate compressors

4:2 Compressor	Power(nW)	Delay(psec)	Transistor Count
Existing [9]	128	1.078	9
Existing [4]	128	1.068	8
Existing [5]	564.5	16.79	10
Exact Compressor-ELP-MGDI	0.00228	28.22	20
Exact Compressor [23]	838	47.75	38
Exact-Compressor-CMOS	59.52	578	56
Proposed-ELPMGDI	**0.064**	**0.0210**	**5**



(a) (b)

Figure 4. Proposed 4:2 compressor **a** gate-level schematic, **b** transistor-level design

3.3 ELP-MGDI Based Approximate Multiplier

Since digital multipliers are often able to handle mistakes, approximate multipliers are made with the intention of minimizing the size and complexity of operations yet maintaining their true purpose in mind. To reduce the size of intermediate or final outputs, compressors are essential. The reduction stage in a multiplier is especially important in terms of energy dissipation and transistor count. An evaluation is being conducted on the effectiveness [23] of employing the suggested compressors in approximate multipliers by utilizing an 8×8 unsigned Dadda tree multiplier. The partial product reduction in the suggested approximate multipliers uses both approximate and truncate section. Considered is an 8 by 8-bit unsigned Dadda multiplier, as illustrated in *figure 5*.

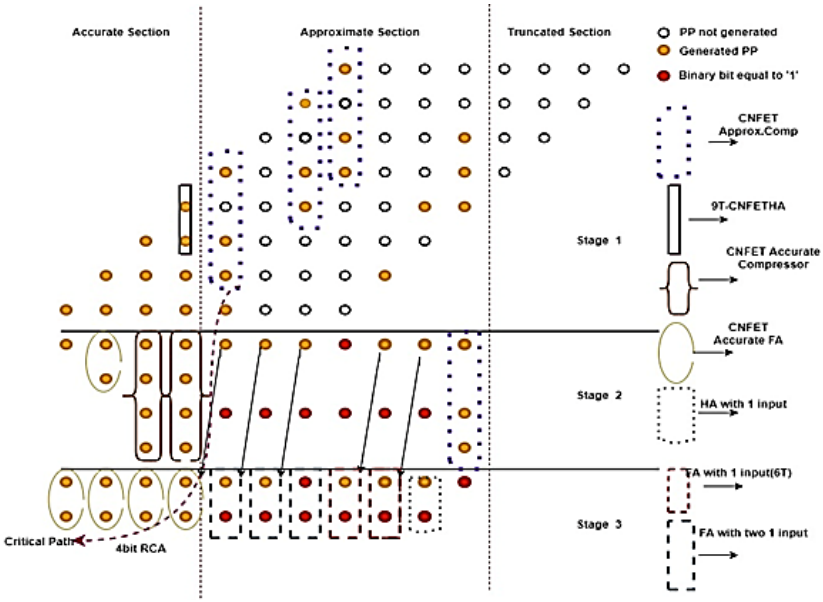


Figure 5. 8-bit approximate Dadda multiplier

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Approximation devices are then used to compress the partial results. Approximation devices are then used to compress the partial results. In the end, a ripple carrier adder (RCA) generates the output. Periodically truncating the four least significant columns has minimal impact on the precision of the multiplier. However, it leads to an improvement in hardware efficiency.

Therefore, the approximate multiplier requires two accurate compressors, four approximate compressors, five full adders, and one-half adder to be implemented successfully, along with this Half adder with '1' input and Full adder with '1' input, Full adder with two '1' inputs are used. In the stage 1, we employ three approximate 4:2 compressors along with a 6T half adder (HA). The stage 2 of design includes a 5T approximate compressor, 20T based exact compressors, and an optimized full adder (FA). By not generating partial product (represented as blank dots), as the proposed compressor do not use x2, for x2 (the number of required AND gates in our flawed multiplier is reduced from 64 to just 25. This eliminates the need for 50 transistors instead of the existing FinFET CMOS AND Gate i.e., six transistors, which requires 234 transistors. Additionally, designing an accurate compressor with this ELPMGDI technique only requires 20 transistors, whereas the existing multiplier utilizes 30 transistors. This further reduction of ten transistors significantly decreases switching power consumption. Additionally, optimized Full adders and half adders in the Ripple Carry Adder (RCA) section in stage 3. Overall, these optimizations result in a more efficient design for the multiplier, reducing hardware requirements, power consumption, and enhancing the performance further using ELP-MGDI logic style.

As a result, the critical path of proposed approximate multiplier is composed solely of the delays from one approximate 4:2 compressor (5T), one exact compressor (20T), and a four-bit optimized Ripple Carry Adder (RCA).To provide a visual representation of the final outcome, *figure 6* presents the simulation result for the 8-bit implementation where two 8-bit inputs generate 12 bit product as 4 least significant bits are truncated.

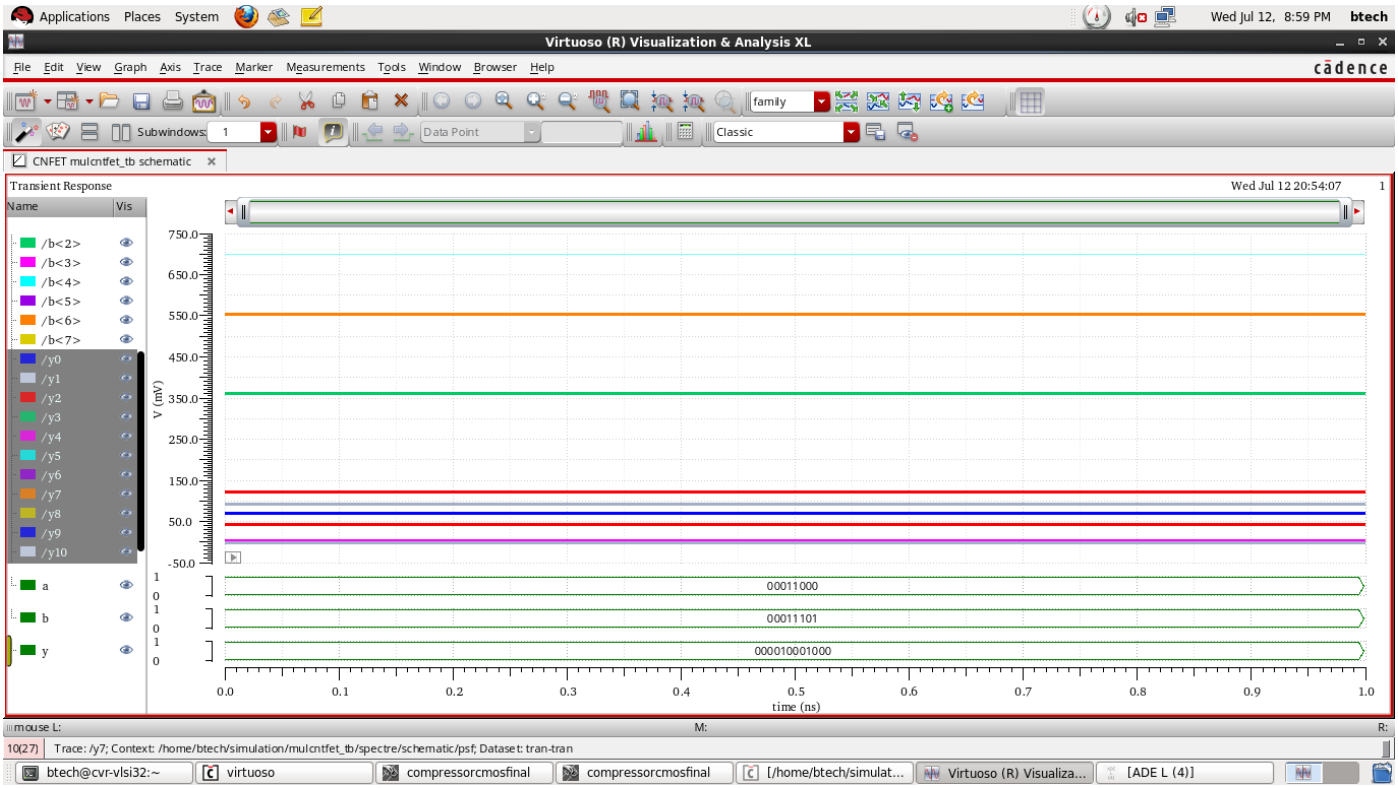

Figure 6. Simulation result of 8-bit Approximate Multiplier

4. RESULTS AND DISCUSSION

Overall, these observations demonstrate the efficiency and performance improvements achieved in the proposed multiplier design. Results of Power and Delay as depicted in *table 3* and demonstrated by the comparison graphs presented in *figure 7* and *figure 8*. The exceptional characteristic of the proposed approximate dadda multiplier results in a significantly faster speed compared to the FinFET-based approximate multiplier [10].

Table 3 Power-Delay Comparison of 8-bit Approximate Multiplier

Bit-width	Technique	POWER (μW)	DELAY (nsec)	PDP (fJ)
8-bit Multiplier	Existing FinFET [22]	9.37	0.022	2.07
	Existing FinFET [5]	3.6	0.074	0.27
	CMOS-CNTFET	5.76	356.8	2055.6
	MGDI-CNTFET (proposed)	**1.68**	**0.0228**	**36.48X 10^{-3}**

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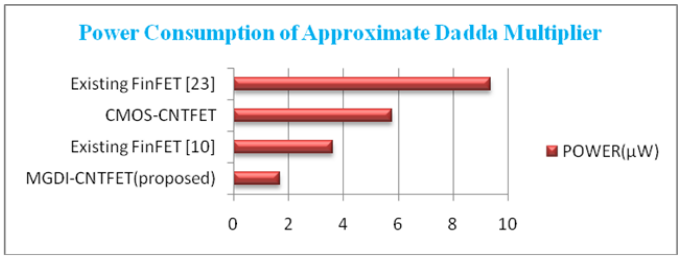

Figure 7. Power comparison of 8x8 Dadda multiplier

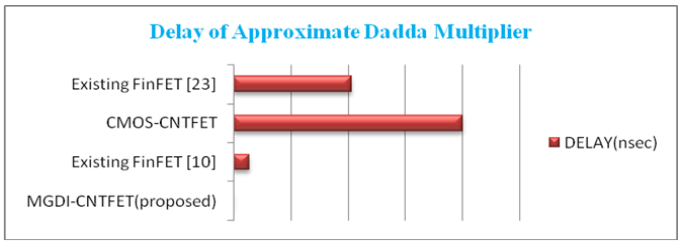

Figure 8. Delay of 8x8 Dadda multiplier

5. CONCLUSION

Both the Full Adder and the compressor cell play a crucial role in determining how well multiplication functions in entire DSP system. As a result, this work presents a unique strategy for a high-speed and extremely low power multiplier realized using MGDI-CNFET. The proposed ELP- MGDI technique shows extremely low power consumption as it takes only two transistors to implement any logic gate with less power consumption, delay compared to CMOS and FinFET Technology. The simulation results demonstrated that the ELP-MGDI 4:2 compressor, when compared to previous compressors, achieved significant reductions in transistor count, latency, power consumption, and Power-Delay Product (PDP). On average, these reductions amounted to 44.4%, 37.5%, 50%, and 57.33%, respectively. Furthermore, when compared to the approximative multipliers, these improvements reached an impressive 99%. The advantage of the suggested compressor and multiplier over its competitors has been demonstrated by simulated results at both the transistor and application levels.

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