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Design and Implementation of a Transmitter for IR-UWB Standard

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ABSTRACT- In wireless communication, the Ultrawide Band (UWB) is a technique for achieving a higher data rate, low power consumption, and less complexity. Impulse Radio - Ultra-Wide Band (IR-UWB) uses the baseband signal technique, reducing circuit complexity and power consumption. This work proposes an IR-UWB transmitter block with low power and tunable bandwidth that meets the UWB regulations of LRP (Low-Rate Pulse) UWB. The transmitter proposed uses a time-interleaved architecture using 0.18um CMOS technology using Cadence Virtuoso, which consists of On Off Keying (OOK) Circuit for the four stages of a pulse generator that operates in 6.17GHz-9.10GHz. The width of the pulse is between 0.096ns to 0.162ns using a current steering inverter. The proposed transmitter block has an output swing of 30 mV at 1MHz input Pulse Repetition Frequency (PRF) and a maximum PRF of 1GHz, at a 1GHz pulse rate, the power consumption was measured to be 8.3 mW.

Keywords: Delay circuit, bandwidth, Impulse Radio- Ultrawide Band, pulse generator, transmitter

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1. INTRODUCTION

In wireless communication, the UWB is a technique for achieving a higher data rate, low power consumption, and less complexity. The UWB subcategories are IR-UWB and Multiband-OFDM Ultra-Wide Band (MB-OFDM UWB). The MB-OFDM UWB's transceiver architecture is identical to that of traditional wireless OFDM. This leads to higher power consumption, making the system inappropriate for applications with restricted energy resources [1] [2]. IR-UWB's distinct feature is its use of the baseband signal method without a carrier signal, which reduces circuit complexity and power consumption. High-frequency pulses are generated using either Phased Locked Loops (PLL), delay blocks, or Local Oscillators (LO), and then the signal is shaped using various techniques [3]. [4] Describes using inductors and a chip-based filtering approach for carrier-based up-conversion.

The LO used in [5] and [6] is comparable to a traditional narrow-band transmitter, with a relatively large area and high-power consumption. In [7], [8], [9], and [10], it utilizes Multi-pulse Combination (MPC) with direct pulse production that solely employs digital circuits. The method demonstrated was practical and took less space. However, the issues were difficulties in obtaining the desired envelope owing to changes in the process that resulted in the employment of filters. In [11], to generate the pulse, an RLC tank employs OOK and incorporates the MPC technique. The pulse generator (PG) used in [12] is the 7th derivative of the Gaussian, which uses the 5th Gaussian derivative paired with the second-order RLC.

Generally, there are two approaches to UWB signal generation: Direct and Indirect. The Direct approach, like IR-UWB, attempts to generate wideband signals with a concise duration in time directly from the baseband signal [13]. On the other hand, the indirect approach accomplishes the wide bandwidth directly from the frequency domain using techniques like up-converting or spectrum spreading [13], [14], and [15]. The indirect method uses carrier signals, where the circuits are complex and consume more power as compared to direct pulse generation, but the limitation is limited bandwidth usage.

This work proposes an IR-UWB transmitter block with low power and tunable bandwidth that meets the LRP-UWB regulations using the Direct UWB Generation method. According to the standard specification of LRP, the spectrum allotted is from 6.2896 GHz to 9.1856 GHz. The symbols are modulated using either OOK or PPM (Pulse Position Modulation), depending on the mode. Symbols are created by combining one or more active bursts of UWB pulses. The LRP UWB PHY supports the following three transmission modes: Base mode, for the highest data rate, Extended mode, for the moderate data rate but improved sensitivity and Long-range mode, for the best sensitivity-UWB is a versatile technology with a wide range of applications due to its precise and low-

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power characteristics. It finds use in radar, high-speed data transfer, asset tracking, worker safety, and proximity sensing in both consumer and industrial contexts. This work proposes an IR-UWB with LRP designed to operate in baseband mode with a data rate of 1 Mbps and a maximum data rate of 1 Gbps, which follows the amended specification of IEEE 802.15.4-2020.

The procedure for implementing the proposed work is as follows. Initially, MATLAB (version R2023) was used for analyzing and modelling various UWB pulse shapes, gaining insights into their characteristics [15]. Identified the necessary components for the transmitter block of an IR-UWB system (Proposed block as illustrated in *figure 2*. In *section 2*, the proposed time-interleaved architecture of the IR-UWB transmitter for low power and tunable circuit is discussed, followed by the designing and implementation of the current steering delay element with an OOK Circuit using Cadence Virtuoso. Designed the individual sub-blocks of the IR-UWB system using a 180nm CMOS technology process considering the initial design specification (As indicated in *table 4*). An IR-UWB PG was designed where the parametric analysis -transient output of a single-stage Pulse- Generator with voltage control (Vcntr) (was performed, finally using the sub-blocks, we built a four-stage IR-UWB transmitter using Cadence Virtuoso for which the results discussed were considered *section 3*.

Optimized the design parameters of these sub-blocks to meet specific performance specifications. Finally Integrated the sub-blocks into the IR-UWB Transmitter using Cadence Virtuoso, ensuring functional connectivity and overall system performance as illustrated in *figure 9*. In this work, we have optimized the power of the four-stage IR-UWB by parametric analysis of the circuit components in order to reduce the power consumption. Also, parametric analysis was carried out to measure the S-parameter for the IR-UWB transmitter using cadence virtuoso *section 4.* Throughout the process, rigorous testing and simulation are crucial to validate that the IR-UWB transmitter meets its intended specifications and functions as required. Finally, the verified circuit from Cadence Virtuoso in 180nm can be further proceeded for fabrication of the IC.

2. IR-UWB TRANSMITTER BLOCK DIAGRAM

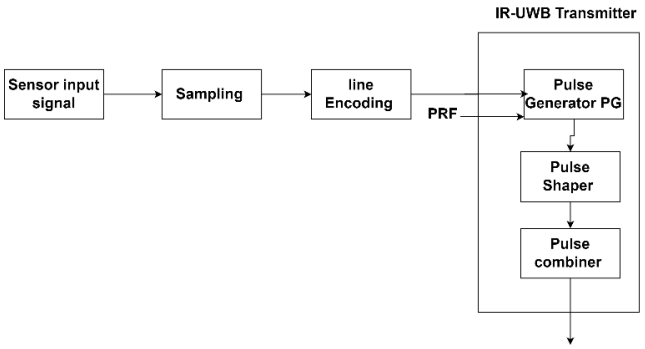

Figure 1: Block of transmitter system (with IR-UWB Block)

Figure 1 shows the block diagram of the transmitter system (with IR-UWB Block). The inputs are sensed and converted to appropriate digital data using sampling and line encoding as in a traditional transmitter. Followed by an UWB transmitter block consisting of a pulse generator, pulse shaper, and pulse combining block. This work proposes an IR- UWB transmitter block with low power consumption and Tunable bandwidth that meets the UWB regulations. The baseband signal of low frequency will be the input to the pulse-generator block.

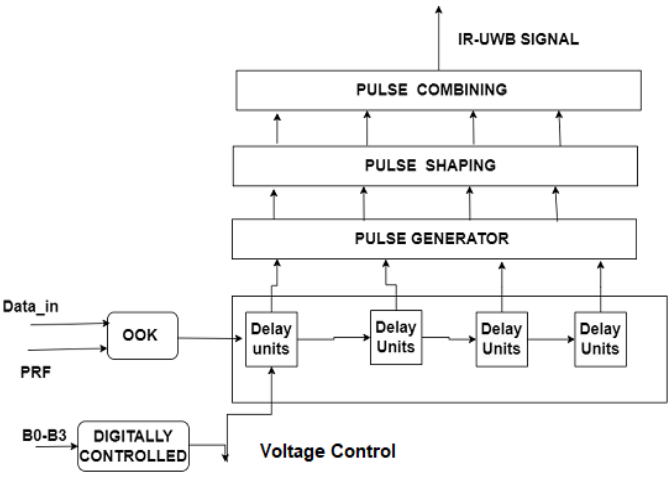

Figure 2: Time-interleaved architecture of IR-UWB transmitter Proposed

The proposed block diagram of the IR-UWB transmitter is indicated in *figure 2*. It is challenging to produce a pulse with a width ranging in a few nanoseconds, which makes the pulse generator a crucial component of an IR-UWB transmitter. A UWB signal is created by combining the generated pulses in the pulse-combining block. In this work, a finite impulse response (FIR) filter consisting of transistors is proposed which is an active filter. Time-interleaved architecture for IR-UWB System that is proposed is indicated in *figure 2*. The baseband signal, typically in MHz, are input to the Delay Unit. A pulse-generator generates a pulse that is further pulse-shaped to produce a signal of either a "1" or a "0." In order to achieve a tunable IR-UWB transmitter circuit, we have used the inputs B3-B0 which are the digital inputs to the current steering delay element. They are used to digitally control the delay in the circuit which in turn tunes the width of the pulse of the IR-UWB transmitter. The narrow pulses generated by the logic gates of the impulse generator are merged to produce the UWB signal using combining circuits.

To have bandwidth optimization, we have proposed the delay cell using a current-steering circuit. Tunable and low power are the main goals of this work. The OOK is incorporated into our design as a low-power circuit as in *figure 3*, where the input to this block is the Data_in and the Pulse Repeating Frequency (PRF) and the output is the Data_in_ook. Where INV is an inverter and transistor NM2 is responsible for charge leakage and potential locking. The transistors (NM1 and PM1) serve as a transmission gate that sends a clock signal (PRF) to the output Data_in_ook under the command of the baseband data signal (Data_in). When the data signal is '1', the clock signal (PRF) is transmitted to the output. Otherwise, the output signal is a low-

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level '0' signal. As a result of this. The baseband signal modulates the PRF. The pulse is generated using the designed logic gates, delays, and combining circuit to generate a narrow pulse for a bit 1 and no pulse for a bit 0.

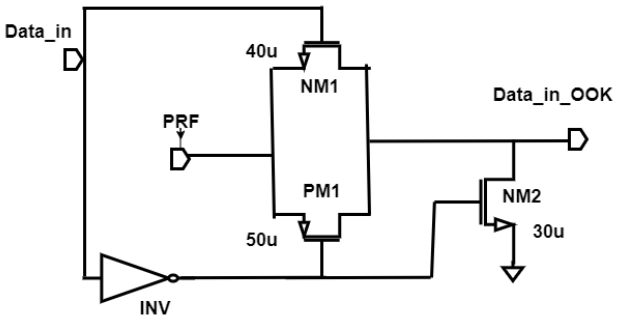

Figure 3: On-Off keying circuit

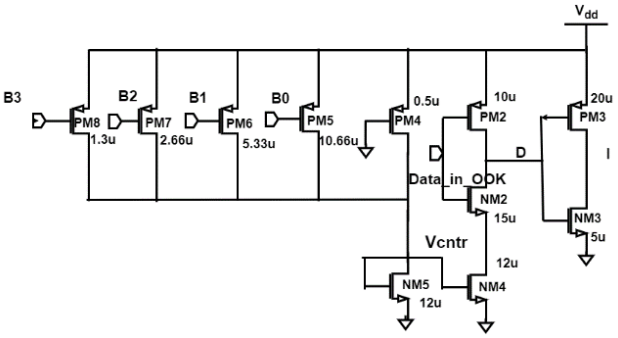

Figure 4: Current steering delay element

The proposed current steering delay elements circuit is depicted in *figure 4*. The main component is a current-steering buffer made up of NM4, NM3, NM2, PM2, and PM3. An NM5-NM4 transistor current mirror circuit controls the regulating current flowing through this buffer. Transistors PM5–PM8 can be turned on through digital inputs B3-B0 to change the current flowing through MN4 while PM4 is always on. To get maximum delay width of PM4 was varied between 0.5u to 20u. It was observed that at W=0.5u the maximum delay is achieved henceforth we fix the value of PM4 as W=0.5u. After sizing PM4, place one PMOS transistor (PM0) in parallel to PM4 and size it to obtain the minimum required delay. We varied between W=0.5u to 20u. Once we find the value of PM0. where the minimum delay is achieved, we fix the value of PM0 as W=20u. This value is used in *equation 1* for the width of MP0. This PM0 is broken into N Transistors in binary fashion using Equation 1

$$(w/l)\_((Mpi))=2\text{^}((i-1)\ )2\text{^}N -1\ (w/l)\_((Mp0)) \qquad (1)$$

Where *i*=1,2,3,4 Substituting in the above equation we get (w/l)Mp1= 1.3u/1.8u as indicated in *figure 4* for PM6,similarly (w/l)Mp2= 2.66u/1.8u for PM8 ,(w/l)Mp3= 5.33u/1.8u for PM7 and (w/l)Mp4= 10.66u/1.8u for PM5 .

Figure 5 and *figure 6* are the waveforms for the delay cell with digital inputs (16 variations) through the four PMOS transistors. The four digital input sequences B3-B0 (*figure 4*) as input (where CLK at 10GHz, CLK by 16 at 625MHz, CLK by 8 as 1.25GHz, CLK by 4 as 2.5GHz, and CLK by 2 as 5GHz *figure 4*).

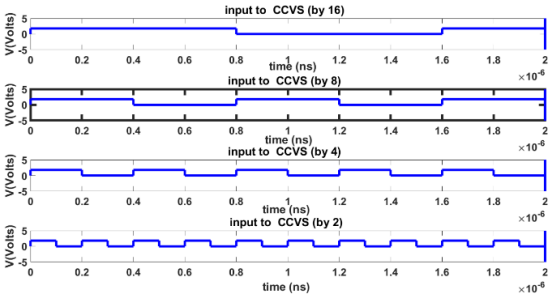

Figure 5: Waveform1 for the delay cell with the current steering delay element

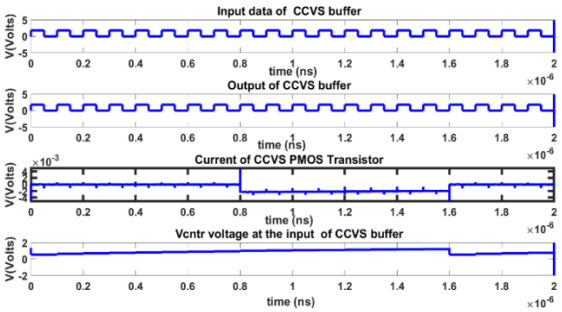

Figure 6: Waveform2 for the delay cell with the current steering delay element

When the digital input is 1111, the corresponding *Vcntr* is less and produces a longer delay which helps to design pulses with a longer delay. Also, it's observed that when the digital input is 0000, the corresponding *Vcntr* is high and produces a smaller delay which helps to design pulses with a shorter delay. *Vcntr* was varied between 0.5V to a maximum of 1.43V (*figure 6*). As indicated in *table 1* for the digital input between 1111 to 0000, to the current steering delay element the corresponding *Vcntr* was measured between 545mV to 1430mV. It is observed that as Input varies from 1111 to 0000 the *Vcntr* was increasing.

Table 1: Digital input to the delay element circuit and the corresponding Vcntr generated

Sl.no	digital input B3-B0	Vcntr (mV)	Sl.no	digital input B3-B0	Vcntr (mV)
1.	1111	545	9.	0111	1020
2.	1110	644	10.	0110	1040
3.	1101	709	11.	0101	1070
4.	1100	763	12.	0100	1100
5.	1011	810	13.	0011	1230
6.	1010	855	14.	0010	1320
7.	1001	897	15.	0001	1352
8.	1000	937	16.	0000	1430

3. IR-UWB PULSE GENERATORS (IR-UWB PGS)

Figure 7 is the delay circuit with Vcntr to tune the delay, which in turn controls the frequency of the IR- UWB signal. The delay circuit is proposed to achieve an extensive tuning range. The

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delay tuning voltage *Vcntr* applied to the NMOS NM4 regulates the amount of current flowing through the inverter. The drain current and delay time have an inverse relationship that controls the NMOS Transistor. Both the controlling transistor and the inverter transistors are in linear regions,

For nmos transistor *Vgsn > Vthn and Vdsn < Vgsn-Vthn*
For pmos transistor *Vgsp < Vthn and Vdsn > Vgsn-Vthn*

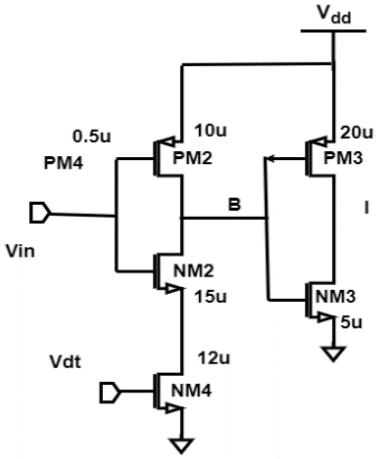

Figure 7: Schematic of delay unit with Vcntr

Figure 8 shows the Virtuoso ADE transient analysis - parametric of the circuit (*figure 7*), Considering Vcntr 0.6V to 1.8V. If Vcntr is less, then the drain current is less, and there will be more delay. and vice-versa. By varying Vcntr between 0.7V to 1.8V, the current varies linearly, and hence delay varies linearly as in *figure 7*.

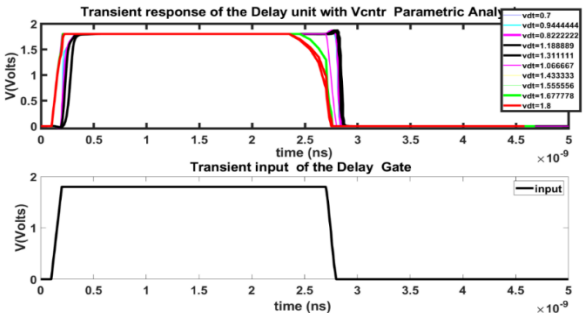

Figure 8: Transient response of the delay unit with Vcntr - parametric analysis

Figure 9 shows the schematic of the four-stage PG with Vcntr consisting of a Nand gate and inverters to get a narrow pulse. Next, it includes a pulse combiner using NMOS and PMOS transistors to combine both the positive and negative pulse to form a narrow pulse that follows the UWB regulation. The final stage is the coupling circuit and 50-ohm load to represent the antenna. The delay or buffer uses the current steering inverter to achieve an extensive tuning range. Vcntr is applied to the buffer/ delay cell through NMOS gate, which sets the current *i.e.*, the inverter is starving for the current. By varying Vcntr, the current varies linearly, and hence the delay varies linearly.

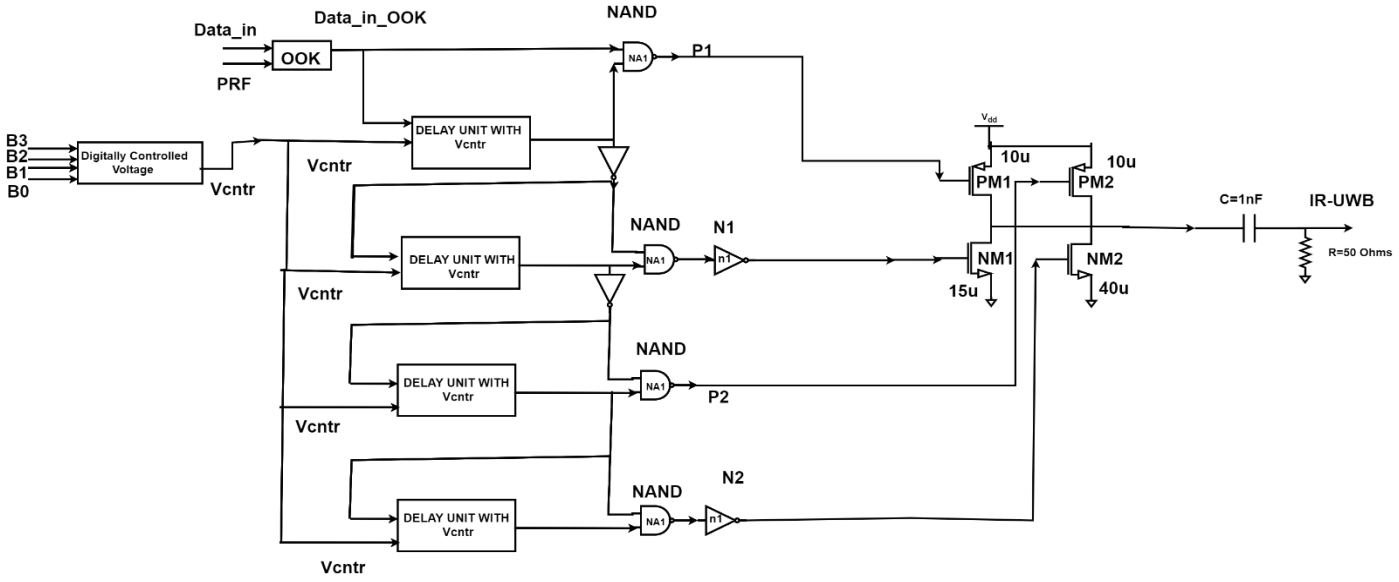

Figure 9: Schematic test of four stages of pulse generator

4. RESULTS AND DISCUSSION

4.1 Delay Variation due to Vcntr

Figure 10 shows the parametric analysis of the pulse-generator (PG) with Vcntr varying between 0.6 V to 1.8 V of a single stage PG using Vcntr. By varying Vcntr, the current varies linearly, and hence the delay varies linearly, as tabulated in *table 2*. It is observed that the delay is less as Vcntr increases. The minimum Vcntr for the circuit is the threshold voltage of the transistor, which is considered as 0.7 V. In our design we have considered from 1V and the max control voltage for the circuit is 1.4 V. As indicated in *table 2* the bandwidth of operation for this range of control voltage is between 6.17GHz to 9.10GHz (considering Vcntr between 1V and 1.3V).

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Table 2: Calculation of delay variation due to Vcntr

Vcntr (V)	Delay (ns)	Frequency (GHz)
1	162ps=0.162ns	6.17GHz
1.2	113ps=0.113ns	8.8GHz
1.3	109ps=0.109ns	9.10GHz
1.4	96ps=0.096ns	10.41GHz

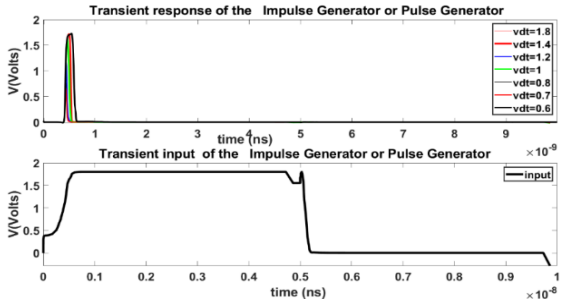

Figure 10: Parametric analysis setup and transient output of single-stage pulse- generator with Vcntr

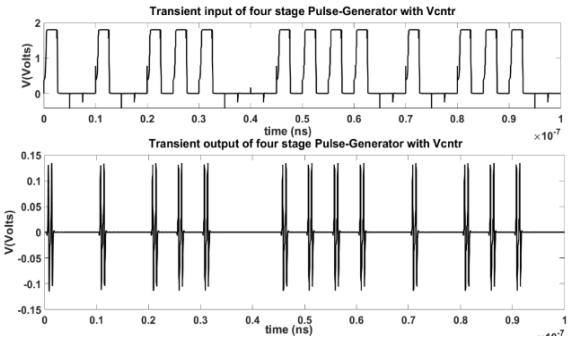

Figure 11: The transient output of a four-stage pulse-generator with Vcntr

4.2 Transient response, DC power, and transient power

Figure 11 shows the transient of a four-stage pulse-generator, where net3 is the data input, and net048 is the 4-stage output of the pulse generator at 1GHz input data. It is observed that UWB pulse is generated only if the data is 1 which works on OOK modulation which is a solution to low power circuits. In *figure 12.* The total transient power of the four stages pulse-generator with Vcntr using Cadence virtuoso was measured to be 45mw after optimization of the circuit. In *figure 13* the total dc power of the four-stage Pulse-Generator with Vcntr using Cadence Virtuoso was measured to be 8.5mw after optimization of the circuit.

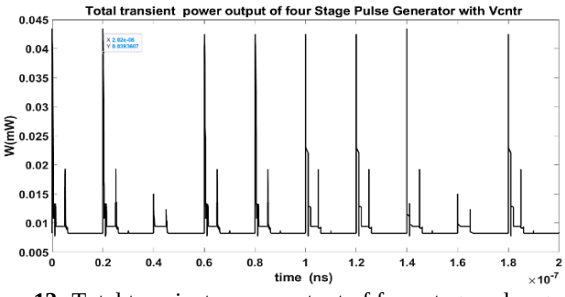

Figure 12: Total transient power output of four-stage pulse-generator with Vcntr

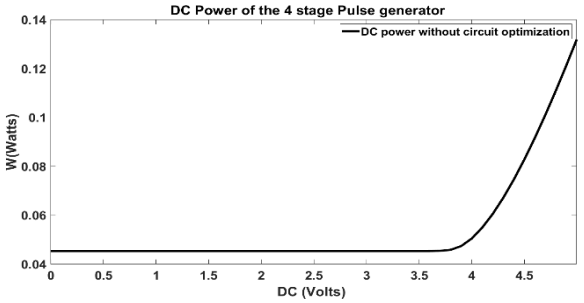

Figure 13: Total dc power output of four stage pulse- generator with Vcntr

4.3 The Spectrum of an Impulse generator or Pulse generator of four stages

The Spectrum measured for the four-stage IR-UWB using Cadence Virtuoso is shown in *figure 14*. It shows the spectrum measurement where Fc changes as Vcntr changes. Its analyzed that as Vcntr increases, the Fc also increases. In this work, the design of the four-stage IR UWB transmitter is implemented in cadence virtuoso 0.18um CMOS process. Its Transient response is as shown in *figure 15*. As listed in *table 3* the parametric analysis is carried out by varying Cp for Vcntr between 1V and 1.4V at various values of C, where the Vcntr is between 1V - 1.4V.

Table 3: Vcntr between 1V and 1.4V at various values of C where the S11 below-10db is ideal

C(PF)	Frequency (GHz) Fc	S11(dB) at Fc	Bandwidth
0.5PF	8.6GHz	-12.95dB	7.89GHz-8.99GHz
0.66PF	9.00GHz	-17.26dB	8.089GHz-.765GHz
0.833PF	9.61GHz	-21.29dB	8.42GHz - 10.6GHz
1.2PF	10.23GHz	-14.26	9.1GHz - 11.24GHz

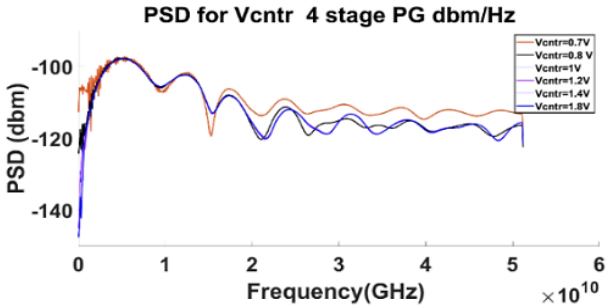

Figure 14: The spectrum of the impulse generator or pulse-generator (PG) of four stages using Vcntr for various values 1V and 1.4V (net048)

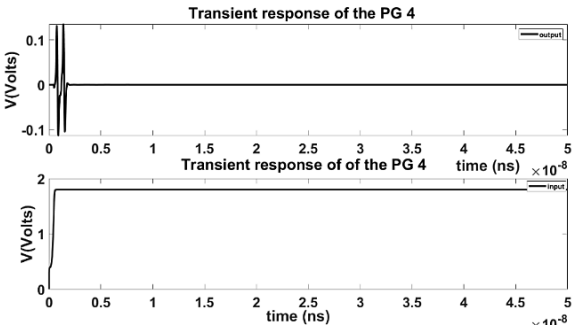

Figure 15: ADE transient response of four stages using Vcntr

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The described test setup employs Cadence Virtuoso ADE for S-parameter analysis in the context of an IR-UWB transmitter design. The setup comprises two ports: Port 0, configured as the input with a 10 ns bit waveform source, and Port 1, designated as the output with a 50-ohm DC source representing the transmitter's antenna. A broad frequency sweep spanning from 1 GHz to -10 GHz is performed to comprehensively assess the system's behavior. S-parameter analysis is visualized in rectangular plots with a dB20 scale, encompassing all four S-parameters (S11, S12, S21, and S22) to characterize signal reflections and transmissions at input and output ports. The direct plot form within Cadence Virtuoso ADE streamlines data visualization. Furthermore, the evaluation of the IR-UWB transmitter's performance includes parametric analysis, systematically varying capacitance (C) between 0.5 pF and 1.2 pF (as indicated in *figure 16-19*). These analyses are crucial for optimizing the transmitter design, ensuring impedance matching, power transfer, and signal integrity within the specified frequency range. Such meticulous S-parameter analyses are fundamental in RF and microwave circuit design to validate and enhance the functionality of transmission systems and components.

Figure 16 shows the S11 parameter measured by varying the C between 0.5PF to 1.2PF. The bandwidth of the designed IR UWB transmitter is considered between 7.89GHz -10.6GHz by S parameter analysis For S11 below -10dB even though the PSD shows a more extensive range as tabulated in *table 3*. *Figure 17* shows the S22 parameter that was measured by varying C between 0.5PF to 1.2PF. The output return loss measured was less than - 1.5dbB. *Figure 18* shows the S12 parameter that was measured by varying C between 0.5PF to 1.2PF. S12 reverse isolation loss is less than -90dB. *Figure 19* shows the S21 parameter that was measured by varying C between 0.5PF to 1.2PF. S21, the gain of the circuit is -125dB.

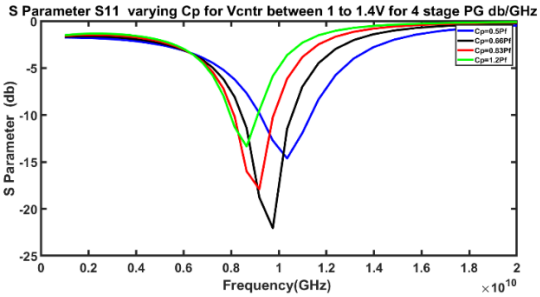

Figure 16: S11 measurement— parametric analysis of IR-UWB transmitter

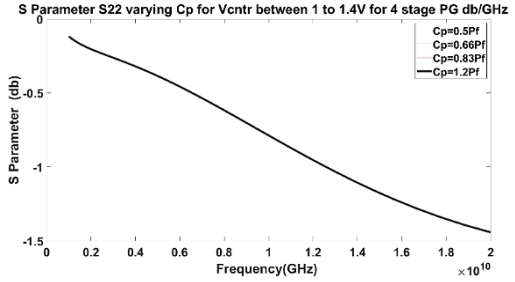

Figure 17: S22 measurement— parametric analysis of IR-UWB transmitter

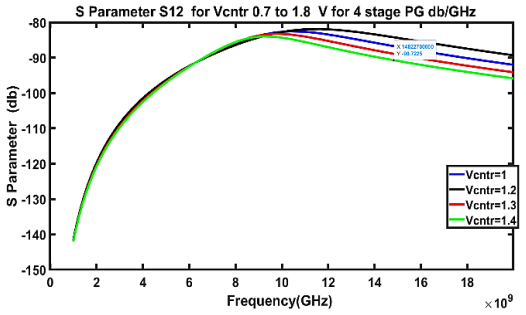

Figure 18: S12 measurement— parametric analysis of IR-UWB transmitter

Table 4 gives the initial design specifications and the designed specification of this Work. Finally, *table 5*, compares the performance summary of this work. We have used a 180nm process technology since it is a well-established technology with a long track record of reliability. Designing and prototyping chips in a 180nm process can be faster and require fewer design iterations compared to other advanced process technologies. This can lead to quicker time-to-market for certain products. The modulation used in our work is OOK which is a solution for low-power circuits as compared to other modulation schemes. The output amplitude of the designed transmitter is 30mv and the energy dissipation is 8PJ/ Pulse where the power consumption measured was 8mW at 1GHz input data rate.

Table 5 compares our work with previous works. In this proposed work the Bandwidth achieved is up to 2.4GHzThe proposed system is a low complex, low power consumption and a tunable circuit for an IR-UWB System with bandwidth achieved is up to 2.4GHz. To summarize, we propose the time-interleaved Architecture of the IR-UWB Transmitter for low power and tunable circuit that is designed and implemented using Cadence Virtuoso in 0.18um CMOS technology. In order to build a transmitter with tunablity the current steering delay element was designed. The pulse generator, the core of the IR-UWB transmitter was designed where the parametric analysis - transient output of the single-stage pulse- generator with Vcntr was performed. Finally used these sub-blocks to build a four-stage IR-UWB transmitter. In this work we have optimized the power for the four-stage IR-UWB by parametric analysis of the circuit components to reduce the power consumption and also parametric analysis was carried out for measuring the S-parameter for the IR-UWB transmitter using cadence virtuoso.

5. CONCLUSION

The all-digital tunable IR-UWB transmitter proposed uses a time interleaved architecture that consists of four stages of a pulse generator that operates in the frequency range of 6.17GHz-9.10GHz, designed using 0.18um technology and has a lower design complexity than other architectures that use LO, power amplifiers, and Mixers. The proposed tunable delay makes the system efficiently use the IR-UWB bandwidth by giving digital input to the current steering that can be varied between 0.5V to 1.43V. For the designed circuit in this work, the pulse width is between 0.096ns to 0.162ns using a current steering inverter that makes the generated signal meet theLRP

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UWB regulations. The proposed transmitter block has an output swing of 30 mV at 1MHZ input PRF and a maximum PRF of 1GHz. At a 1GHz pulse rate, the power consumption was measured to be 8.3 mW. The OOK modulation technique incorporated in the design enhances power efficiency, making the transmitter well-suited for battery-powered devices and other low-power applications. The transmitter's adaptability makes it suitable for a wide range of applications, including security systems and various consumer electronics. Since the design is only on the transmitter it's limited to Medical Applications where accuracy and deviations are major concerns.

Table 4: Performance Summary of this Work

Parameters	Initial Design Specification	Designed Specification
Technology	0.18µm CMOS	0.18µm CMOS
Bandwidth (Transient response)	6.2896 GHz to 9.1856 GHz	6.17GHz-9.10GHz
Bandwidth (PSD and S parameter)	6.2896 GHz to 9.1856 GHz	7.89GHz – 10.6 GHz
Tunable pulse width	< 2ns	0.096ns to 0.162ns
PRF	1 MHz	1 MHz
Maximum PRF	1 GHz	1 GHz
Transmit power density	<-41.3 dBm/MHz.	-97dBm/MHz
Maximum Power Consumption	< 15mW	8.3mW at 1GHz PRF
Energy Dissipation	15PJ/Pulse	8.3 pJ/Pulse
Power Supply	1.8V	1.8V

Table 5: Performance summary and comparison with other works

Parameter	[16]	[17]	[18]	[19]	[20]	[21]	[22]	[23]	[24]	[25]	This work
Process(nm)	180	65	180	130	130	180	180	180	180	180	180
Modulation	DBPSK	OOK	BPSK	N/A	FM	OOK	OOK	OOK/PPM	OOK/PPM	OOK	OOK
Output Amp(mV)	640	750	1000	940	NA	56	100	67	60	13	30
Tunable Frequency	No	No	No	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes
Energy Dissipation (pJ/bit)	N/A	21.6	86	3.6	987	N/A	50	50	45	15	8
Data Rate (Mbps)	36	10	250	10	1.0	31.25	1 Gbps	1 Gbps	16Mbps-Max 1Gbps	1 Gbps	1Mbps/1 Gbps max
Freq. (GHz)	3.1–5.1	3.1–8	3.5–6.5	3.1–4	3.5–4	3.1–10.6	0.5GHz-5.5GHz	0.5GHz-5.5GHz	3-9GHz	1GHz-8GHz	6.17GHz-9.10GHz
Supply Voltage (V)	2.2	1.2	1.8	1.2	1.2	1.8	1.8	1.8	1.8	1.8	1.8

REFERENCES

[1] Radic, J., Djugova, A., Nagy, L., & Videnovic-Misic, M. (12 ,2013). New design of low power, 100 Mb-s IR-UWB pulse generator in 0.18 mu m CMOS technology. Microelectronics Journal, 44, 1215-1222. doi:10.1016/j.mejo.2013.08.007

[2] Lee, K. K., & Lande, T. s. (12 ,2014). A 2.8–7.5 pJ/Pulse Highly-Flexible Impulse-Radio Ultra-Wideband Pulse-Generator. Progress In Electromagnetics Research C, 55, 139–147. doi:10.2528/PIERC14110301

[3] Wu, J., Wang, W., Liang, Q., Wu, X., & Zhang, B. (2014). Compressive Sensing-Based Signal Compression and Recovery in UWB Wireless Communication System. 14(13). doi:10.1002/wcm.2228

[4] Chang. (12 2005). CMOS 5th Derivative Gaussian Impulse Generator for UWB Application.

[5] Campbell, S. L., & Gear, C. W. (1995). The index of general nonlinear DAES. Numer. Math., 72(2), 173–196.

[6] Sim, S., Kim, D.-W., & Hong, S. (2009). A CMOS UWB Pulse Generator for 6-10 GHz Applications. IEEE Microwave and Wireless Components Letters, 19(2), 83–85. doi:10.1109/LMWC.2008.2011318

[7] Zhou, L., Chen, Z., Wang, C.-C., Tzeng, F., Jain, V., & Heydari, P. (2011). A 2-Gb/s 130-nm CMOS RF-correlation-based IR-UWB transceiver front-end. IEEE Transactions on Microwave Theory and Techniques, 59(4), 1117–1130

[8] Ryckaert, J., Van der Plas, G., De Heyn, V., Desset, C., Van Poucke, B., & Craninckx, J. (2007). A 0.65-to-1.4 nJ/Burst 3-to-10 GHz UWB All-Digital TX in 90 nm CMOS for IEEE 802.15.4a. IEEE Journal of Solid-State Circuits, 42(12), 2860–2869. doi:10.1109/JSSC.2007.908665

[9] Lee, K. K., Dooghabadi, M. Z., Hjortland, H. A., Næss, & Lande, T. S. (2011). A 5.2 pJ/pulse impulse radio pulse generator in 90 nm CMOS. 2011 IEEE International Symposium of Circuits and Systems (ISCAS), 1299–1302. doi:10.1109/ISCAS.2011.5937809

[10] Zhao, M. J., Li, B., & Wu, Z. H. (2013). 20-pJ/Pulse 250 Mbps Low-Complexity CMOS UWB Transmitter for 3-5 GHz Applications. IEEE Microwave and Wireless Components Letters, 23(3), 158–160. doi:10.1109/LMWC.2013.2245412

[11] Kulkarni, V. V., Muqsith, M., Niitsu, K., Ishikuro, H., & Kuroda, T. (2009). A 750 Mb/s, 12 pJ/b, 6-to-10 GHz CMOS IR-UWB transmitter with embedded on-chip antenna. IEEE Journal of Solid-State Circuits, 44(2), 394–403. doi:10.1109/JSSC.2008.2011034

[12] Batur, O., Akdag, E., Akkurt, H. K., Oncu, A., Koca, M., & Dundar, G. (11, 2012). An ultra low-power dual-band IR-UWB transmitter in 130-nm CMOS. Circuits and Systems II: Express Briefs, IEEE Transactions On, 59, 701–705. doi:10.1109/TCSII.2012.2218474

[13] De Oliveira, A., Garay, J. R., Justo, J., & Kofuji, S. (08 2013). A Complete Ultra Wide Band Transmitter System for Impulse Radar. Recent Patents on Engineering, 7, 133–139. doi:10.2174/1872212111307020006

[14] Susan, S. Sophiya, & Yellampalli, S. S. (2019). UWB System: Its Regulations Trends and Applications. International Journal of Recent Technology and Engineering (IJRTE) ICETESM, 7.

[15] Susan S., S., Gupta, K. A., & Yellampalli, S. S. (2020). Analysis of a Transmitter System for IEEE 802.15.4a UWB Standard. 2020 2nd International Conference on Innovative Mechanisms for Industry Applications(ICIMIA), 54–59. doi:10.1109/ICIMIA48430.2020.9074963

[16] Norimatsu, T., Fujiwara, R., Kokubo, M., Miyazaki, M., Maeki, A., Ogata, Y., … Sakamura, K. (2007). A UWB-IR Transmitter With

International Journal of
Electrical and Electronics Research (IJEER)
Research Article | Volume 11, Issue 4 | Pages 909-916 | e-ISSN: 2347-470X

Digitally Controlled Pulse Generator. IEEE Journal of Solid-State Circuits, 42, 1300–1309.

[17] Zhang, Z., Li, Y., Mouthaan, K., & Lian, Y. (2018). A Miniature Mode Reconfigurable Inductorless IR-UWB Transmitter - Receiver for Wireless Short-Range Communication and Vital-Sign Sensing. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 8(2), 294–305. doi:10.1109/JETCAS.2018.2799930

[18] Gunturi, P., Emanetoglu, N. W., & Kotecki, D. E. (2017). A 250-Mb/s Data Rate IR-UWB Transmitter Using Current-Reused Technique. IEEE Transactions on Microwave Theory and Techniques, 65, 4255–4265.

[19] Zhang, Z., Li, Y., Wang, G., & Lian, Y. (2018). The Design of an Energy-Efficient IR-UWB Transmitter With Wide-Output Swing and Sub-Microwatt Leakage Current. IEEE Transactions on Circuits and Systems II: Express Briefs, 65(10), 1485–1489. doi:10.1109/TCSII.2018.2861833

[20] Ali, M., Shawkey, H., Zekry, A., & Sawan, M. (2018). One Mbps 1 nJ/b 3.5 - 4 GHz Fully Integrated FM-UWB Transmitter for WBAN Applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 65(6), 2005–2014. doi:10.1109/TCSI.2017.2771369

[21] Baolin Wei, Tian Chen, Chao Lu, Weilin Xu, Yuanzhi Zhang, Xueming Wei, Hongwei Yue, & Jihai Duan (2019). An all-digital frequency tunable IR-UWB transmitter with an approximate 15th derivative Gaussian pulse generator. Integration, 69, 301-308.

[22] Zhu, Y., Zuegel, J., Marciante, J., & Wu, H. (2019). Distributed Waveform Generator: A New Circuit Technique for Ultra-Wideband Pulse Generation, Shaping and Modulation. Solid-State Circuits, IEEE Journal of, 44, 808 - 823. doi: 10.1109/JSSC.2019.2013770.

[23] Zhu, Y., Zuegel, J., Marciante, J., & Wu, H. (2018). A 10.9GS/s, 64 Taps Distributed Waveform Generator with DAC-Assisted Current-Steering Pulse Generators in 0.18μm Digital CMOS. IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, Orlando, FL, USA, 2018, pp. 13-16, doi: 10.1109/SMIC.2018.10.

[24] Zhu, Y., Hu, J., & Wu, H. (2019). A 2.5 Gpulse/s, 25 pJ/pulse, 0.18μm CMOS Impulse Radio UWB Transmitter Based on Dual-Polarity Distributed Waveform Generator. In 2019 IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (pp. 1-4). doi: 10.1109/SMIC.2019.4770540.

[25] Janaki, S., & Yellampalli, S.S. (2013). Design of impulse distributed waveform generator. 2013 Fourth International Conference on Computing, Communications and Networking Technologies (ICCCNT), 1-6.