FOREX Publication
Open Access | Rapid and quality publishing

International Journal of
Electrical and Electronics Research (IJEER)
Research Article | Volume 11, Issue 4 | Pages 939-943 | e-ISSN: 2347-470X

A Symmetric Multi-Level Cascaded H-Bridge Inverter for Renewable Energy Integration

S. Muthukaruppasamy[1], K. Sarada[2], Priya R. Patil[3], and R. Dharmaprakash[4]
[1]*Department of EEE, Velammal Institute of Technology, Panchetti, Chennai, mksamy14@yahoo.com*
[2]*Department of EEE, Koneru Lakshmaiah Education Foundation, Vaddeswaram, sarada@kluniversity.in*
[3]*Department of EE, Shree Ramchandra College of Engineering, Pune, priyapatil.srcoe@gmail.com*
[4]*Department of EEE, Panimalar Engineering College, Chennai, rdharmaprakash@yahoo.co.in*

***Correspondence:** S. Muthukaruppasamy; mksamy14@yahoo.com

ABSTRACT- The advanced multi-level cascaded H-Bridge inverter system described in this paper is novel and intended for effective integration of renewable energy sources. Phase-displacement pulse width modulation (PD-PWM) control has been employed in the proposed five-level topology to produce output voltage with better quality. The system incorporates proficient filtering methods with a low total harmonic distortion (THD) desired outcome. With a stable output of 230 V at 50 Hz and a 2.3 kW capacity, the inverter system has been satisfied the exacting IEEE 519 standards for power quality. The MATLAB/Simulink is implemented to simulate and model the entire system, exhibiting its superior performance in terms of harmonic reduction and grid compliance. The innovative design offers a dependable respond to for integrating renewable energy, ensuring smooth and high-quality power injection into the grid.

Keywords: Inverter; IEEE 519 standards; PD-PWM; renewable energy; THD.

ARTICLE INFORMATION

Author(s): S. Muthukaruppasamy, K. Sarada, Priya R. Patil, and R. Dharmaprakash;

Received: 06/09/2023; **Accepted**: 20/10/2023; **Published**: 30/10/2023;
e-ISSN: 2347-470X;
Paper Id: IJEER 0609-05;
Citation: 10.37391/IJEER.110409
Webpage-link:
https://ijeer.forexjournal.co.in/archive/volume-11/ijeer-110409.html

Publisher's Note: FOREX Publication stays neutral with regard to Jurisdictional claims in Published maps and institutional affiliations.

1. INTRODUCTION

Modern multi-level inverters have become an essential technology for grid integration, electric vehicles (EVs), industrial applications, and renewable energy. Direct current (DC) generated from renewable sources like solar panels or batteries is converted into alternating current (AC), which is suitable for powering a variety of appliances, by inverters. Harmonic distortion and voltage output restrictions on conventional two-level inverters can result in decreased efficiency and added strain on the electrical components. In order to overcome these difficulties, advanced multi-level inverters synthesise the output of AC voltage from multiple levels of DC voltage sources. As a result, they produce output waveforms that are smoother, have a lower harmonic content, and are more efficient, which makes them very desirable for applications that call for high-quality power conversion. Advanced multi-level inverters are essential for improving the grid integration of solar and wind energy in the field of renewable energy. Because they can produce higher output voltages, they no longer need as many step-up transformers, which reduces energy waste and infrastructure expenses. They additionally ensure compliance to stringent grid codes due to their superior harmonic performance, which makes it simpler to seamlessly incorporate clean energy into the power grid [1-3].

Multi-level inverters are gaining popularity due to benefits such as reduced harmonic distortion, improved voltage levels, and improved power quality. Diode-clamped, capacitor-clamped (flying capacitor), and cascaded H-bridge inverters are representations of common types. The neutral point clamped (NPC) inverter, also known as the diode-clamped inverter, produces multiple voltage steps by using diodes to clamp voltages at specific levels. The flying capacitor inverter uses capacitors to produce a range of voltage levels, improving the quality of the waveform. For multi-level voltage output, the cascaded H-bridge inverter incorporates several H-bridge modules [4-7].

Inverters with multiple levels are able to deliver higher voltage levels without having to switch at extremely high frequencies, which reduces switching losses and electromagnetic interference. The pulse width modulation (PWM) control techniques used by multi-level inverters, which guarantee precise control of the output waveform, are one of the key factors enhancing their performance. In this article, various PWM techniques used in multi-level inverter operation are explored. PWM, a control technique, modifies the pulse width of a signal to produce a desired output voltage or current waveform. PWM techniques are essential for producing high-quality output waveforms and reducing harmonic content in multi-level inverters [8-9]. The most fundamental PWM method, known as sinusoidal pulse width modulation (SPWM), aims to create an output voltage waveform that closely resembles a sinusoidal waveform. This is accomplished by contrasting a high-frequency carrier waveform with a reference sinusoidal waveform. A finely controlled output voltage is

FOREX Publication
Open Access | Rapid and quality publishing
International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 11, Issue 4 | Pages 939-943 | e-ISSN: 2347-470X

produced by modulating the carrier waveform's pulse width in accordance with the reference waveform. Although SPWM is relatively simple to implement, voltage distortion at low modulation indices is possible [10-13].

Multi-level inverters may additionally experience increased component stress and power losses. Better harmonic performance and less voltage distortion are made possible by the large number of voltage levels, but power semiconductor devices may be subjected to greater voltage and current stress as a result. This may have an impact on the energy conversion process by increasing switching losses and lowering overall efficiency. The size and cost of the components used in multi-level inverters present another significant obstacle. Voltage changes, harmonics, and grid disturbances have the potential to degrade both the inverter's performance as well as the connected renewable energy sources. Robust control strategies are required to maintain stable operation, lower voltage fluctuations, and provide grid support services like reactive power compensation and voltage regulation. Furthermore, to integrate multi-level inverters with renewable energy systems, sophisticated modelling and simulation techniques are required. Accurate models are needed to predict the inverter's unpredictable behavior under a variety of operating conditions, such as shifting renewable energy production and shifting grid dynamics [14-25].

The following list includes the different objectives for the design and analysis of an advanced multi-level cascading H-bridge inverter system for integrating renewable energy:

- Including the selection of power semiconductor devices, gate drivers, and control schemes, create a thorough design for a five-level cascaded H-bridge inverter system. To achieve precise voltage output levels and reduce switching losses, optimize the modulation method.
- Develop a reliable interface that can effectively manage input power fluctuations while converting the variable DC output of renewable energy sources into stable AC output.
- Perform a thorough analysis of the output waveform of the inverter to determine the THD level. Implement strategies such as PD-PWM to reduce THD and ensure harmonic distortion compliance with grid standards.
- Establish a suitable output filter to lower high-frequency harmonics and enhance the output waveform quality of the inverter. Examine how well the filter provides at reducing undesirable harmonics as well as its effect on affects the stability and performance of the system.
- Analyze extensive simulations to determine the advanced inverter system's overall effectiveness and performance. Examine the system's performance metrics, such as efficiency, output voltage regulation, and harmonic content, in relation to IEEE 519 standards.

2. PROPOSED FIVE LEVEL INVERTER WITH RENEWABLE ENERGY INTEGRATION

Two symmetrical voltage sources and six power switches are used in the five-level multilevel inverter which has been proposed. It facilitates five operating modes, improving the quality of the voltage output. The highest positive output voltage is produced in mode 1 by combining the power of the two sources. One source is used in mode 2 to produce a lower power output. In mode 3, both sources are not interconnected to sources in order to produce a zero output. The second source is inverted in mode 4 to produce a negative mid-level output. The highest negative output power at mode 5, employs two sources. This set up efficiently satisfies a range of load requirements while optimizing voltage levels and quality. The limitation of proposed MLIs is it requires two independent DC voltage sources for producing five levels. As the number of levels increases, requirement of voltage sources also increases, which is not acceptable. *Figure 1* illustrates the PV integrated grid connected system with proposed MLI. *Figure 2* depicts the proposed MLI system. *Figure 3-5* illustrates the various modes of operation.

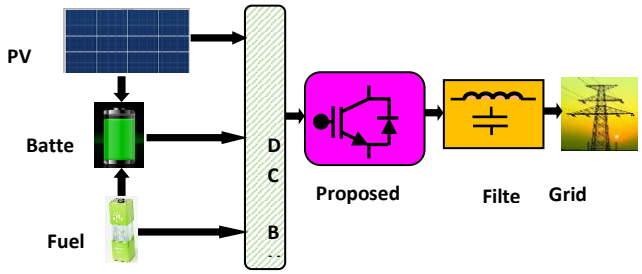

Figure 1: PV integrated grid connected system with proposed MLI

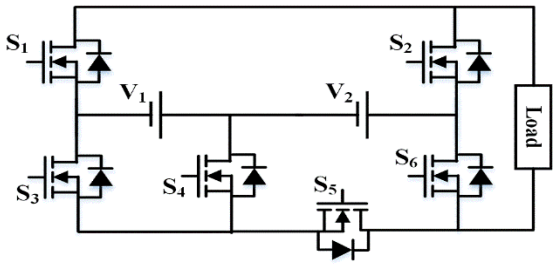

Figure 2: Proposed five level inverter topology

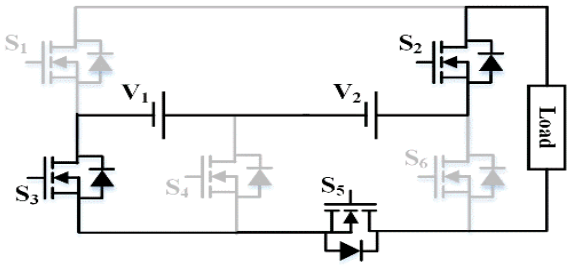

Figure 3: $+2V_{DC}$ output voltage

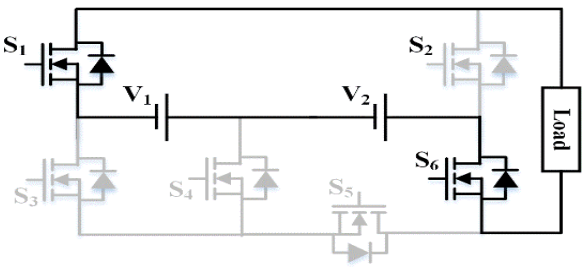

Figure 4: -2VDC output voltage

FOREX Publication
Open Access | Rapid and quality publishing
International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 11, Issue 4 | Pages 939-943 | e-ISSN: 2347-470X

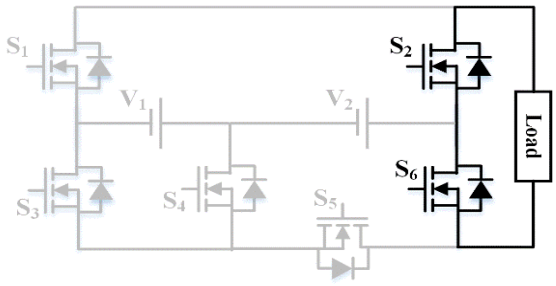

Figure 5: $0V_{DC}$ output voltage

Table 1: Switching logic of proposed MLI

Voltage State	S_1	S_2	S_3	S_4	S_5	S_6
$+2V_{DC}$	0	1	1	0	1	0
$+V_{DC}$	0	1	0	1	1	0
$0V_{DC}$	0	1	0	0	0	1
$-V_{DC}$	1	0	0	1	1	0
$-2V_{DC}$	1	0	0	0	0	1

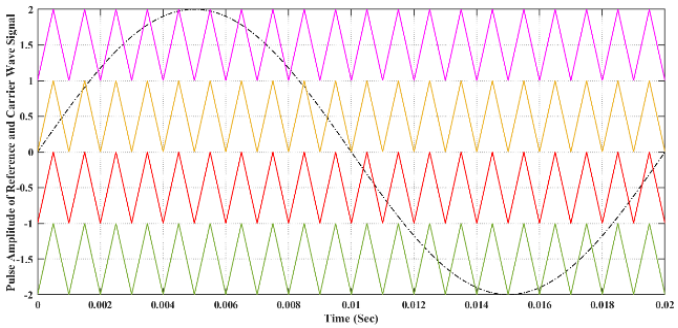

Figure 6: Phase disposition - Pulse width modulation

The proposed five-level multilevel inverter employs a phase disposition pulse width modulation (PWM) technique to control its output. This approach ensures efficient utilization of DC sources and reduces harmonic distortion. In phase disposition PWM, reference and carrier wave signals are compared to generate switching pulses for the inverter's switches. The reference waveform represents the desired output voltage, while the carrier waveform is typically a high-frequency triangular waveform. By modulating the width of the pulses, the inverter produces an output waveform that closely follows the reference signal. This technique enables finer control over the output voltage levels, enhancing the inverter's performance and enabling applications in high-power systems such as renewable energy integration and motor drives. *Figure 6* illustrates the Phase disposition pulse width modulation with sinusoidal reference and triangular carrier wave signal.

3. RESULTS AND DISCUSSION

The proposed five-level multilevel inverter utilizes a symmetrical input voltage of 115 V to generate an output voltage of 230 V at 50 Hz, operating with a high switching frequency of 2650 Hz. This inverter employs advanced pulse-width modulation techniques to synthesize the desired voltage levels, resulting in reduced harmonic distortion and improved voltage quality. To enhance its performance, a filter capacitor and inductor are integrated to mitigate voltage fluctuations and provide smoother output. This configuration enables efficient and precise voltage conversion, making it suitable for various applications requiring high-quality power conversion with minimized harmonic content. *Figure 7* illustrates the five-level staircase output voltage and current for resistive load condition. *Figure 8* depicts the output current and voltage during RL without LC filter. *Table 2* illustrates the various design parameters, which is required to operate lesser THD condition.

Table 2: Proposed MLI design parameters

S. No.	Parameters	Values/Quantity
1.	DC symmetrical voltage source	115 V
2.	Number of DC sources	2
3.	Number power MOSFET switches	6
4.	Switching frequency	2650 Hz
5.	Resistive Load	110 Ω
6.	Filter capacitance	162 µF
7.	Filter inductance	2.2 mH
8.	Voltage output	230V
9.	Current output	10.1 A
10.	Power output	2.323 kW

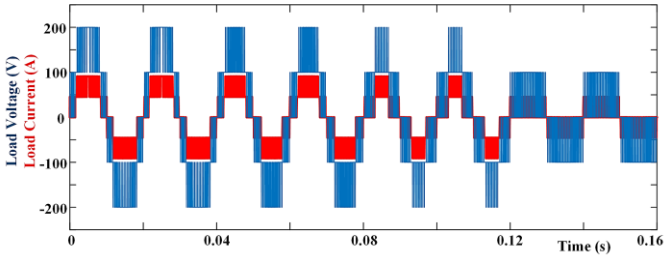

Figure 7: Five level output voltage and current of MLI using R-load

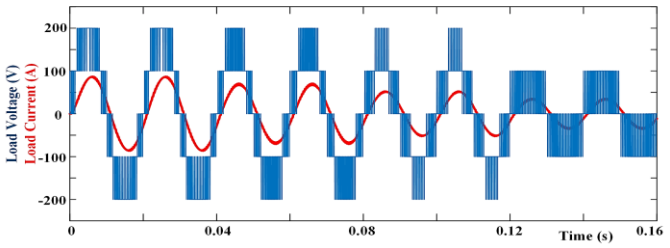

Figure 8: Five level output voltage and current of MLI using RL-load

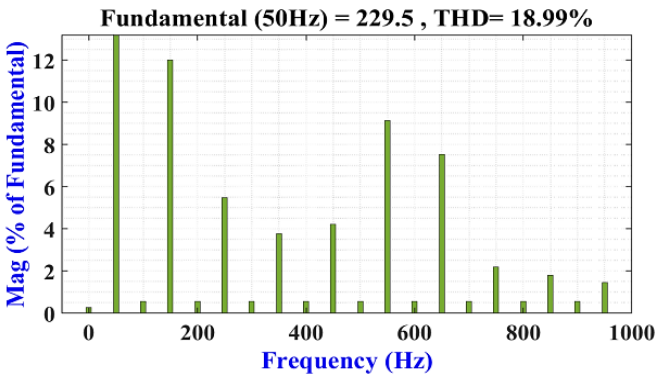

Figure 9: THD analysis of output voltage during R and RL load

FOREX Publication
Open Access | Rapid and quality publishing
International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 11, Issue 4 | Pages 939-943 | e-ISSN: 2347-470X

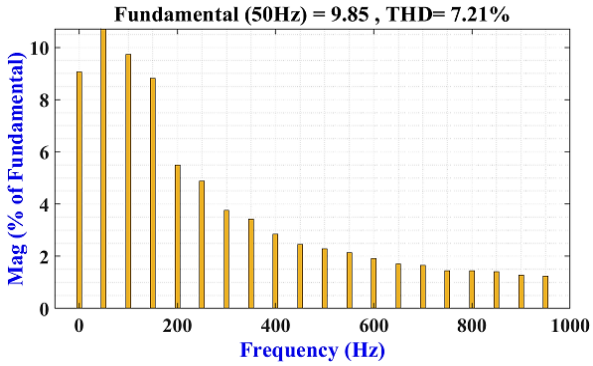

Figure 10: Output current during RL load with LC filter

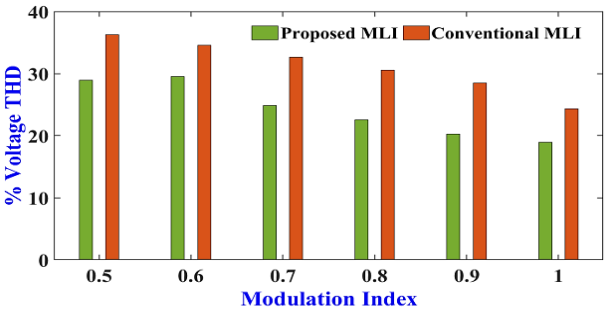

Figure 11: %Voltage THD of proposed and conventional MLI

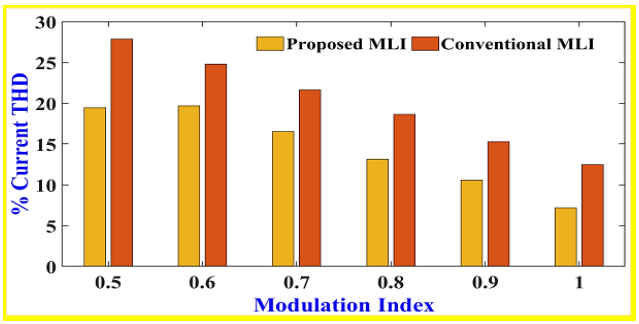

Figure 12: %Current THD of proposed and conventional MLI

THD analysis of output voltage and current under RL load without a filter is shown in *figure 9* and *figure 10* respectively. The THD analysis of the output current under RL load with an LC filter is shown in *figure 11*. The current THD has attained at 1.84% during maximum modulation index. *Figure 11* shows the voltage to harmonic distortion (THD) of the proposed and conventional MLIs, with the proposed MLI having been produced at a lower voltage than the conventional MLI, which consists of eight power switches. Similarly, *figure 12* compares the %current THD of proposed and conventional MLI and also shows that the proposed inverter produces lower THD values. *Table 3* shows the comparison of proposed MLI with existing MLIs in the literature.

Table 3: Comparison of proposed MLI with existing MLIs

Components	Proposed MLI	Classical MLIs			References						
		NPC	FC	CHB	[19]	[22]	[20]	[23]	[21]	[24]	[25]
DC Source	2	1	1	2	2	1	4	1	2	1	2
Capacitors	0	4	10	0	0	2	0	8	0	10	0
Unidirectional switches	6	8	8	8	7	6	20	22	14	18	12
Bidirectional switches	0	0	0	0	2	1	0	0	0	0	0
Driver circuits	6	8	8	8	9	7	20	22	14	18	12
Clamping diodes	0	12	0	0	6	2	0	0	4	0	0

4. CONCLUSION

The integration of maximum power point tracking the proposed five-level multilevel inverter with 6 IGBT power switches and 2 symmetrical voltage sources has demonstrated promising results. Operating at 230 V and 50 Hz, it efficiently generated an output power of 2.32 kW. The achieved low total harmonic distortion (THD) of 1.84% in current during LC filter and 7.12% under RL load conforms to the stringent IEEE 519 standards, ensuring a high-quality output waveform. The control strategy can be improved to achieve even lower THD levels and greater effectiveness. Furthermore, investigating the integration of energy storage systems and renewable energy sources can improve its applicability in contemporary power systems. Overall, the proposed multilevel inverter design shows great promise for safe and dependable power conversion, with room for future developments in power electronics and the incorporation of renewable energy sources. The future scope of this work is to improve the reliability of proposed MLI topology and also apply the space vector PWM techniques for better use of proposed MLI in applications like drives, grid integration of RES etc.

REFERENCES

[1] He, J.; Ye, Y.; Wang, X. ZVS and Inrush Charging Current Suppression Design for Switched-Capacitor Multilevel Inverters. IEEE Transactions on Power Electronics 2023, 38 (9), 10611–10616. https://doi.org/10.1109/tpel.2023.3290570.

[2] Khoun-Jahan, H. Switched Capacitor Based Cascaded Half-Bridge Multilevel Inverter with Voltage Boosting Feature. CPSS Transactions on Power Electronics and Applications2021, 6 (1), 63–73. https://doi.org/10.24295/cpsstpea.2021.00006.

[3] Suresh, K.; Parimalasundar, E. Fault Analysis and Clearance in FL-APC DC–AC Converter. IEEE Canadian Journal of Electrical and Computer Engineering2023, 46 (1), 1–6. https://doi.org/10.1109/icjece.2022.3220090.

International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 11, Issue 4 | Pages 939-943 | e-ISSN: 2347-470X

[4] Tak, N.; Chattopadhyay, S. K.; Chakraborty, C. Single-Sourced Double-Stage Multilevel Inverter for Grid-Connected Solar PV Systems. IEEE Open Journal of the Industrial Electronics Society2022, 3, 561–581. https://doi.org/10.1109/ojies.2022.3206352.

[5] Suresh, K.; Parimalasundar, E.; Sujatha, M. S.; Kumar, N. M. G. Design and Implementation Bidirectional DC–AC Converter for Energy Storage System. IEEE Canadian Journal of Electrical and Computer Engineering2023, 46 (2), 130–136. https://doi.org/10.1109/icjece.2022.3233840.

[6] Han, D.; Peng, F. Z.; Dwari, S. A Multilevel Active CM Noise Power Filter for Multilevel Inverters. IEEE Transactions on Industrial Electronics2023, 70 (6), 5454–5462. https://doi.org/10.1109/tie.2022.3194586.

[7] Rahman, S.; Meraj, M.; Iqbal, A.; Ben-Brahim, L.; Abu-Rub, H.; Khan, I. Novel Level-Shifted PWM Technique for Cascaded Multilevel Quasi-Impedance Source Inverter. IEEE Journal of Emerging and Selected Topics in Power Electronics 2021, 9 (5), 5918–5928. https://doi.org/10.1109/jestpe.2021.3096844.

[8] Sarebanzadeh, M.; Hosseinzadeh, M. A.; Garcia, C.; Babaei, E.; Islam, S.; Rodriguez, J. Reduced Switch Multilevel Inverter Topologies for Renewable Energy Sources. IEEE Access2021, 9, 120580–120595. https://doi.org/10.1109/access.2021.3105832.

[9] Suresh, K.; Parimalasundar, E. Newly Designed Single-stage Dual Leg DC-DC/AC Buck-boost Converter for Grid Connected Solar System. International Journal of Circuit Theory and Applications2023. https://doi.org/10.1002/cta.3709.

[10] Akbari, A.; Ebrahimi, J.; Jafarian, Y.; Bakhshai, A. A Multilevel Inverter Topology with an Improved Reliability and a Reduced Number of Components. IEEE Journal of Emerging and Selected Topics in Power Electronics 2022, 10 (1), 553–563. https://doi.org/10.1109/jestpe.2021.3089867.

[11] Suresh, K.; Parimalasundar, E. ITBC Controlled IPWM for Solar Based Wide Range Voltage Conversion System. IETE Journal of Research2023, 1–9. https://doi.org/10.1080/03772063.2023.2217788.

[12] Kumar, B. H.; Janardhan, K.; Kumar, R. S.; Rahul, J. R.; Singh, A. R.; Naidoo, R.; Bansal, R. C. An Enhanced Space Vector PWM Strategies for Three Phase Asymmetric Multilevel Inverter. International Transactions on Electrical Energy Systems2023, 1–21. https://doi.org/10.1155/2023/5548828.

[13] Al-Hitmi, M. A.; Hussan, Md. R.; Iqbal, A.; Islam, S. Symmetric and Asymmetric Multilevel Inverter Topologies with Reduced Device Count. IEEE Access2023, 11, 5231–5245. https://doi.org/10.1109/access.2022.3229087.

[14] Jena, K.; Kumar, D.; Janardhan, K.; Kumar, B. H.; Singh, A. R.; Nikolovski, S.; Bajaj, M. A Novel Three-Phase Switched-Capacitor Five-Level Multilevel Inverter with Reduced Components and Self-Balancing Ability. Applied Sciences2023, 13 (3), 1713. https://doi.org/10.3390/app13031713.

[15] Liu, Y.; Liu, C.; Gao, X.; Liu, S. Design and Control of a Decoupled Multichannel Wireless Power Transfer System Based on Multilevel Inverters. IEEE Transactions on Power Electronics2022, 37 (8), 10045–10060. https://doi.org/10.1109/tpel.2022.3159129.

[16] Hosseinzadeh, M. A.; Sarebanzadeh, M.; Garcia, C. F.; Babaei, E.; Rodriguez, J. An Asymmetric Switched-Capacitor Multicell Inverter with Low Number of DC Source and Voltage Stress for Renewable Energy Sources. IEEE Access2022, 10, 30513–30525. https://doi.org/10.1109/access.2022.3140786.

[17] B. H. Kumar, M. M. Lokhande, An enhanced space vector PWM for nine-level inverter employing single voltage source. IEEE Transportation Electrification Conference (ITEC-India). 1-6 (2017) doi: 10.1109/ITEC-India.2017.8333711.

[18] Jena, K.; Kumar, D.; Kumar, B. H.; Janardhan, K.; Singh, A. R.; Naidoo, R.; Bansal, R. C. A Single DC Source Generalized Switched Capacitors Multilevel Inverter with Minimal Component Count. International Transactions on Electrical Energy Systems2023, 1–12. https://doi.org/10.1155/2023/3945160.

[19] R. A. Madhukar and K. Sivakumar, "A Fault-Tolerant Single-Phase Five-Level Inverter for Grid-Independent PV Systems," IEEE Trans. Ind. Electron., vol. 62, no. 12, pp. 7569-7577, Dec. 2015.

[20] J. Nicolas-Apruzzese, S. Busquets-Monge, J. Bordonau, et al., "Analysis of the fault-tolerance capacity of the multilevel active-clamped converter,"IEEE Trans. Ind. Electron., 60, (11),pp. 4773–4783, 2013.

[21] M. Aly, E. M. Ahmed and M. Shoyama, "A New Single-Phase Five-Level Inverter Topology for Single and Multiple Switches Fault Tolerance," IEEE Trans on Power Electron., vol. 33, no.11, pp. 9198-9208, Nov. 2018.

[22] S.P. Gautam, S. Gupta, L. Kumar, "Reliability improvement of transistor clamped H bridge- based cascaded multilevel inverter,"IET Power Electron., 10, (7), pp. 770–781, 2017.

[23] A. Chen, L. Hu, L. Chen, et al., "A multilevel converter topology with fault-tolerant ability, IEEE Trans. Power Electron.,"vol. 20, no. 2, pp. 405–415, 2005.

[24] A. Ghazanfari and Y. A. I. Mohamed, "A Resilient Framework for Fault-Tolerant Operation of Modular Multilevel Converters," IEEE Transactions on Industrial Electronics, vol. 63, no. 5, pp. 2669-2678, May 2016.

[25] H. K. Jahan, F. Panahandeh, M. Abapour and S. Tohidi, "Reconfigurable Multilevel Inverter with FaultTolerant Ability," IEEE Transactions on Power Electronics, vol. 33, no. 9, pp. 7880-7893, Sept. 2018.