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International Journal of
Electrical and Electronics Research (IJEER)
Research Article | Volume 12, Issue 1 | Pages 12-19 | e-ISSN: 2347-470X

Design and Analysis of Ultra-low Power Voltage Controlled Oscillator in Nanoscale Technologies

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ABSTRACT- In latest wired and wireless communication equipment, VCO (voltage-controlled oscillator) is the major building block and particularly used as the stable high frequency clock generator. VCO performance is measured through frequency range, power supply used, area occupied, power consumption, delay, and phase noise. VCO is the cascaded of odd number of inverter stages in a ring format, hence it is also articulated as a ring oscillator. Today's portable communication devices are battery operated. Hence, low power and area efficient designs play a key role in battery life enhancement and device size reduction. Device scaling improves the effective silicon area utilization, but it leads to more leakages. Therefore, low power techniques along with the technology scaling is the best way of low power designs. In this article, discussed various low power schemes. The ring oscillator designs are carried out in various nano meter scaled technologies such as 180nm, 90nm,65nm and 45nm. A 5-stage ring oscillator is implemented in each technology along with low power schemes, simulated in Cadence virtuoso, and noted power, delay, and area. Observed that the proposed ring oscillator with sleepy keeper technique generated a stable frequency of oscillations in the range of 1GHz-2GHz. A control voltage of 1.8V to 0.4V is applied and targeted the power less than 30mW and delay in 0.25p sec.

Keywords: Ring oscillator VCO, CMOS inverter, low power schemes, PLL.

ARTICLE INFORMATION
Author(s): Priyaka Kumara B.S and Dr. Sobhit Saxena;
Received: 21/09/2023; **Accepted**: 01/12/2023; **Published**: 15/01/2024;
e-ISSN: 2347-470X;
Paper Id: IJEER 2109-15
Citation: 10.37391/IJEER.120103
Webpage-link:
https://ijeer.forexjournal.co.in/archive/volume-12/ijeer-120103.html

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1. INTRODUCTION

From past few decades, the advancements in modern wireless communication equipment, demands a robust and low-power communication systems along with long battery life. This need increases exponentially, as they have significant components, such as VCOs and phase locked loops (PLLs) and have a wide variety of applications in the electronic field. Therefore, significant research has been conducted over the decades to satisfy the requirement. VCO is the major block used to provide a local frequency signal to the PLL in the communication equipment, and PLL is equipped in frequency synthesizer circuits and clock recovery circuits used to bringing the synchronization between the signals. From this scenario, it's understood that the VCO design has a significant importance in the PLL circuits. VCO circuits can be designed with different electrical and electronic components, based on the components used and the applications they are named LC oscillator, ring oscillator and relaxation oscillator. Typically, LC oscillator provides better phase noise, higher frequency of oscillations at the cost of small frequency tuning range and complex fabrication process of inductors and capacitor on the silicon area. Unlike LC oscillators, the ring oscillators provide an ease of fabrication on silicon and wide frequency tuning range [1]. Oscillator circuit is evaluated based on the different metrics, such as operating frequency, range coverage, power consumption, pushing and phase noise. The figure of merit (FOM) is another factor to compare the performance of same kind of architecture oscillators, its formula is given by the *equation (1)*.

$$FOM = 10\log\left(\frac{F_0}{\Delta F}\right)^2\left[\frac{1}{V_{DD}*I*PN}\right] \quad (1)$$

Where, F_0-center frequency, ΔF-frequency offset, V_{DD}-supply voltage, I-current, PN-phase noise.

When compared to the LC oscillators, ring oscillators have low FOM as they consume more power, and worse phase noise for the same frequency. Generally, current starved ring oscillators provide high tuning range, less area and low phase noise than the traditional ring oscillators [2]. An Oscillator is an electronic circuit, which produces a periodic signal with the internal noise and does not use the input signal. Basically, Oscillator has positive feedback or direct feedback from the output to the input to have in phase between output and input signals. The forward path is usually an amplifier with an amplification factor of 'A', and the feedback path has a feedback components with frequency dependent attenuation factor is 'β(jω)'. An oscillator is responsible for producing a sustained (neither increasing nor decreasing its amplitude) frequency of oscillations at a particular frequency or within the range of frequencies. For this,

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Barkhausen's criterion should meet such as magnitude and phase conditions.

Magnitude criterion: Must meet a specific magnitude criterion to avoid divergent or damped oscillations (no global amplification or attenuation per each loop cycle). If there is a positive amplitude ($|T(j\omega_o)|>1$), then the condition holds.

Phase criterion: $\angle T(j\omega_0)$ must equal 00 or 3600 for a phase to be in effect. If the phase criterion is not satisfied, the oscillations will either decline or increase soon after the power is turned on. $T(j\omega) = |A\beta(j\omega)| \approx 1$ is the oscillator's overall loop gain. The only method to ensure that the system oscillates at a frequency where the phase requirement is satisfied is to permit self-excitation through positive feedback. The frequency (ω_o) at which the amplitude criteria are met by design sometimes differs from this frequency. As a result, the system would want to oscillate at a different frequency (say ω_1). Assuming the amplitude requirement holds at the higher frequency ω_1, oscillations would exhibit increasing amplitude (without a limiting mechanism). However, we will get damped oscillations if the loop gain magnitude is <1 at frequency ω_1. In this case, Barkhausen's criteria would only be appropriate for steady-state oscillations. In this technique, a sinusoidal signal may travel the whole feedback loop length without losing any amplitude or changing its phase.

VCO used in communication equipment is a cascaded connection of odd or even number of CMOS inverter stage in a ring fashion as in *figure 1(a)*. In the cascading connection, output of the previous stage inverter is the input for the next stage of inverter, and the last stage output is feedbacked and connected as the input to the first stage inverter. Ring type connection has few benefits like ease of implementation, wide frequency range with low control voltage. In the ring oscillator, each stage would be considered as a delay element.

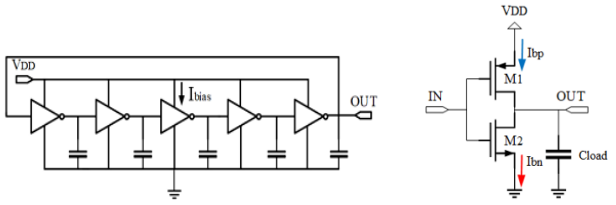

Figure 1: (a) Ring oscillator (b) CMOS inverter

Each inverter in the ring oscillator, has one PMOS and one NMOS devices as in *figure 1(b)*, when the input voltage level Vin=0, the PMOS device will turn ON and the NMOS will turn OFF, therefor the current drawn from VDD and flows to the output node via the PMOS device. Similarly, when the input signal Vin=1, the PMOS will turn OFF and the NMOS will turn ON. Now the current flows from the output node to ground via NMOS device. In the CMOS inverter, both the devices should work in the saturation region, and the conditions for the devices to be in the saturation are VGS>VTH and VDS>(VGS-VTH). 'VGS' is the gate source voltage of the device, 'VTH' is the device threshold voltage of the device, and 'VDS' is the drain to source voltage of the transistor. When the devices are in the saturation, each device have certain amount of ON resistance and the parasitic capacitances, thereby each inverter stage in the ring oscillator results significant amount of propagation delay (τ_d), which is define as the sum of both rise time and fall time delaysand represented in the *equations (1) and (2).*

The rise delay, $\tau_{rise}=\tau_{dHL}=\ln(2)R_{non}C_{load}$, (2)

The fall time delay,$\tau_{fall}=\tau_{dLH}=\ln(2)R_{pon}C_{load}$ (3)

WhereR_{non} and R_{pon} are the NMOS and PMOS transistors ON resistance respectively. And C_{load} is the load capacitance of each inverter stage.Therefore $\tau_d=(\tau_{dHL}+\tau_{dLH})/2$ and frequency of oscillations $f_{osc}=\frac{1}{2\tau_d}$ and, for N inverter stages, the frequency of oscillations $f_{osc}=\frac{1}{2N\tau_d}$. Where τ_d is the time delay of single inverter stage.τ_d can be calculated as the time constant of RC low pass filter (LPF). Delay and frequency of oscillations expressed in terms of the bias or control current, amplitude of oscillations and parasitic capacitances is presented in *equations (4) and (5).*

$$\tau_d = \frac{V_{osc}*C_G}{I_{cont}} \quad (4)$$

$$f_{osc} = \frac{I_{cont}}{2N*V_{osc}*C_G} \quad (5)$$

Where,
V_{osc} – amplitude of oscillations, C_G – paracitic capacitance of P&N MOS devices, I_{cont} – control current.

In this paper, introduction on ring oscillator is discussed in the introduction part. Literature is presented in the existing work part. The recent developments and modified circuits and techniques applied to the ring oscillator are presented in the proposed work chapter. The results and the discussions are presented in results and discussions topic. Finally, concussions on the designs presented in the conclusions chapter.

2. EXISTING WORK

For 180nm and the above technology, the dynamic power contributes major power share in the chip power, whereas below 180nm technology, the static power component dominates the dynamic power component share. Subthreshold leakage or current contributes major share to the static power dissipation. Subthreshold leakage is due to the current flows from drain to source when $V_{GS}<V_{TH}$ [18]. This current has exponential relation to the device threshold voltage. Device threshold voltage scaling makes rapid subthreshold current increase in nano scaled devices. Hence, in lower technology nodes, the subthreshold leakage should be minimized thereby improving the device performance. A few techniques were proposed and discussed in the literature to curtail static power such as stack approach, sleep transistor approach, sleepy stack approach and zigzag approach. Each low power technique has its own merits and demerits [17].

The basic inverter shown in *figure 2(a)* has PMOS and NMOS transistors widths are Wp=2 and Wn=1respectively. In the stack

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approach, each transistor is replaced with two transistors of the same kind. The width of each transistor is half of the original transistor as shown in *figure 2(b)*. Sleep transistor technique is another way to reduce the leakage power, here, sleep transistors between the pullup device and V_{DD}, and between the pulldown device and GND as shown in *figure 2(c)*. In conventional CMOS inverter, PMOS is connected to V_{DD} and NMOS is connected to GND always. To maintain logic-1 in sleep mode, the sleepy keeper approach has been used. The sleep transistors are either high V_{TH} type or low V_{TH} type [2]. These sleep transistors help in isolating the pullup or pulldown or both the devices from V_{DD} or GND. Sleep transistor will turn OFF when the circuit is not in use i.e in the sleep mode. This technique is also known as gated V_{DD} or (multi threshold CMOS) MTCMOS or gated GND techniques. Few setbacks were reported with this technique, the sleep devices incur area and delay overheads, and both pullup and pulldown networks would have floating values, hence loses the state in the sleep mode. These floating values will show impact on the wakeup and energy of the sleep transistors. By mixing the forced stack and the sleep transistor techniques shown in the *fig.2(d)*, a new circuit results, called sleepy stack technique. Consider a stack technique with the W/L =3 for PMOS and W/L =1.5 for NMOS as in the stack approach. A high V_{TH} PMOS sleep transistor with W/L =3 connects in parallel with one of the devices in stacked PMOS, similarly high V_{TH} NMOS sleep with W/L =1.5 is connected in parallel with one of the devices in stacked NMOS as in the fig and, maintain equivalent input capacitance. Sleep transistor role is same as the role in the sleep transistor approach. *i.e.* during the active mode, they are ON and during sleep mode, they are OFF. Here, the switching speed has been improved compared to the switching speed in the stack method, since during the active mode, the sleep devices are always ON, hence the voltage value at the drain of each sleep transistor is connected to its source, and always available. Therefore, the low-VTH transistor linked to the gate output receives current flow instantly independent of the states of the other transistors in parallel with the sleep transistor. These two effects work together to allow the sleepy stack structure to maintain the identical logic state while using minimal leakage power during sleep mode. The cost of this is expanded floor space [3].

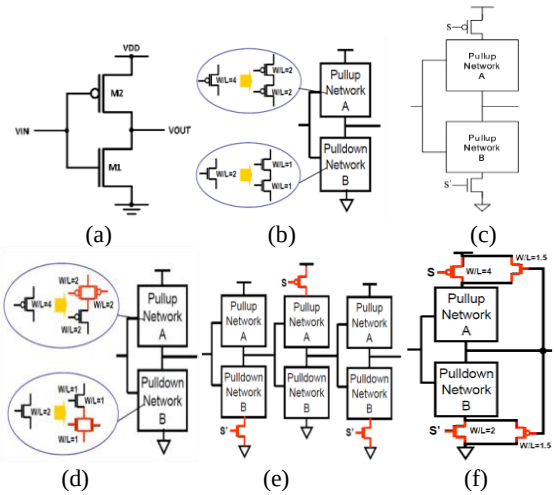

Figure 2: a) Basic b) Stack approach c) Sleepy transistor d) sleepy stack e) Zigzag technique f) Sleepy keeper

Zigzag is another low-power method made to reduce the cost of waking time in the sleep transistor technique that came before it. One logic circuit comprises two steps, as shown in *figure 2(e)* choose a specific circuit state. To choose a condition for the circuit, turn OFF the pull-down network for each gate whose output is high and turn ON the pull-up network for each gate whose result is low. When the output logic is 1, a pull-down sleep transistor is used. If the output value is 0, a pull-up sleep transistor is used. The result can help stop the floating state problem, but only sometimes [4]. Two changes have been made to the sleep transistor circuit in *figure 2(c)* to lower the transmission delay and keep the logic states. As shown in Fig. 2(f), a W/L=1.5 connected NMOS keeper transistor in parallel to a PMOS sleep transistor, and a W/L=1.5 PMOS keeper device is connected parallel to the NMOS sleep transistor. In sleep mode, the NMOS device is linked to VDD to keep the output at logic 1, and NMOS is the only source of VDD to pull up the network when turned off the sleep transistor. During active mode, PMOS is the only way to connect the network to the ground when turned on the sleep transistors. In the same way, the sleepy keeper method uses this '0' number and connects PMOS to GND to keep logic 0 in sleep mode. When sleep transistors are present, the resistance of the ON line goes up, which makes the transmission delay shorter. This method is used to keep the circuit's logic state.

3. PROPOSED WORK

In the field of wire/wireless communication, the VCO is used widely as PLL and frequency synthesizer. A good VCO would have low power, low phase noise, less delay of each stage, low jitter, and wide range of frequency. Odd number of inverter stages are connected as delay buffer chain and made inversion only occurs one time between the final stage to the input. The earlier ring oscillator designs reported high power consumption, and temperature dependency of frequency of oscillations. In the ring oscillator, when the number of stages increases, the frequency of oscillations decreases because both are inversely related, and delay of the single stage is multiplied with this. Hence, the best way to increase the frequency is to reduce the delay associated with each stage. To reduce the delay of each stage, bios currents of transistors are used to control the propagation delay of each delay unit. Similarly, to lower the overall power consumption of the ring oscillator, sleepy stack approach combined bias current control network. PMOS and NMOS devices in the inverter circuits are operated either in the subthreshold region or in the strong inversion region. If they are operating in the strong inversion region, the current in each stage reduces with the temperature, hence 'f_{osc}' value will decrease [6]. When they are operating in subthreshold region, the current in each stage increases and thereby 'f_{osc}' value increases. We don't want all high or low oscillations at same frequency, the negative feedback should become at a specific frequency, ω_0. Common source amplifier with dominant pole, neglect all parasitic [7]. The stages are identical from each other because gate input impedance of MOS FET is infinite. Stacked approach inverter has been used in the five-stage ring oscillator design, used gpdk 90nm CMOS technology and supply voltage

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of 1.8V applied to achieve low power of 27.36uW [14]. A 9-stage ring oscillator designed with gpdk 90nm technology to generate 2GHz frequency [15]. A 5-stage ring oscillator is designed with different low power techniques mentioned above.

With each technic a five-stage ring oscillator has been implemented in 180nm, 90nm, 65nm and 45nm technology nodes, then each is simulated and measured different performance matrices such as static and dynamic powers, delay, and area.

Design: The design specifications are frequency (1GHz to 2GHz), supply voltage (1.8V to 0.4V), and power consumption < 30mW. Consider the basic inverter shown in *fig.1(b)*, where source current (I_{bp}) *via* PMOS and sink current (I_{bn}) via NMOS are balanced when both are ON and made equal. This is done by proper sizing of the inverter components.

$$I_{bn} = I_{bp}$$
$$k_n(V_{GS} - V_{THn})^2 = k_p\left(V_{SG} - V_{THp}\right)^2 \quad (5)$$

$V_{SG} = V_{DD} - V_1 \& V_{GS} = V_1$ where V_1 is the triggering voltage of the inverter,V_{SG}source gate voltage.

$$k_n(V_1 - V_{THn})^2 = k_p\left(V_{DD} - V_1 - V_{THp}\right)^2$$

$$(V_1 - V_{THn})^2 = \frac{k_p}{k_n}\left(V_{DD} - V_1 - V_{THp}\right)^2$$

$$V_1 = \frac{\sqrt{\frac{k_p}{k_n}}(V_{DD} - V_{THp}) + V_{THn}}{\left(\sqrt{\frac{k_p}{k_n}} + 1\right)} \quad (6)$$

After substitution and simplification, the NMOS device size is given in *equation (7)*

$$\frac{W}{L} = \frac{C_l}{\tau_d \mu_n C_{ox}(V_{DD} - V_{THn})}\left[\frac{2V_{Th}}{V_{DD} - V_{THn}} + ln\left(\frac{4(V_{DD} - V_{THn})}{V_{DD}}\right) - 1\right] (7)$$

With the bias currents in the inverter, the rise and fall delays in the *equations (2) & (3)* are modified and presented in *equations (8) and (9)*

$$\tau_{rise} = \tau_{dHL} = \frac{C_{eff}(V_{DD} - V_1)}{I_{bn}} \quad (8)$$

$$\tau_{fall} = \tau_{dLH} = \frac{C_{eff} V_1}{I_{bp}} \quad (9)$$

Where C_{eff} is the effective capacitance, including parasiticcapacitance (C_G) of the inverter shown in *equation (4)*, in series with load capacitance (C_l). Assuming that $I_{bn} = I_{bp} = I_{cont}$. After substitution all these in *equations (8) and (9)*, the *equation (5)* is written as

$$f_{osc} = \frac{I_{cont}}{N * V_{DD} * C_{eff}} \quad (10)$$

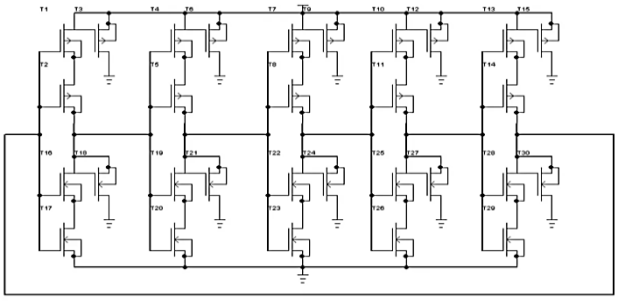

Figure 3: A 5-stage sleepy keeper RO

A 5-stage RO with sleepy keeper approach-bias current is shown in *fig.3*, and the schematic is presented in *fig.4*. Inverting stage produces 180^0 phase shift, to make 360^0 phase shifts from output to input, a phase lead or phase lag network should be placed in the feedback path. The choosing of resistor value is based on the condition that the input impedance of a network must be large in comparison to the output impedance of the inverter amplifier stage [19-21].

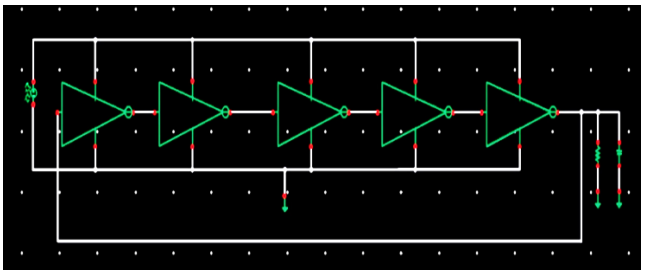

Figure 4: A 5-stage sleepy keeper RO

Not to load the output significantly, which would reduce the amplifier stage gain. The resistance of the RC network should be chosen to a value of 10K ohms, since the amplifier output impedance is in the range of 50K ohms. For an RC network, $f = \frac{1}{2\pi RC}$. And for 2GHz frequency, the value of is assumed to choose R=10KΩ. Then the value of $C = \frac{1}{2\pi Rf} = 31.4fF$. From equations (4) and (5), $\tau_{dHL} + \tau_{dLH} = 0.7(R_{non} + R_{pon})C_l$ ---- (11), $C_{oxn} = 0.625fF$ and $C_{oxp} = 1.25fF$. $R_{non} = 3.4K\Omega$ and $R_{nop} = 3.4K\Omega$, for five stages, N=5 and the $C_l = \frac{N}{2(C_{oxn} + C_{oxp})} = 1.33fF$. Then substitute the values in equation 5, $\tau_{dHL} + \tau_{dLH} = 0.7(3.4K + 3.4K)1.33f$ =6.33psec. For five stages, $f_{osc} = \frac{1}{2*5*6.33} = 15.7GHz$. From simulations, total delay, $\tau_d = \tau_1 + \tau_2 + \tau_3 + \tau_4 + \tau_5 = 1.91 + 2.12 + 2.89 + 3.75 + 4.91$.

4. RESULT AND DISCUSSION

A 5-stage RO is implemented in180 nm technology node long with different low power techniques, and the simulation results are presented in *table 1*. At this node, both SK dVth technique and sleepy keeper techniques produced better results in all aspects when compared with other techniques.

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Table 1: 180nm technology 5-stage ROs Results

180nm	Delay (S)	Static power (W)	Dynamic power (W)	Area (μm²)
Base Case	$7.18E^{-11}$	$5.01E^{-09}$	$1.56E^{-05}$	$3.25E^{+02}$
Stack	$2.08E^{-10}$	$3.43E^{-10}$	$1.21E^{-05}$	$1.12E^{+03}$
Sleep	$1.18E^{-10}$	$8.63E^{-10}$	$1.61E^{-05}$	$1.02E^{+03}$
Zigzag	$7.34E^{-11}$	$1.00E^{-09}$	$1.58E^{-05}$	$7.40E^{+02}$
Sleepy Stack	$1.45E^{-10}$	$6.01E^{-10}$	$1.18E^{-05}$	$1.96E^{+03}$
Sleepy Keeper	$1.58E^{-10}$	$3.51E^{-10}$	$1.07E^{-05}$	$1.74E^{+03}$
Sleep dVth	$1.44E^{-10}$	$1.42E^{-12}$	$1.66E^{-06}$	$1.02E^{+03}$
Zigzag dVth	$7.35E^{-11}$	$4.49E^{-13}$	$1.59E^{-05}$	$7.40E^{+02}$
SS dVth	$1.65E^{-10}$	$7.95E^{-14}$	$1.15E^{-05}$	$1.96E^{+03}$
SK dVth	$1.94E^{-10}$	$3.62E^{-12}$	$1.10E^{-05}$	$1.74E^{+03}$

A 5-stage RO is implemented in 90nm technology node along with different low power techniques, and the simulation results are presented in *table 2*. At this node, both SK dVth technique and sleepy keeper techniques produced better results in all aspects when compared with other techniques.

Table 2: 90 nm technology 5-stage ROs Results

90nm	Delay (S)	Static power (W)	Dynamic power (W)	Area μm²)
Base Case	$6.6E^{-11}$	$4.46E^{-09}$	$1.42E^{-06}$	$8.94E^{+01}$
Stack	$1.9E^{-10}$	$2.37E^{-10}$	$1.22E^{-06}$	$3.09E^{+02}$
Sleep	$1.09E^{-10}$	$5.71E^{-10}$	$1.51E^{-06}$	$2.82E^{+02}$
Zigzag	$6.69E^{-11}$	$6.92E^{-10}$	$1.48E^{-06}$	$2.03E^{+02}$
Sleepy Stack	$1.32E^{-10}$	$4.25E^{-10}$	$1.09E^{-06}$	$5.39E^{+02}$
Sleepy Keeper	$1.42E^{-10}$	$2.50E^{-10}$	$1.00E^{-06}$	$4.78E^{+02}$
Sleep dVth	$1.60E^{-10}$	$5.61E^{-13}$	$1.56E^{-06}$	$2.82E^{+02}$
Zigzag dVth	$6.81E^{-11}$	$6.28E^{-13}$	$1.48E^{-06}$	$2.03E^{+02}$
SS dVth	$1.85E^{-10}$	$1.01E^{-12}$	$1.10E^{-06}$	$5.39E^{+02}$
SK dVth	$2.11E^{-10}$	$1.56E^{-12}$	$1.04E^{-06}$	$4.74E^{+02}$

A 5-stage RO with different low power techniques is implemented with 65nm technology node, and the simulation results are presented in *table 3*. At this node, both SK dVth technique and sleepy keeper techniques produced better results in all aspects when compared with other techniques.

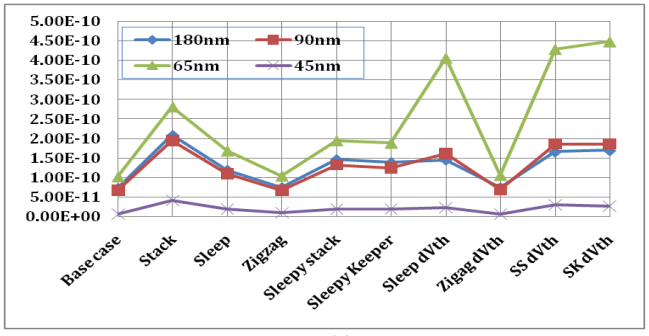
Table 3: 65nm technology 5-stage ROs Results

65nm	Delay (S)	Static power (W)	Dynamic power (W)	Area (μm²)
Base Case	$1.9E^{-10}$	$1.82E^{-08}$	$8.68E^{-07}$	$4.66E^{+01}$
Stack	$2.8E^{-10}$	$2.51E^{-09}$	$7.29E^{-07}$	$1.61E^{+02}$
Sleep	$1.68E^{-10}$	$7.07E^{-09}$	$9.32E^{-07}$	$1.47E^{+02}$
Zigzag	$1.03E^{-10}$	$6.58E^{-09}$	$8.89E^{-07}$	$1.06E^{+02}$
Sleepy Stack	$1.94E^{-10}$	$3.91E^{-09}$	$6.21E^{-07}$	$2.81E^{+02}$
Sleepy Keeper	$2.07E^{-10}$	$2.98E^{-09}$	$5.62E^{-07}$	$2.49E^{+02}$
Sleep dVth	$4.05E^{-10}$	$2.90E^{-11}$	$9.99E^{-07}$	$1.47E^{+02}$
Zigzag dVth	$1.05E^{-10}$	$7.67E^{-11}$	$9.34E^{-07}$	$1.06E^{+02}$
SS dVth	$4.28E^{-10}$	$3.42E^{-11}$	$6.46E^{-07}$	$2.81E^{+02}$
SK dVth	$4.98E^{-10}$	$8.64E^{-10}$	$6.02E^{-07}$	$2.49E^{+02}$

From the simulation results presented in *table 1* to *table 5* and the corresponding graphs are shown in *figure 5(a)* to *figure 5(e)*. From these it is observed that at 180nm node, the amount of static power is less compared with the other nodes. At 65nm node, dynamic power is less compared to other nodes and finally it is observed that at 45nm both delay and area of the designs decreased compared to others.

Table 4: 45nm technology 5-stage ROs Results

45nm	Delay (S)	Static power (W)	Dynamic power (W)	Area (μm²)
Base Case	$6.57E^{-12}$	$1.01E^{-06}$	$1.27E^{-06}$	$2.28E^{+01}$
Stack	$4.15E^{-11}$	$1.52E^{-07}$	$2.73E^{-07}$	$7.73E^{+01}$
Sleep	$1.95E^{-11}$	$3.94E^{-07}$	$1.25E^{-06}$	$7.05E^{+01}$
Zigzag	$9.74E^{-12}$	$3.92E^{-07}$	$1.27E^{-06}$	$5.09E^{+01}$
Sleepy Stack	$1.98E^{-11}$	$2.32E^{-07}$	$6.07E^{-07}$	$1.34E^{+02}$
Sleepy Keeper	$2.00E^{-11}$	$1.65E^{-07}$	$5.96E^{-07}$	$1.97E^{+02}$
Sleep dVth	$2.26E^{-11}$	$8.65E^{-09}$	$1.24E^{-06}$	$7.05E^{+01}$
Zigzag dVth	$7.18E^{-12}$	$1.20E^{-08}$	$1.25E^{-06}$	$5.09E^{+01}$
SS dVth	$3.07E^{-11}$	$1.02E^{-08}$	$5.84E^{-07}$	$1.34E^{+02}$
SK dVth	$3.10E^{-11}$	$7.41E^{-09}$	$5.87E^{-07}$	$1.19E^{+02}$



(a)

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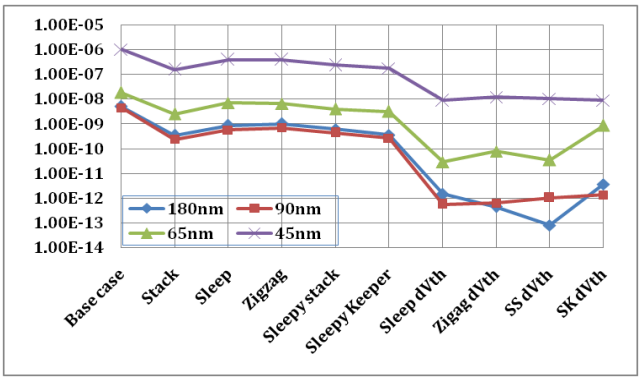
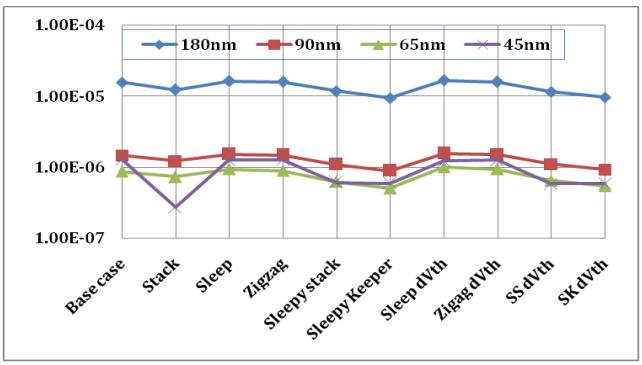
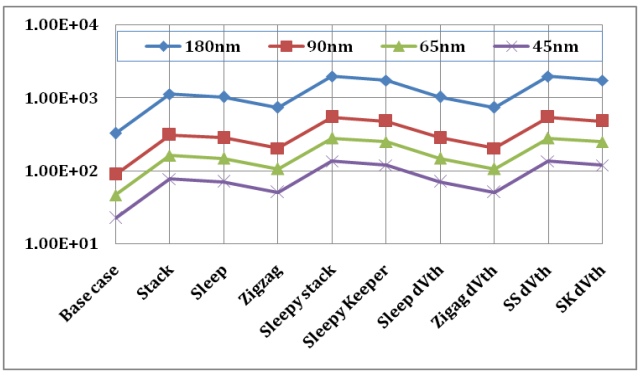


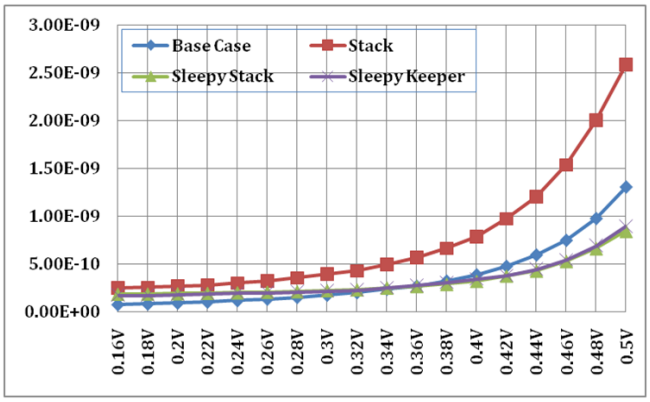
(b)



(c)



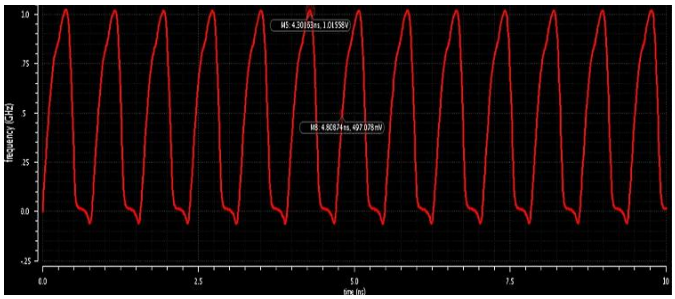
(d)



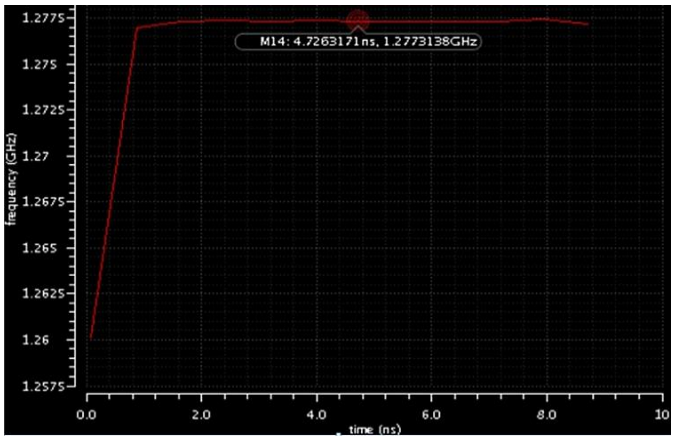
(e)

Figure 5: Comparison results of different 5-stage ROs implemented with different technology nodes (a) delay comparisons (b) static power comparisons (c) dynamic power comparisons (d) are comparisons (e) overall Comparisons

A 5-stage ROs implemented with various low power schemes implemented on 180nm, 90nm, 65nm and 45nm nodes, and the results are presented in *table1-table 4* and the corresponding graphs are shown in *figure 5(a)* to *figure 5(e)*. It is observed that 45nm technology implementations presented in table 4 show a significant amount of delay and area improved. And the sleepy keeper approach performed better compared to the other techniques. When compared to sleep approach, sleepy stack achieves 2% delay increase, up to 91% area increase but 41% decrease in static power. Sleepy keeper achieves 1% increase in speed, up to 70% area increase and 56% decrease in static power. The sleepy stack method requires as much as 74% more space, although it may be up to 52% quicker than the forced stack method that preserves state. Up to 55% covered more area with the sleepy keeper method. However, only up to 53% quicker can be achieved. Compared to base case, sleepy stack achieves 77% decrease in static power and 53% decrease in dynamic power.



(a)



(b)

Figure 6: (a) 5-stage RO output (b) 5-stage RO frequency response

Sleepy keeper achieves 83% decrease in static power and 54% decrease in dynamic power. The leakage power is reduced by a factor of 15 with the dual Vth sleepy stack, while the latency is reduced by 26%, and the area is increased by 75% compared to the forced stack. The double V_{th} tired keeper is 35 % faster and uses 55% less space than the forced stack while lowering leakage power by 17 times. 5-stage ROs designed with sleepy keeper and bias current technique transient results are presented in figure 6, from the results it is observed that the frequency of oscillations is 1.27GHz, and the comparison results are shows in *table 5*.

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Table 5: Comparison with Similar Kind of Designs

Ref no	Process (nm)	Supply (V)	Power (µw)	Delay (ps)	Frequency (Hz)	Area (mm^2)	stages (nA)	Technique
9	90	1.2	46.8	43.84	1.2G	111.30	7	Current starved
10	130	1	16.85	--	24M	1.22	5	Current starved
11	130	1.8	56	--	20M	0.22	5	Dual Vth
12	130	3.3	55.6	--	1995.5 M	1.32	3	RC n/w
13	180	1.8	34.1	--	1M	0.084	5	Sleep Dynamic Vth CTAT
15	90	1.3	30	--	2G	0.56	9	combines multi-objective optimization
16	90	0.3	7	--	235M	0.002	3	bootstrapping
This work	45	0.5	16	0.25	1.27G	$1.99x10^{-5}$	5	Sleepy keeper

5. CONCLUSION

A 5-stage Ros with different low power techniques implemented with CMOS inverters in the paper. Each design is implemented in different nano scale technologies, and simulated to verify different performance metrics, and observed that sleepy keeper technique employed in the RO design shows better performance than all other schemes. The power, area, and the delay values of the proposed RO are better than any other literature. It produced the maximum frequency of oscillation and bandwidth than other types of ROs.

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