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Design DC/AC Converter for Renewable Energy Sources

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ABSTRACT- Multilevel inverters are vastly used in power systems and "renewable energy sources" (RES) to provide an AC voltage with a low level of harmonic contents. This paper aims to design a 9-level inverter for RES such as photovoltaic (PV), wind turbines, and fuel cell *etc.* a 9- level inverter. The proposed inverter is constructed by 12 IGBT switching devices where all of which are powered by 4 DC sources of 81 V without balancing capacitors to make DC voltage 324 V. A Phase disposition (PD), alternative phase opposition disposition (APOD), and POD with a slight phase shift are the methods of modulations that are used to provide a sinusoidal waveform of the output current and voltage. The minimum "Total harmonic distortion" (THD %) of the output voltage of the inverter is 13.68 % and 1.7 % in the cases where there is no filter and with filter conditions respectively. A PI controller is utilized for regulation of the load voltage is regulated by based on the RMS value of the inverter output voltage.

Keywords: 9-Level, Harmonics, Inverter, Modulation, THD.

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1. INTRODUCTION

Recently, due to the increase in global warming and energy demand where these are considered essential energy challenges worldwide. [1-3]. Among all the solutions that are concerning these challenges, "renewable energy sources" (RES) are introduced such as such as fuel cells, PV panels, and wind turbines [4-5]. Generally, the electrical energy is obtained from the RES in DC form. Thus, it is required to use such DC/AC converters that can provide the sinusoidal waveform of the voltage and currents at the fundamental frequency with a low "total harmonic distortion" percentage (THD %) [6-7]. Many multilevel DC/AC converters (inverters) (MLI) topologies are introduced for the RES applications [8-10]. By raising the levels number of the output voltage, low THD % is obtained with increasing system reliability and loading efficiency. So, there is a large concern about designing 9-level inverters. Maruthu Pandiyan. R et al. [11] designed a cascaded H bridge 9-level inverter for PV systems. The design is made of 16 IGBT switching devices. N. N. Prasetiyo and L. H. Pratomo [12] introduced 9-level MLI which is constructed by a combination of H-Bridge inverter preceded by 4 step-down DC-DC converters and. The 4 step-down DC-DC converters operate with high switching frequency to generate the voltage levels and the H-bridge portion is operated by the fundamental frequency (50 or 60 Hz) to reverse the output voltage polarity. In [13] a hybrid wind and PV RES 9-level inverter. The design is made of 9 IGBT switches with 2 power sources with a cascaded mechanism to increase voltage levels. Both authors in [14] had introduced a single source 9-level inverter with a boost mechanism with 11 IGBT switches. Their proposed design is appropriate for voltages at low ranges utilizations such as PV and fuel cells. A single DC source switched capacitor 9-level inverter is made in [15] for PV systems. The benefits of this design are a reduction in spike currents of the charged capacitors, multiple levels of the DC source input section, and voltage boosting. Z. Sarwer et al. [16] had presented 2 designs of switched capacitors inverter. The number of the output voltage levels is 9. Both designs are powered by a single DC source in parallel with 2 DC side capacitors. The number of the switching devices are 8 for the 1st design and 10 for the 2nd design. B. N. Rao et al. [17] had also designed the same number of level inverter and DC supply source. The number of power switches is 8. Where the THD is 12.9% and 1.85 for the inverter voltage and current respectively. A 9-level step-up inverter had been made by Y. Wang et al. [18] which is supplied by a single DC source and can attain 4-times of voltage gain. In this design, the H-bridge portion is eliminated and the inverter topology is built by using 13 of power switches. The PD modulation method is used by 8 carriers where the THD is 15.18%. The aim of this paper is another design of a 9-level inverter for RES. It is constructed by several DC sources with a reduced number of switching than the conventional cascaded H bridge type with the same number of output voltage levels. Also, the proposed design involves the utilization of many modulation methods to obtain a lower THD %. The topics of this paper are ordered as follows: An introduction, the proposed DC/AC converter, Modulation methods, and switching modes, results & discussion, and conclusions.

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2. PROPOSED DC/AC CONVERTER

The proposed 9-level inverter schematic diagram is shown in Figure 1. The inverter is supplied by 4 DC sources named Vdc_1 to Vdc_4. The inverter is constructed by 12 IGBT switches where each IGBT switching device contains an anti-parallel across it. Four of the 12 IGBTs are forming an H-bridge inverter. The H-bridge portion is essential to make the sine waveform of the inverter's output voltage. The switches S1 to S8 are responsible about the changing between the different levels of the output voltage. The output voltage is made of 9 levels in form of +Vdc, $+\frac{3}{4}$ Vdc, $+\frac{1}{2}$ Vdc, $+\frac{1}{4}$ Vdc, 0 Vdc, $-\frac{1}{4}$ Vdc, $-\frac{1}{2}$ Vdc, $-\frac{3}{4}$ Vdc, and $-$Vdc. In comparison with cascaded bridge 9-level inverter [12], in the current design there are reduction in the used IGBT switching devices by 25 %.

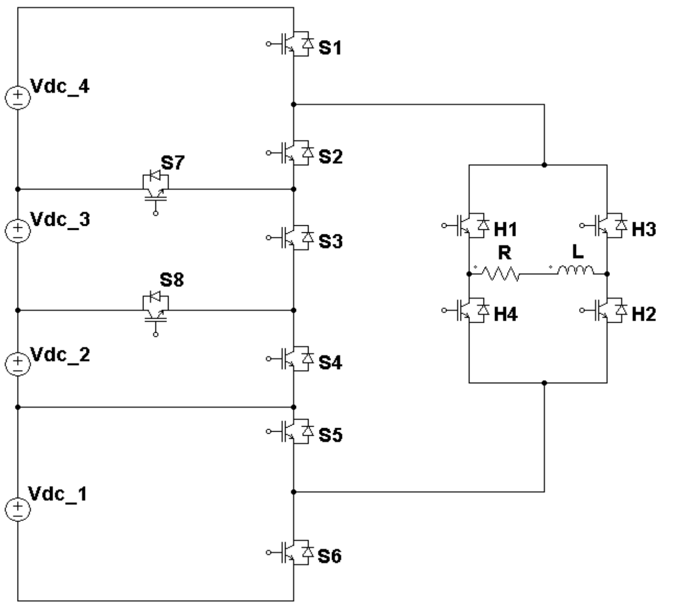

Figure 1. The proposed nine-level inverter

3. MODULATION, SWITCHING MODES, AND VOLTAGE CONTROL

The modulation technique in this inverter is sinusoidal "pulse width modulation" (PWM). There are four triangular waveforms as carriers in are set at high frequency up to 20 kHz. These carriers are used to modulate a reference signal which is an absolute of a sine wave as shown in *figure 2*.

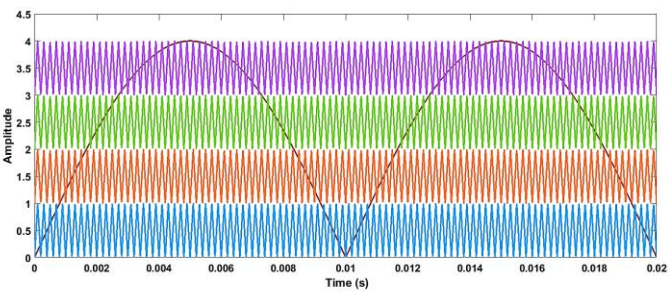

Figure 2. Modulating signals with the four carriers

The relation between the reference signal A_r and the four carriers which are $Ac_1, Ac_2, Ac_3, \& Ac_4$ is called the modulation index M_i where:

$$M_i = \frac{A_r}{Ac_1 + AC_2 + Ac_3 + Ac_4} \quad (1)$$

Each of A_r, $Ac_1, Ac_2, Ac_3, \& Ac_4$ signifies the highest value of their respective waveforms. The expression of the output voltage can be by:

$$V_o = M_i \times Vdc \times \sin(\omega t) \quad (2)$$

Where Vdc represents the sum of all DC sources voltage. Each carrier can be set at different methods like alternative phase opposition disposition (APOD), phase disposition (PD), and phase opposition disposition (POD) [19-21].

In this study, there is a possibility to investigate the performance of a slight phase shift between carriers for each of the mentioned modulation methods. The phase shift can be made through shifting of three of the carrier's waveforms time by 0, 0.00004, 0.00006, 0.00008 (s) respectively as shown in *figure 3*.

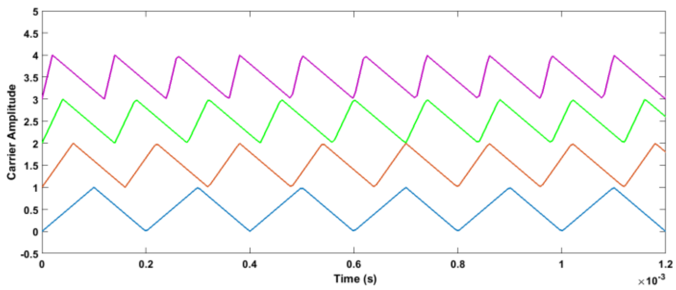

Figure 3. Carriers slight phase shift

There is a comparison between each carrier with the reference signal to generate the pulse signal for the S1 to S8 switches. For the H1 to H4 IGBT switches the reference signal is compared with zero. Figure (3) shows the SIMULINK model of the pulses generation for each IGBT switch. Table (1) lists the switching mode status for each IGBT switch. In the proposed design, the number of output voltage levels (N) can be expanded or shrunk by the number of DC sources and IGBT switches where the general formula for the number of DC sources concerning N is:

$$Number\ of\ DC\ sources = \frac{N-1}{2} \quad (3)$$

Also, the general formula of the number of IGBT switches is:

$$Number\ of\ switching\ devices = N + 3 \quad (4)$$

The formula of percentage of total harmonic distortion (THD) is [22]:

$$THD = \sqrt{\left(\frac{V_{rms}^2}{V_{1,rms}^2}\right) - 1} \times 100\% \quad (5)$$

Where V_{rms}^2 represents the total output voltage RMS value and $V_{1,RMS}^2$ represents the fundamental components RMS value of the output voltage.

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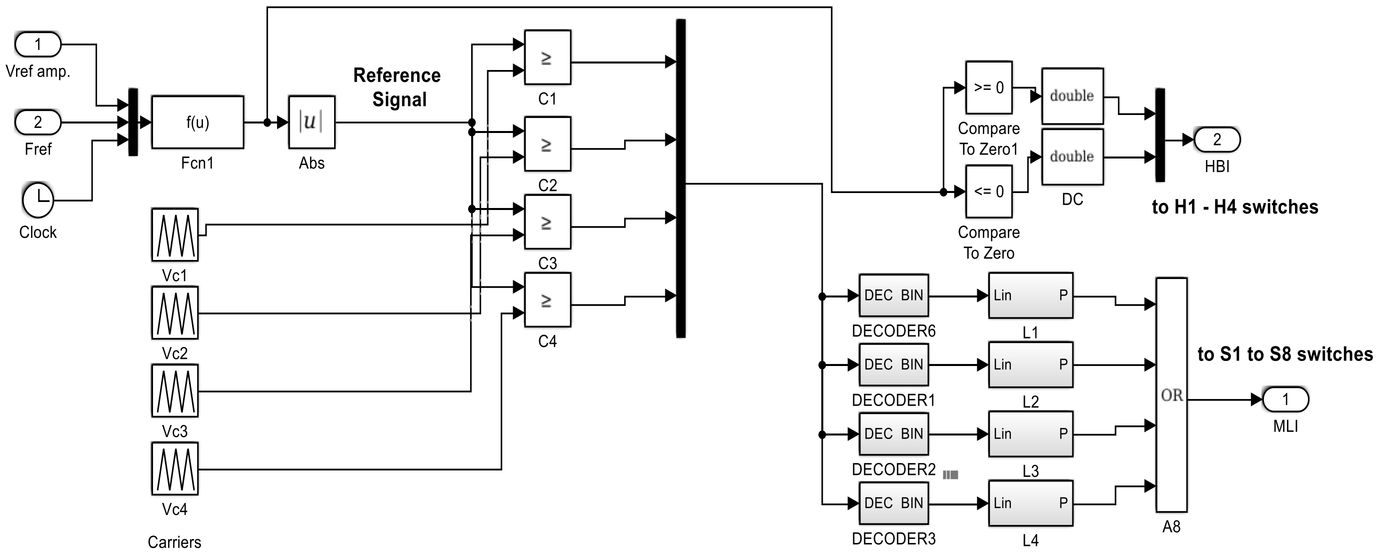

Figure 4. simulation model for the pulse generation for each IGBT switch

Table 1. Operation modes of the proposed 9-level inverter

Switches	+Vdc	$\frac{3}{4}$ Vdc	$\frac{1}{2}$Vdc	$\frac{1}{4}$ Vdc	0	0*	$-\frac{3}{4}$ Vdc	$-\frac{1}{2}$ Vdc	$-\frac{1}{4}$ Vdc	−Vdc
S1	ON	ON	ON	ON	OFF	OFF	ON	ON	ON	ON
S2	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
S3	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF
S4	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF
S5	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
S6	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
S7	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
S8	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
H1	ON	ON	ON	ON	OFF	ON	OFF	OFF	OFF	OFF
H2	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF
H3	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON	ON
H4	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	ON	ON

The output voltage of the proposed inverter can be regulated be using of a PI controller [23]. This controller is based on two main regulators which are the integral and the proportional regulators where it is expressed mathematically by:

$$u(t) = K_p e(t) + \frac{K_c}{T_i}\int_0^t e(t)dt \qquad (6)$$

Where $u(t)$ is referred to the controlling is signal, $T_i$represents the integration time, K_p is the proportional gain, and $e(t)$ represents the error between the actual inverter value and the desired RMS value.

The regulation is based on the value of the RMS voltage of the inverter output voltage. Thus, the RMS voltage signal is sensed by a voltage meter and compared with a reference. The generated signal from the PI controller is multiplied with a sine wave with the same amplitude and frequency of the A_r signal. The result is passed through a gain to produce the controlling A_r modulating signal. The proposed control signal is shown in *figure 5*.

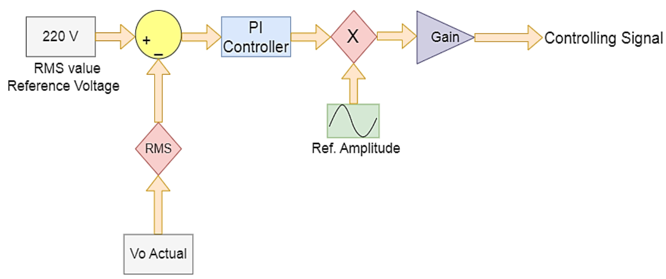

Figure 5. Proposed controller of the inverter output voltage

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4. RESULTS AND DISCUSSION

The designed 9-level inverter is simulated in MATLAB SIMULINK. The output voltage at its output terminals and the load current are shown in *figure 5*. Four DC sources are involved in the design. Each source is 81 V. The accumulation of all DC sources yields 324 V which represents the peak value of the output voltage waveform. The fundamental frequency and the carrier frequency are set at 50 Hz and 10 kHz respectively. The rated power of the designed inverter is up to 10 kW.

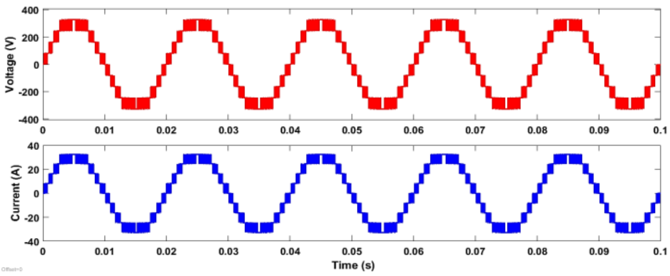

Figure 6. Output load voltage and current (without filter)

Figure 6 represents the THD % of the output terminal voltage at rated frequency. It was found that the THD is 13.68 % without adding a filter at the load side. Where the modulation index is 1. The RMS value of the output voltage is 229.1 V. It is possible to add an LC filter where the inductance (L) of it is 4.06 mH and the capacitor (C) of it is 6.25 µF. The filtered output voltage is shown in *figure 8.*

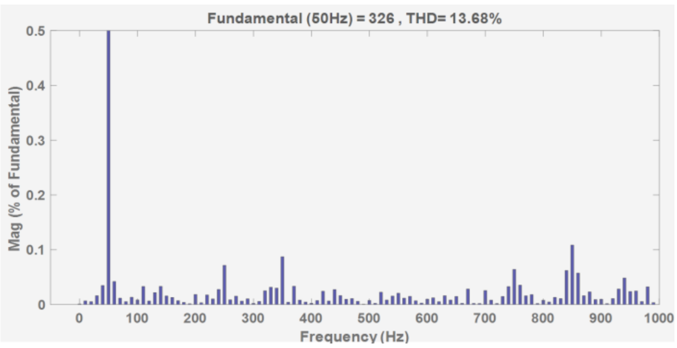

Figure 7. THD percentage of the load voltage (without filter)

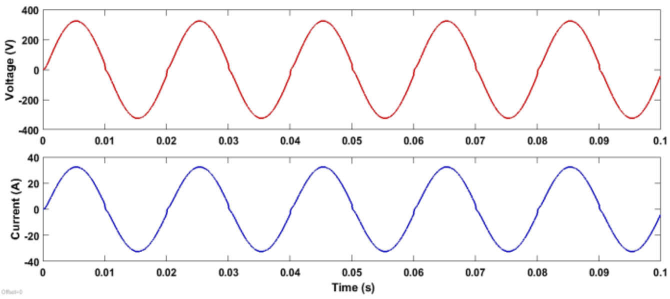

Figure 8. Output load voltage and current (with filter)

In this research, there are 3 methods of modulation are made which are PD, POD, APOD. *Table (2)* lists the output voltage THD % without filter for each modulation method. It was found that the PD lets the output voltage has the lower THD whereas the APOD makes it has the highest possible THD %.

Table 2. THD % at different methods of modulation (without filter)

Modulation type		Voltage THD (%)
Carriers without phase shift	PD	13.68
	POD	13.7
	APOD	13.72
Carriers with phase shift	PD	13.7
	POD	13.68
	APOD	13.74

In any modulation method, three modulation status can be applied which represents the relation between the modulation index (M_i) and the THD. These statuses are full modulation when the peak of the highest carrier is equals the peak of the reference sine signal i.e. M_i=1, or under modulation when M_i < 1 and over modulation when M_i> 1 [24]. Table (y) lists the modulation status in the case with filter or without filter. From this table, it can be noted that in the case without filter, the over modulation reduces the THD % whereas in the case with the filter the Full wave modulation provides the lowest THD% of the output voltage and in over modulation is the highest THD % due to the occurrence of DC signal with the THD % which cannot be filtered out.

Changing of the M_i can regulate the 9-level inverter output voltage by changing its shape, number of levels, and its RMS value as well. If the M_i< 0.75 the inverter works as 7-level inverter, if the M_i< 0.5, the proposed inverter can work as 5-level inverter, if the M_i< 0.25, it will behave as 3 level inverter. To regulate the output voltage of the inverter, the proposed voltage controller of Figure 5 is used where the gains of the PI controller are 20 and 0.03 for the integral and proportional gains respectively. The gains are obtained through manual tuning to get the best regulation results.

Table 3. THD % at different modes of modulation in PD method

	Filtering status	Full wave modulation (M_i=1)	Under modulation (M_i=0.8)	Over modulation (M_i=1.2)
Carriers without phase shift	Without filter	13.68 %	15.71%	12.58%
	With filter	1.77	1.84 %	2.44 %
Carriers with phase shift	Without filter	13.7 %	17.19 %	12.48 %
	With filter	1.7 %	1.75 %	2.34 %

Figure 9 shows the current and voltage results of the voltage controller performance before and after load switching, where the load is switched from 4480 W to 9680 W. In this figure, it can be noted that the regulator rapid response where the voltage

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at the load side is fixed at the same RMS value and only the load current is increased.

Table 4 represents a comparison of some of the previous work-specified data about 9-level inverter design with the proposed work. The comparison is made about the modulation method, No. of DC sources, THD percentage of the design output voltage, and No. of power switches. In this table, it can be seen that the current study was not limited to a single modulation method, also, an investigation is made about the slight phase shift of each of the well-known modulation methods which are PD, APOD, and POD. With using of filters, present work gives a lower THD than the other previously made 9-level inverter designs that are mentioned in this paper.

Table 4. Comparison of previous studies about 9-level inverter design with the current study

Ref. No.	Modulation Method	DC Sources No.	Output Voltage THD (%)	Power Switches No.
[12]	Not specified	4	1.89 (with filter)	16
[13]	PD	1	16.73 (without filter)	9
[15]	Not specified	1	Not specified	11
[16] 2-designs	Level shifted PWM	1	9.2 and 16.76	8 and 10
[17]	PD	1	12.9	8
[18]	PD	1	15.18	14
Proposed work	Phase shifted (PD, POD , and APOD)	4	13.7, 13.68, and 13.74 (without filter) 1.7 (at PD with filter)	12

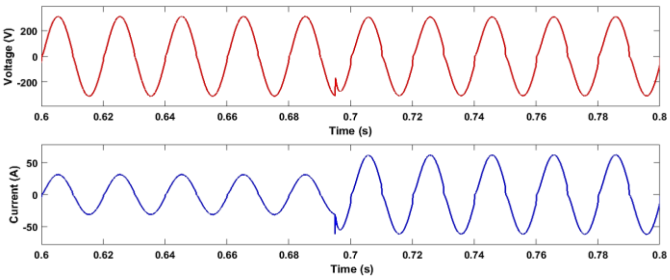

Figure 9. Effect of voltage controller after load switching 4480 W to 9680 W

5. CONCLUSION

In this paper, a design and simulation for 9-level inverter for RES is made successfully. It can be deduced that in this design provide the output voltage at low THD percentage weather its output terminals are filtered on unfiltered. Also, the modulation by PD method is better than POD and APOD methods. After adding an LC filter, the best results in THD are when the Mi =1 where full modulation between the carriers and reference signal can occur. Due to the existence of several DC sources, this inverter is suitable to be supplied through different voltage levels of RES such as PV solar or wind turbines. Through the investigation of the phase shifted modulation techniques, it was found that the THD is reduced than the typical PD, APOD, and POD methods especially when the filters are used where with PD methods the THD is 1.7 %. The proposed voltage controller has a rapid response to load changes with an accurate value of RMS voltage at the load side. In the future, the four DC sources will be substituted by high capacitors value and only a single DC supply can be used across them. Also, utilization of better voltage regulation methods is necessary for rapid response to uncertainties such as load switching of source voltage flickers.

Conflicts of Interest: “The authors declare no conflict of interest.”

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