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A Cascaded H-Bridge Multilevel Inverter with DC Cells Input Fault Tolerance Capability Based on PSC-PWM Control

Tajeddine Khalili[1], Abdelhadi Raihani[2], Amal Kadri[3], Soukaina Saghir[4], and Mustapha Oulcaid[5]

[1]LICPM Laboratory, ENSA Béni Mellal, Sultan Moulay Sliman University, Béni Mellal, Morocco
[1,2,3]EEIS Laboratory, ENSET Mohammedia, Hassan II University of Casablanca, Morocco
[4,5]LGS Laboratory, ENSA Béni Mellal, Sultan Moulay Sliman University, Béni Mellal, Morocco

***Correspondence:** Tajeddine Khalili (Khalili.tajeddine@gmail.com)

ABSTRACT- Multilevel inverters have proven their efficiency in generating better AC voltage outputs. This functional quality is mainly due to the use of multi-source DC inputs. Despite the fact that this type of topology is generally reliable, switching faults caused by the complete loss of a switching component or DC input cell may still occur. Such incident may inflict heavy impacts to the conversion chain resulting in a permanent damage to the switching cells or the connected load. This article presents a dynamic switching control strategy capable of tolerating DC cells open-circuit input faults in basic symmetric Cascaded H-bridge multilevel inverter architectures. The proposed topology uses a control scheme to overcome the switching cells' fault by adapting the configured level of conversion and bypassing the flawed unit with no additional switching components. Furthermore, the proposed control strategy is capable of reversing back the inverter configuration to its original functional state after the disappearance of the faut. This research article answers the need for a theorical study of a fault tolerant Cascaded H-Bridge multilevel inverter where the short circuit's fault types are bypassed by Pulse width modulation alteration only.

Keywords: Multilevel inverter, Cascaded H-Bridges, Open circuit fault tolerance, Phase shift control, SPWM, Polymorphic multilevel inverter.

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1. INTRODUCTION

Multilevel inverters (MLIs), in last years have emerged as one of the most promising applications in the energy conversion field [1-3]. Their attractive features are behind this ever-growing interest. In fact, multilevel inverters, through their capability of generating more than two levels, have dominated the classic DC/AC converters in terms of performance [4-6]. MLIs offer lower switching losses and can operate at higher voltage applications, unlike classic converters which are generally limited to lower voltage use and suffer greater switching losses. MLIs are constantly studied for integration in various technology applications like electric vehicles [7-9], stand alone and connected multi photovoltaic string conversion systems [10-12]. Despite the noticeable performance of multilevel inverters architectures, many flaws and operating incidents have been reported [13-14]. One major issue, is the loss of a DC input cell or switching component prior to a major fault on the AC voltage output side. This, has been the object of research papers aiming to establish a fault detection and evaluation approaches [13-15]. Research works proposed numerous applications to compensate or even instantly overcome the effect of a switching fault. This tolerance can be achieved through instantaneous reconfiguration and structural design [16-17]. The tolerance capability can also be integrated using adequate control strategies and proper online diagnosis of the DC input cells and switching components [18-22]. Cascaded H-Bridge multilevel inverter (CHBMLI), being a performant architecture is often the basis of such upgrades.

In ref. [15], Anand et al proposed a generalized switch fault diagnosis protocol based on the same CHBMLI architecture using mean voltage prediction, their proposed scheme is capable of detecting the source of a fault withing one period. However, no setup was proposed to overcome the fault, and the detection protocol itself, is destined to faulty switches and doesn't identify cases where the DC source is the origin of the fault. In Ref. [17], Raza et all proposed a research paper introducing a modified multi-DC source structure of MLIs with fault tolerant capability against open circuit fault, the structure namely clears the fault incident trough the proper readaptation of the command. The entire structure was conceived in order to simplify the switching strategy alteration in case of a failure. Nevertheless, the proposed scheme integration in industrial applications is highly complicated, due to the number of combinations needed for every situation. In addition, authors didn't study the impact of modulation type on the architecture despite an evaluation of the switching losses. In Ref. [18], Zhao

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Liu et all focus on battery energy storage systems (BESS) failure. Authors assume that during a BESS management system fault, the proposed control method can regroup the batteries withing the BESS and evenly distribute the active power between its cells (Batteries and capacitors). The architecture presented by the authors is mainly based on the CHBMLI and ensure the continuum of the BESS management after a control failure, however, it doesn't offer a strategy in case of a specific battery voltage drop or switch open/short-circuit fault. In Ref. [19] Jinyu Wang and all propose a detailed analysis of a fault tolerant operation in modular multilevel converters (MMCs) based on an adaptive phase shifted carrier modulation control. The proposed method bypasses the faulty switch in a cell and readapt the feedback voltage, thus, keeping the cell's functionality unchanged. This operation is conducted using a voltage balancing controller equipped with a sorting method destined to control the carriers. this strategy offers a reliable method to overcome an individual switch failure, However, the work doesn't discuss the short-circuit fault withing the power bank outputs, which would be very complicated in this case because the method basically controls the voltage within the input capacitors.

Many research works, similar to the previously presented contributions, treated the tolerability issue among multilevel inverters using, either the total reconfiguration of the topology or the adaptation of the modulation strategy [20-22]. Following this survey, it can be noticed that the majority of papers have studied the fault occurrence as an open-circuit event within switching components and generally adopts methods that either dramatically changes the circuitry of the MLI or introduces a completely different command protocol for each case. The present paper fills a very important gap regarding the fault tolerance in multilevel inverters; it provides a simple method to overcome a DC voltage input loss in a CHBMLI without demanding any additional components or change in command scheme. While the existing studies deal with faults occurring on the switching devices, the present study is focused on the impact of DC voltage sources connected the CHBMLI; a sudden drop in voltage value can also have a very fatal impact on loads in power conversion applications. Furthermore, the control strategies mostly use a modulation alteration in order to keep a steady level, or modifies the structure of the original architecture. The current paper is focused on the CHBMLI as a study subject under fault conditions while offering the same SPWM in each fault condition with a change in phase shift applied to the original carriers while reconfiguring the adopted conversion level. The studied symmetric CHBMLI is capable trough integrated bypasses and online control of overcoming a DC open-circuit input fault. Multiple DC inputs and semiconductor switches have been used, depending on the MLI configuration, to operate at the maximal allowed level. Following a fault occurrence, the related controller adapts the output level in order to reduce the fault effect and keep a symmetric voltage output. Additionally, the developed architecture reestablishes the normal functioning sate after the fault disappearance on input side or switching hardware. This technical approach ensures the best operating performance in times of normal functioning. In addition to the fault tolerance capability, the proposed architecture minimizes the Total Harmonic Distortion (THD) content in the output voltage by favoring the highest possible configuration of levels through the exploitation of all functional components. The limited use of additional switches guarantees minimal switching losses and an economic integration to existing regular and hybrid CHBMLI-type topologies. A detailed analysis of the proposed fault tolerant multilevel CHBMLI based inverter was presented. The operating of the converter is analyzed under various fault scenarios, after which, a summarized performance analysis with fault tolerance analysis is presented in order to assess the efficiency of the proposed scheme. The results are then, validated trough proper simulation reasoning and analysis using MATLAB and Simulink.

2. CHBMLI MODEL

2.1 The CHBMLI Architecture

The architecture concept used in this article is based on a classic cascaded H-bridge multilevel inverter. This topology is constructed by cascading a series of H-bridge inverters; 2 full-bridge cells can produce a staircase voltage waveform of 5 levels. Unlike the two classic architectures Diode Clamped Multilevel Inverter (DCMLI) and the Flying Capacitor Multilevel Inverter (FCMLI), the CHBMLI topology doesn't require the use of interlocking diodes and flying capacitors. This simplicity of integration and the flexibility of use are the main reasons why many research works have used it as a basis for further development [23-24].

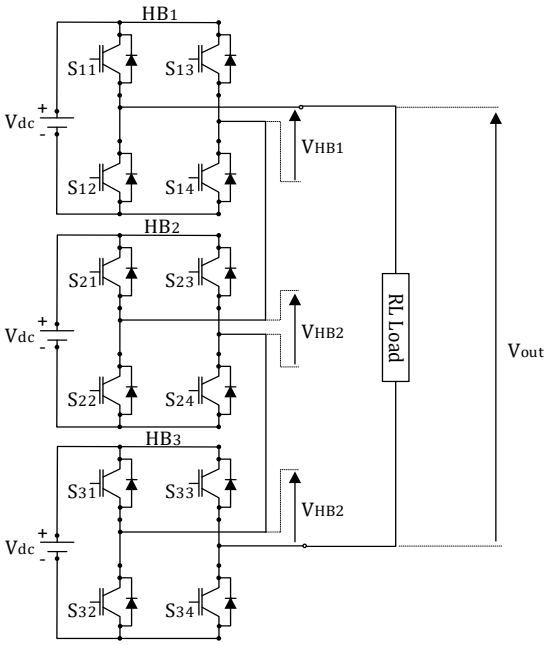

Figure 1. 7 levels Cascaded cells H-Bridge multilevel inverter

In Ref [25], A comparative analysis of different control strategies applied to a 15 levels CHBMLI was conducted to establish the contrast between proportional/integral controller, fuzzy logic controller and neural network controller. It can be seen on this article that the structure of the CHBMLI was slightly altered to minimize switching components and

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maximize the number of generated levels. In ref [26], authors use a simple level doubling network to double up the voltage levels and thus preserving the same modularity without any additional switches. This same technique can be used with any structure to control the voltage level while minimizing the number of used switches.

Figure 1 present the adopted multilevel inverter in 7 levels mode. If we consider an independent HB cell with a V_{dc} input voltage, it can deliver 3 voltage levels: $-V_{dc}, 0, V_{dc}$. With the configuration presented in figure 1, where the voltages V_{dc1}, V_{dc2} and $V_{dc3}$are different 15 levels can be generated, ranging from $-(V_{dc1}+V_{dc2}+V_{dc3})$ to $+(V_{dc1}+V_{dc2}+V_{dc3})$ and using all possible combinations between the different cells. Table 1 presents the possible switching states for one H-bridge cell HB_i with a V_{dci} voltage input. The 4 switches used in each cell HB_i will be noted S_{i1}, S_{i2}, S_{i3} and S_{i4}, the voltage output will be noted V_{Hi}.

Table 1. Possible switches states for a single H-Bridge cell

		S_{i1}	S_{i2}	S_{i3}	S_{i4}
State 1	V_{dci}	1	0	0	1
State 2	0	0	0	0	0
State 3		1	0	0	0
State 4		0	1	0	0
State 5		0	0	1	0
State 6		0	0	0	1
State 7		1	1	0	0
State 8		0	0	1	1
State 9		1	0	1	0
State 10		0	1	0	1
State 11	$-V_{dci}$	0	1	1	0

Table 2 present the voltage output of the multilevel inverter based on the possible combinations of the HB cells. It can be noticed in *table 2* that each output voltage is given by a unique set of cells combinations, however, redundant combinations producing the same voltages can be exploited in case of identical voltage on the HB cells input's side. For instance, if we consider that all voltage inputs are equal to V_{dc}, the MLI voltage output $2V_{dc}$, is possible in all the following combinations:

- Combination 1: $V_{HB1}=V_{dc}, V_{HB2}=V_{dc}, V_{HB3}=0$
- Combination 2: $V_{HB1}=V_{dc}, V_{HB2}=0, V_{HB3}=V_{dc}$
- Combination 3: $V_{HB1}=0, V_{HB2}=V_{dc}, V_{HB3}=V_{dc}$

As it can be observed on table 1, the voltages V_{dci} and $-V_{dci}$ are possible in singular states (State 1 and State 11). It can also be noticed that all states from 2 to 10 produce a 0 voltage. However, it should be pointed out that state 2 to state 6 can be exploited in single use of the H-Bridge only, since the use of these states might block the cascaded function of the multilevel inverter. States 7 and 8 create a short-circuit for the voltage source $\boldsymbol{V_{dci}}$ and can't be exploited as such. States 9 and 10 are the only states usable in a cascaded configuration, because they allow the interconnection to the next cells without adding the cell's voltage. Following the previously presented arguments, states 1, 9, 10 and 11 are the only states that will be used with the present architecture.

Table 2. Possible voltage combinations within the CHBMLI

MLI output	HB_1 voltage	HB_2 voltage	HB_3 voltage
0	0	0	0
V_{dc1}	V_{dc1}	0	0
V_{dc2}	0	V_{dc2}	0
V_{dc3}	0	0	V_{dc3}
$V_{dc1}+V_{dc2}$	V_{dc1}	V_{dc2}	0
$V_{dc1}+V_{dc3}$	V_{dc1}	0	V_{dc3}
$V_{dc2}+V_{dc3}$	0	V_{dc2}	V_{dc3}
$V_{dc1}+V_{dc2}+V_{dc3}$	V_{dc1}	V_{dc2}	V_{dc3}
$-V_{dc1}$	$-V_{dc1}$	0	0
$-V_{dc2}$	0	$-V_{dc2}$	0
$-V_{dc3}$	0	0	$-V_{dc3}$
$-(V_{dc1}+V_{dc2})$	$-V_{dc1}$	$-V_{dc2}$	0
$-(V_{dc1}+V_{dc3})$	$-V_{dc1}$	0	$-V_{dc3}$
$-(V_{dc2}+V_{dc3})$	0	$-V_{dc2}$	$-V_{dc3}$
$-(V_{dc1}+V_{dc2}+V_{dc3})$	$-V_{dc1}$	$-V_{dc2}$	$-V_{dc3}$

2.2 CHBMLI under normal conditions

During faultless conditions on the DC voltage sources, the proposed CHBMLI is working in standard mode. Meaning that no measures, except those related to the PWM command, are taken into consideration. In this section equal DC sources are considered as voltage inputs for the H-Bridge cells and a seven levels architecture is used as a model basis for the present study. *Table 3* summarizes all the possible combination and switches state in case of 7 levels multilevel inverter under standard conditions and symmetrical sources.

Table 3. Possible switching states in the case of 7 levels CHBMLI with symmetrical sources

V_{out}	S_{11}	S_{12}	S_{13}	S_{14}	S_{21}	S_{22}	S_{23}	S_{24}	S_{31}	S_{32}	S_{33}	S_{34}
$+V_{dc}$	1	0	0	1	0	1	0	1	0	1	0	1
	0	1	0	1	1	0	0	1	0	1	0	1
	0	1	0	1	0	1	0	1	1	0	0	1
$+2V_{dc}$	1	0	0	1	1	0	0	1	0	1	0	1
	0	1	0	1	1	0	0	1	1	0	0	1
	1	0	0	1	0	1	0	1	1	0	0	1
$+3V_{dc}$	1	0	0	1	1	0	0	1	1	0	0	1
0	0	1	0	1	0	1	0	1	0	1	0	1
	1	0	0	1	0	1	1	0	0	1	0	1
	0	1	0	1	1	0	0	1	0	1	1	0
	1	0	0	1	0	1	0	1	0	1	1	0
	0	1	1	0	1	0	0	1	0	1	0	1
	0	1	0	1	0	1	1	0	1	0	0	1
	0	1	1	0	0	1	0	1	1	0	0	1
$-V_{dc}$	0	1	1	0	0	1	0	1	0	1	0	1
	0	1	0	1	0	1	1	0	0	1	0	1
	0	1	0	1	0	1	0	1	0	1	1	0
$-2V_{dc}$	0	1	1	0	0	1	1	0	0	1	0	1
	0	1	0	1	0	1	1	0	0	1	1	0
	0	1	1	0	0	1	0	1	0	1	1	0
$-3V_{dc}$	0	1	1	0	0	1	1	0	0	1	1	0

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It can be noticed on the *table 3*, that each voltage level possesses a number of redundant switching states. This redundancy has been exploited trough research works for balancing stress on specific switches [2-3]. This same principle, can also be used to balance voltage between cells when capacitors are used as mediant inputs. In this research work, the stress and power distribution among switches is not studied. *Figure 3* shows the voltage and current output of the multilevel inverter in the absence of faults.

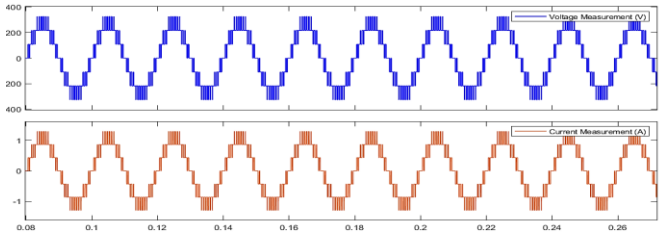


Figure 2. Voltage and current output of the 7 levels CHBMLI under normal conditions

The output voltage of the multilevel inverter can be expressed as the weighted sum of all voltage levels. This can be expressed as follows:

$$V_{out} = \sum_{i=1}^{3}\left[\left(\frac{V_{dci}}{2}\right)[(S_{i1}+S_{i4})-(S_{i2}+S_{i3})]\right] \quad (1)$$

Other expressions involving current logical variable, indicating the current flow have been previously used [28]. However, the proposed expression simplifies the interpretation of the circuit state. Thus, the only data needed is the switches states. Using Fourier expansion, the voltage output can be expressed as follows:

$$V_{out}(\theta) = \sum_{p=0}^{\infty}\left[\frac{4\omega V_{dc}}{\pi}[\cos((2p+1)\theta_1)+\cos((2p+1)\theta_2) + \cos((2p+1)\theta_3)]\sin((2p+1)\theta)\right] \quad (2)$$

In this case θ_1, θ_2 and θ_3 are the firing angles of the 7 levels cascaded H-Bridge multilevel inverter.

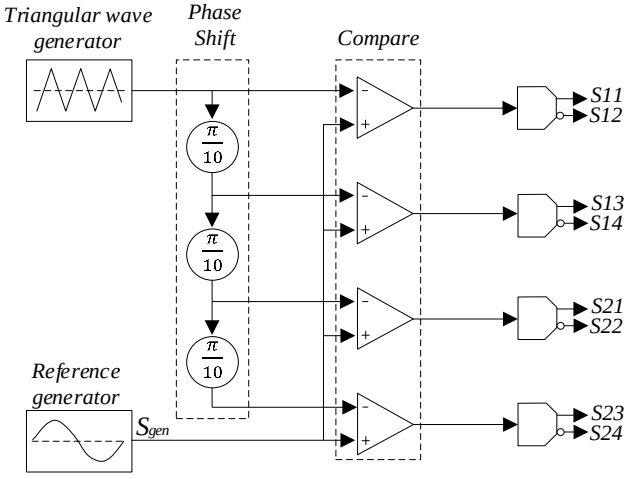


Figure 3. PSCPWM principle used to control the multi-level inverter

The modulation technique used to control the CHB multilevel inverter is based on phase shift carriers (PSCPWM). *Figure 3* illustrates an example of the implemented technique for à 5 levels version of the converter under normal conditions. The reference generator produces the function expressed at *equation (3)* and the wave form generated by the triangular generator oscillates between -1 and +1.

$$S_{gen} = 0.8\,sin(100\pi) \quad (3)$$

Each carrier created by the appropriate phase shift of the triangular waveform is compared to the sinusoidal reference. This comparison gives the adequate control pattern for switches S_{ij}. As it can be seen on *figure 3*, each S_{i1} and S_{i3} respectively have and opposite control signal to S_{i2} and S_{i4}.

3. CHBMLI UNDER FAULT CONDITIONS

During the studied fault incident, one or multiple H-Bridge cells may lose a voltage input which directly affects the generated levels on the staircase waveform of the MLI output. *Figure 4* illustrates the voltage and current output of the CHBMLI in case of $HB2$ cell fault. In this case the phase shifted carriers, used with the PWM controls don't change, because of this, the connected load is affected by the ill symmetry of the voltage output, the distortion of the signal and power loss due to the miscalculation of the firing angles.

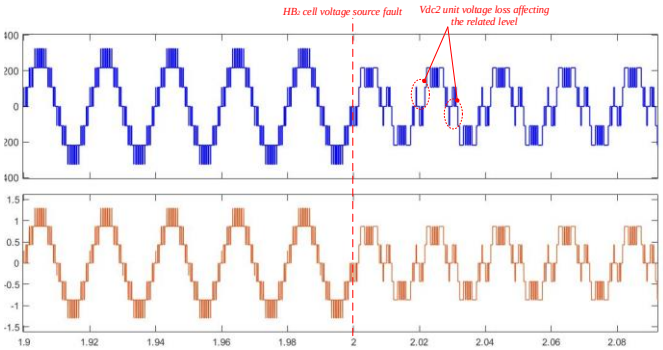
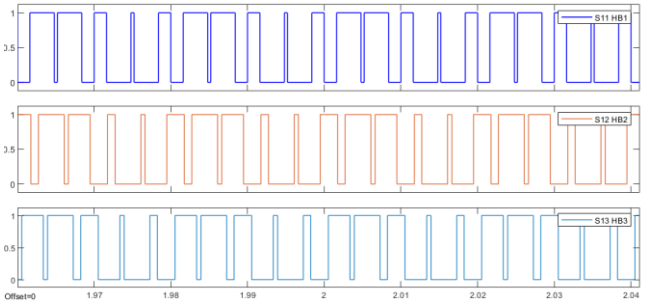


Figure 4. voltage and current output in case of HB2 cell fault in a 7 levels CHBMLI

Figure 6 illustrates the command patterns destined to control each of the switches S_{ij} in the three cells of a 7 levels CHBMLI multilevel inverter. As it can be seen, the switching command pattern doesn't change during the fault incident. These signals correspond to the states shown on *table 3*.



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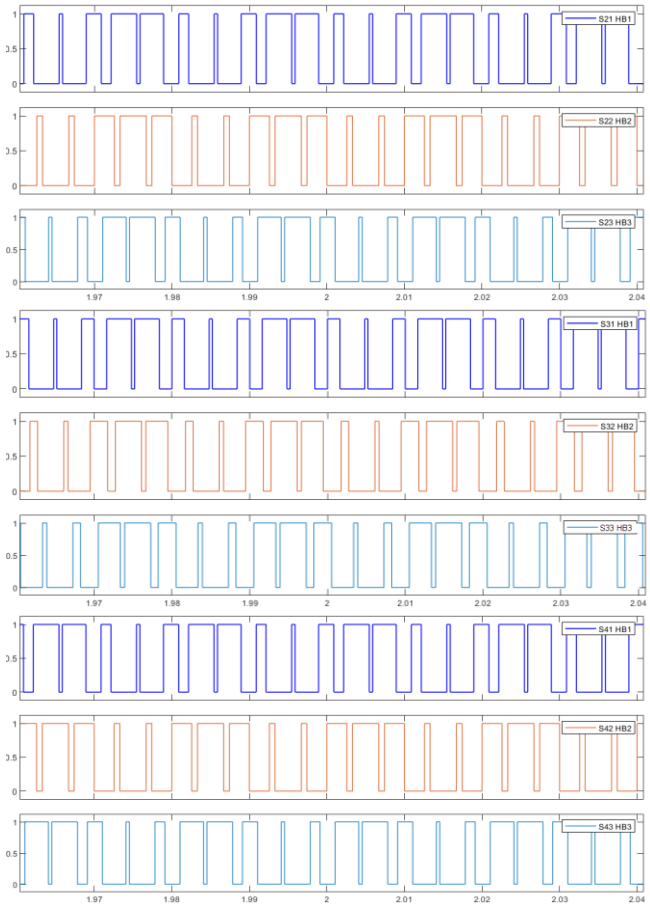


Figure 5. S_{ij} switches command sequence of the 3 cells for a 7 levels CHBMLI

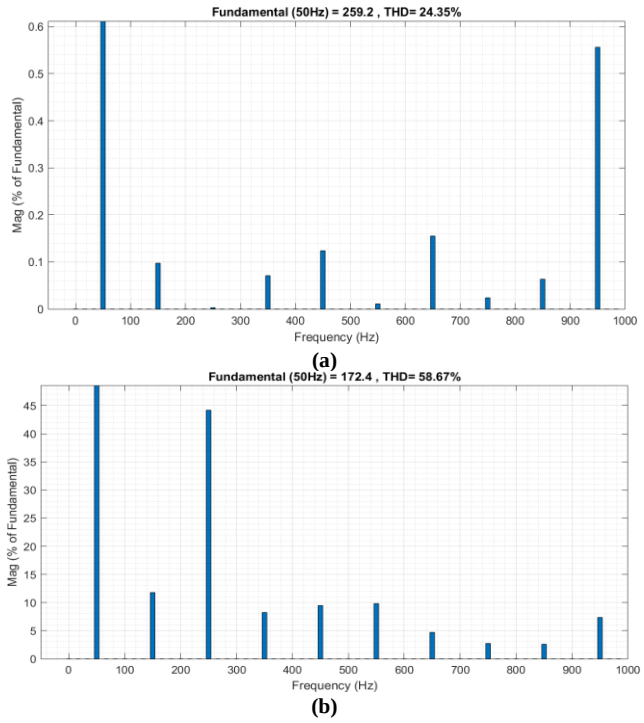
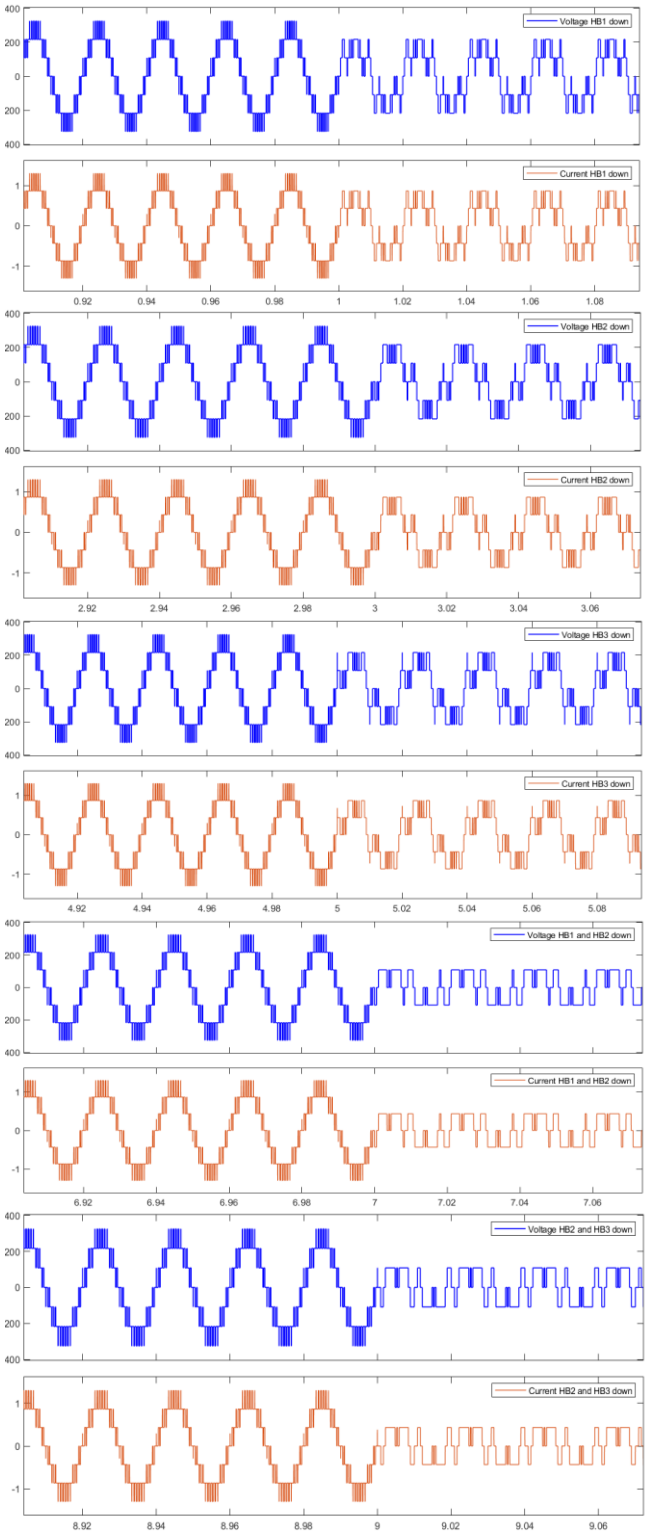


Figure 6. THD change after the loss of HB2. (a) MLI working properly, (b) HB2 cell down

The loss of a DC source at the input of a HB cell greatly affects the output waveform of the multilevel inverter. For instance, in case of 7 levels CHBMLI, the loss of HB2 voltage sources causes the THD to increase from 24.35% to 58.67% as illustrated on *figure 6*. In order to summarize all the possible MLI outputs based on HB cell states, series of simulation were conducted, *figure 7* illustrate all the registered results, classified by cell operation event.



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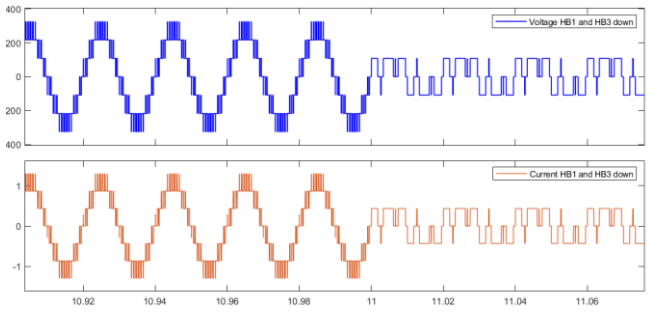

Figure 7. Types of faults of a 7 levels CHBMLI depending on DC source shutdown location

As it can be seen on *figure 8*, the effect of a cell's input loss on the voltage and current output depends on the cell number. When only one HB cell is lost during a normal operating, a semi five levels voltage output can still be observed, however it is severely disfigured. This distortion can both be observed, on the waveform of the voltage output and the total harmonic distortion. *Table 4* lists the measured THD of the voltage output in all possible cases.

Table 4. THD of the voltage output for different states of the 7 levels CHBMLI without any correction

State	Cell HB_1 voltage (V)	Cell HB_2 voltage (V)	Cell HB_3 voltage (V)	THD (%)
State 1	108.4	108.4	108.4	24.35
State 2	108.4	108.4	0	57.89
State 3	108.4	0	108.4	58.67
State 4	0	108.4	108.4	59.09
State 5	108.4	0	0	113.30
State 6	0	0	108.4	109.49
State 7	0	108.4	0	104.50

Table 4 summarizes the THD factor in the complete loss of a cell for different structures, and *table 5* presents the THD in case of voltage drop within single units of the multilevel inverter for different structures. As it can be seen on the same table, when one cell is lost, the loss of cell 1 is the most affecting. However, when two cells are lost, the simultaneous loss of cell 2 and 3 is the more affecting.

4. FAULT TOLERANCE STRATEGY

In the case of the 7 levels MLI architecture, If an H-Bridge cell is lost, the remaining cells can construct a symmetric staircase waveform of 5 levels maximum. The Fourier transform of a well-established 5 levels voltage output (best case scenario), using the same command, can be expressed as follows:

$$\boldsymbol{V_{out}(\theta) = \sum_{p=0}^{\infty}\left[\frac{4\omega V_{dc}}{\pi}\left[\cos\left((2p+1)\theta'_1\right)+\cos\left((2p+1)\theta'_2\right)\right]\sin\left((2p+1)\theta\right)\right]} \quad (4)$$

In this case $\boldsymbol{\theta'_1}$ and $\boldsymbol{\theta'_2}$ denotes the firing angles in the case of 5 levels. If we consider that $\boldsymbol{\theta_1}$, $\boldsymbol{\theta_2}$and $\boldsymbol{\theta_3}$ are the firing angles in the case of 7 levels configurates, we can write the following comparison:

$$\boldsymbol{\theta_1 < \theta'_1 < \theta_2 < \theta'_2 < \theta_3} \quad (5)$$

It is understood from the previous comparison that a proper alteration of the firing angles when a fault occurs can reestablish a proper functioning of the inverter on a lower number configuration. Thus, when two cells are still working properly, they can be used to create a 5 levels staircase waveform.

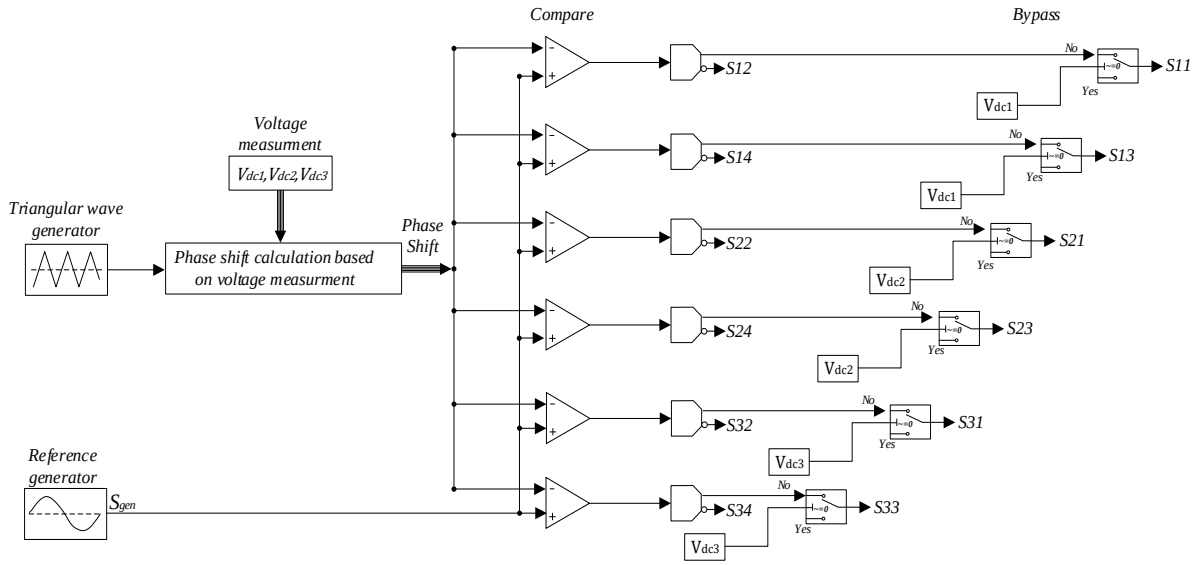

Figure 8. Carriers shift strategy used to control the 7 levels CHBMLI

This can be achieved by changing the phase shift of the carriers. *Figure 9* shows the diagram used to control the carriers shift. In *figure 8* we can see that the switches control stays basically the same, however, when a 0 voltage is measured at the input of a cell, it alters the phase shift of the carriers accordingly. Furthermore, the cell's input is bypassed using the switches of the said cell. For instance, When the CHBMLI is working in 7 levels, 3 firing angles are used to shift the carriers properly,

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however, when a voltage shutdown is detected at the input of one of the cells, the controller sets a new order of the cells by using only 2 firing angles and bypassing the faulty one. In order to integrate the strategy illustrated in figure 8, scheme in figure 9 was developed using MATLAB Simulink.

In the simulation scheme, the CHBMLI is equipped with a controller generating a fault code depending on the DC input voltage.

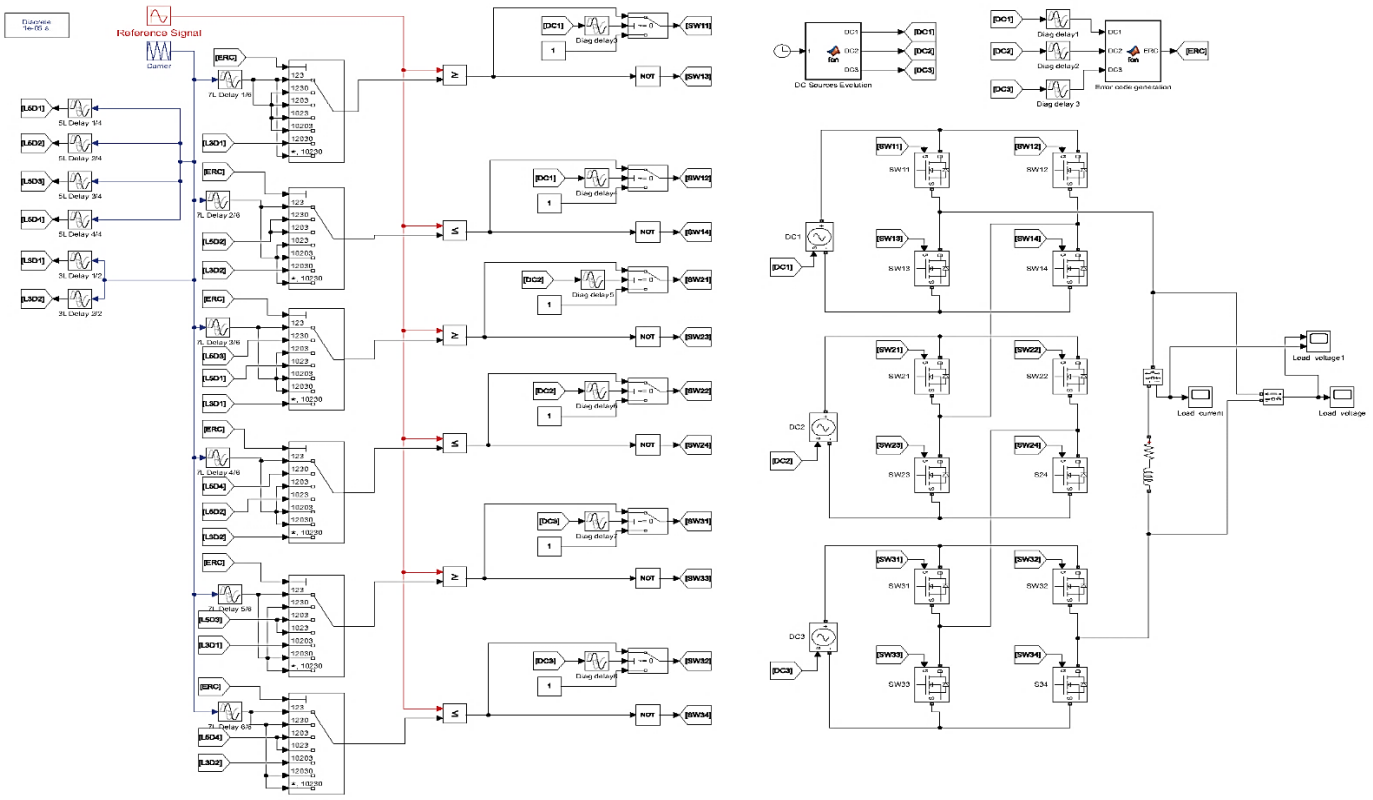
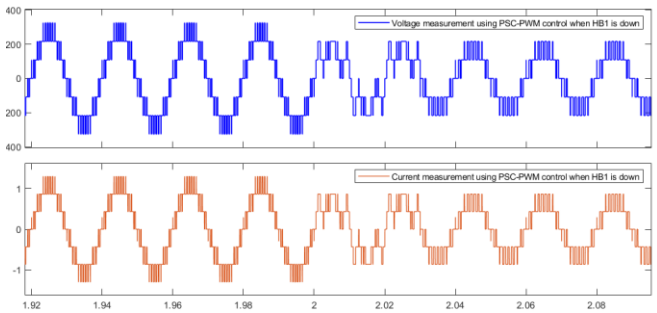


Figure 9. Simulation methodology used to integrate the fault tolerance scheme in the 7 levels CHBMLI

The fault code indicates which DC cell is down or has a very low voltage. For example, when HB2 is down while the two others are ok, the generated code is 1203; the "0" after "2" indicates the location of the fault. Depending on the generated code, the controller takes the necessary measures, bypassing HB2 in this case.

5. RESULTS AND DISCUSSION

In order to assess the validity of the presented control scheme, multiple scenarios involving the loss of HB cell's voltage input have been tested.



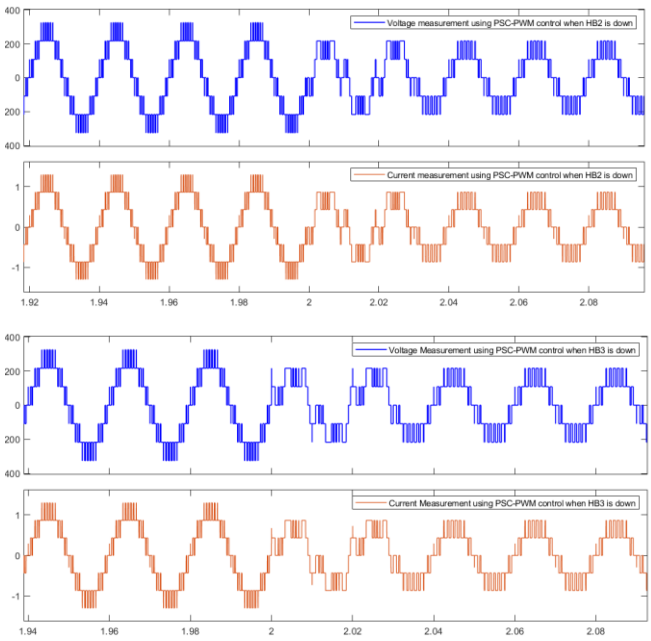


Figure 10. Voltage and current output of the CHBMLI when one DC cells are shutdown

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Figure 10 shows all possible corrections when one cell's voltage input is shutdown, and how the phase shift control influences the inverter's output.

As seen in *figure 10*, after one DC input is lost, the voltage and current output are disfigured and doesn't sync with the original Phase shift configuration. The original switching pattern continues for a certain time while the controller detects the error, after which, the phase shift is altered according to the number of available healthy cells.

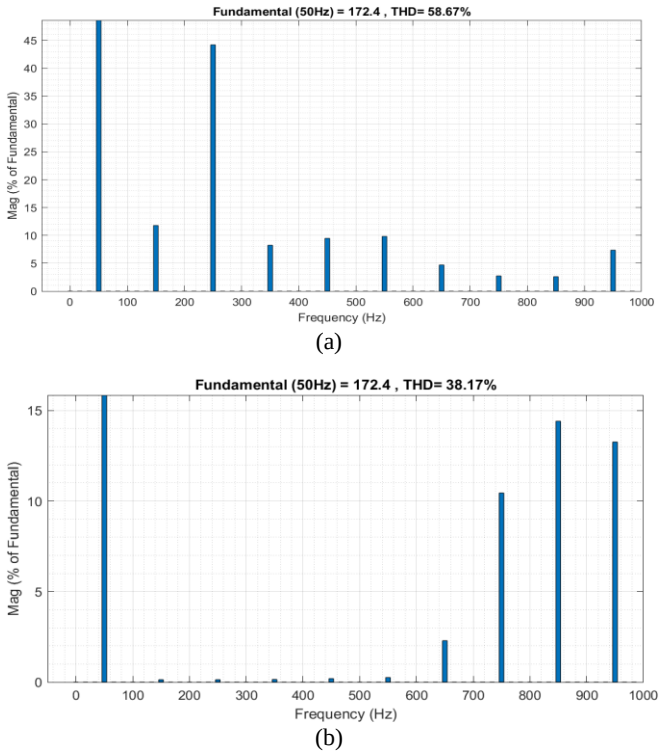

Figure 11. THD when voltage input of cell HB2 is off during the diagnosis window (a) and after the readjustment (b)

For instance, during normal working, the THD of the voltage output is approximately 24.35 %, when HB2 cell's input (V_{DC1}) is shut down, this THD increases to 58.67 % owing to the previously mentioned reasons. In this situation, the proposed control strategy consists of bypassing cell HB2 by short-circuiting the switches S_{21} / S_{23}, opening switches S_{22}/S_{24} and altering the phase-shift of the switches $S_{11}/S_{12}/S_{13}/S_{14}/S_{31}/S_{32}/S_{33}/S_{34}$. As a result, the voltage and current waveforms are readjusted and the voltage THD drops down to 38.17 % thus producing a far better output. *Figure 11* shows the FFT analysis of the voltage output before and after the correction.

The proposed control scheme ensures the best adjustment even if multiple DC inputs are lost. For example, if two DC sources are shut down, the proposed scheme changes automatically the number of levels to 3 levels instead of 5. If the MLI has already transited to 5 levels and loses another DC source it changes to 3 levels mode as well. *Figure 12* shows the voltage and current output when more than one DC cell have their voltage input shutdown then corrected using the proposed control scheme.

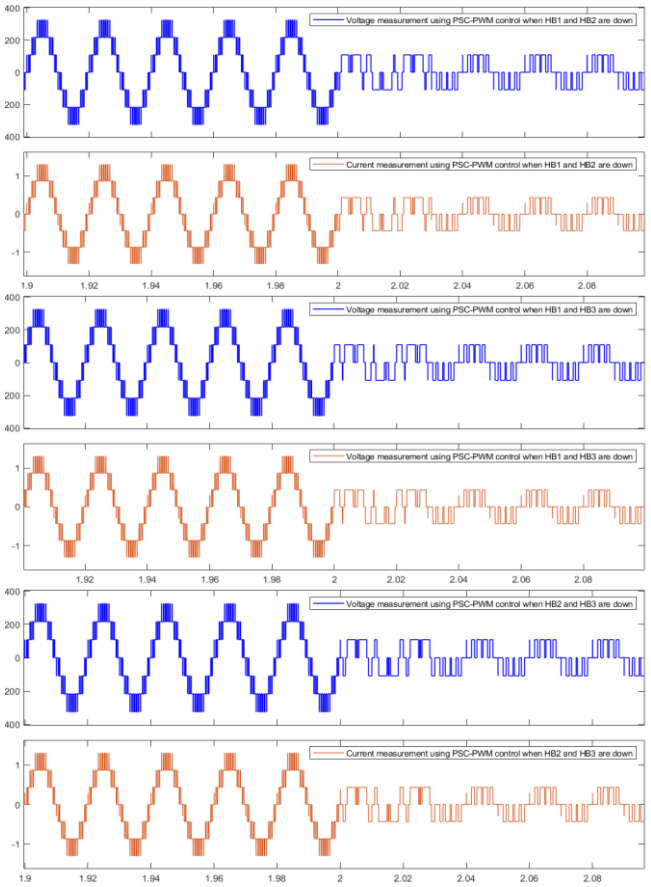

Figure 12. Voltage and current output of the CHBMLI when 2 DC cells are shutdown

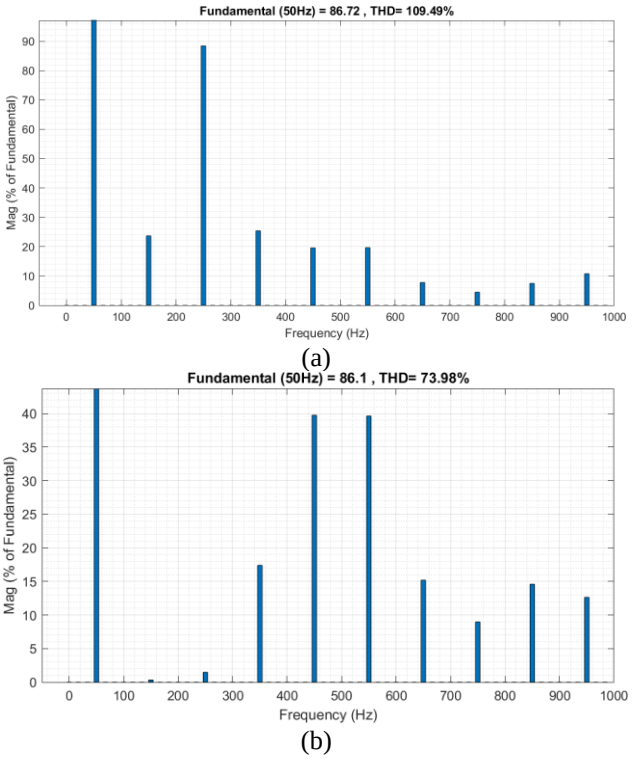

Figure 13. THD when voltage input of cell HB2 is off during the diagnosis window (a) and after the readjustment (b)

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Compared to existing works [18 – 22] it can be seen that no additional components were added in order to bypass the DC source that were shut down. In ref [17] for example, the number of combinations that are involved in bypassing a fault are complicated thus difficult on application level. The present converter changes the level but doesn't require any additional change in the SPWM command except the phase shift value.

As illustrated in *figure 12*, when both DC inputs connected to $HB1$ and $HB2$ are shut down, the voltage levels related to the firing angles θ_1 and θ_2 are missing which results in the signal output recoded during the diagnosis time. After detecting the fault issue, the switches labeled S_{11} / S_{13} in the first cell and S_{21} / S_{23} in the second cell are short-circuited. The switches S_{12}/S_{14} in the first cell and S_{22}/S_{24} in the second cell are opened permanently, meanwhile the rest of the switches $S_{31}/S_{32}/S_{33}/S_{34}$ in the third cell continue to operate according to a set of two-phase shifts.

Figure 13 shows the recorded THD level during the fault incident and after the correction. In the original scheme, the control generates four phase shifts with a resulting in 8 carriers which heavily disfigure the voltage output when the two first cells are note operating correctly resulting in a 109.49 % THD. After the readjustment, only the switches of the third cell are controlled which makes the THD drops to 73.98 %.

Table 5: THD of the voltage output for different states of the 7 levels CHBMLI using the correction scheme

State	Cell HB_1 voltage (V)	Cell HB_2 voltage (V)	Cell HB_3 voltage (V)	THD (%)
State 1	108.4	108.4	108.4	24.35
State 2	108.4	108.4	0	38.17
State 3	108.4	0	108.4	38.16
State 4	0	108.4	108.4	38.18
State 5	108.4	0	0	73.97
State 6	0	0	108.4	73.92
State 7	0	108.4	0	74.01

Table 5 summarizes the recorded THD when the fault correction is applied. It is noteworthy to indicate that the states indexes used in *table 5* are the same as those used in *table 4*. This technical feature was most important to appraise the amelioration provided by the correction scheme.

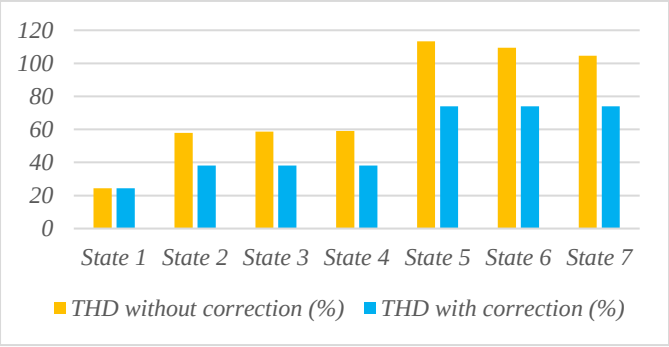

Figure 14. Performance of the CHBMLI under fault conditions with and without the fault tolerance scheme

Figure 16 gives a summarized comparison between the case where the CHBMLI operates without correction and the case where the Fault tolerant strategy is used.

The graphical assessment in *figure 16* clearly shows how the fault tolerance scheme optimizes the THD content after a fault incident on the DC input feed. Compared to existing works, few research papers consider the cases where multiple DC input are at jeopardy [16]. The proposed architecture is capable of reducing the number of levels by bypassing even multiple cells. This is done solely using correct phase shift alteration in the SPWM command.

6. CONCLUSION

In this paper, in order to overcome potential shutdowns in the DC input of symmetric cascaded H-Bridge multilevel inverters, a fault tolerant structure is proposed. The present study fills the gap regarding the use of classic architecture equipped with fault tolerant capacity toward DC input loss. The proposed structure is based on changing the operating level of the inverter when a DC input is shut down without structural modification. The alteration of the configured level is based on properly bypassing the faulty cells. This goes through the correct adaptation of the phase shifts, short-circuiting the top switches and opening the lower switches of each faulty cell. The paper gives a state-of-the-art situation of the fault diagnosis and tolerance in multilevel inverter. Furthermore, a detailed analysis of the cascaded H-Bridge multilevel inverter before fault occurrence, during the fault diagnosis window and after the level alteration is presented using simulation tools. With attention to output quality, a record of the THD and staircase waveform is analyzed under different conditions regarding faults and transitions. Results show that there is a big improvement of voltage and current waveform with lower THD and better possibility for AC/AC conversion. It is noteworthy that the proposed scheme allows the multilevel inverter to reduce maximum number of levels that can be generated when a fault occurs, but also can reestablish the original operating when the DC input is reconnected. The proposed strategy ensures that the connected load receives a proper voltage and current outputs, thus, preventing any permanent damage. These results strongly contribute to the evolution of classic multilevel architectures toward tolerance capability regarding DC inputs loss. Such methodology offers a strong, yet simple way to avoid damages that may be inflicted to connected loads. Despite the fact that the current study didn't investigate the case where unequal DC sources are used, this will be one of the main features that will be analyzed in upcoming works. Additionally, scenarios where the fault occur on switches as open or short-circuit event will be addressed, and a prototype of the studied multilevel inverter will be manufactured.

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