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A New Quazi Z-Source Seven-Level inverter for Photovoltaic Applications

Ajjanna Mulakaledu[1], Chintam Jagadeeswar Reddy[2 *], Y Kamal Kishore[3], Vinod Bakka[4], Botta Kusuma Kumari[5] and Busireddy Hemanth Kumar[6]

[1]*Koneru Lakshmaiah Education Foundation, Vaddeswaram, A.P, India; ajjilecturer@gmail.com*
[2]*PACE Institute of Technology & Sciences (Autonomous), Ongole, Andhra Pradesh-523272, India; drcjdsreddy.1990@gmail.com*
[3]*Ballari Institute of technology and management, Ballari, Karnataka, India; kamalyaranagula@gmail.com*
[4]*Koneru Lakshmaiah Education Foundation, Vaddeswaram, A.P, India; vinodbakka@kluniversity.in*
[5]*Gayathri Vidhya Parishad college of engineering for women, Madhurawada, A.P, India; kusuma.kala@gvpcew.ac.in*
[6]*Mohan Babu University (Erstwhile Sree Vidyanikethan Engineering College), Tirupati, A.P, India; hemub09@gmail.com*

***Correspondence:** Chintam Jagadeeswar Reddy; *drcjdsreddy.1990@gmail.com*

ABSTRACT- This work presents a Quazi Z-Source Seven-Level inverter (qZS7LI) for Photovoltaic (PV) applications. The presented topology partakes the benefit of having a lesser switch count (8 switches) compared to current 7-Level qZ source topologies. The presented qZS7LI consists of three quasi-Z-source based impedance network, 02 bidirectional power switches, and one H-bridge inverter. The presented qZS7LI topology is studied by using pulse-width modulation (PWM) technique. The bidirectional switches and one leg of the H-bridge inverter are employed to insert shot through and generate levels, operating at a high frequency. The PWM control approach offered, together with the corresponding switching systems for each level of generation, are presented. Both simulation and the experimental results validates the operation of presented qZS7LI. A concise comparison is constructed to emphasize the advantages of the suggested qZS7LI topology in contrast to standard topologies.

Keywords: DC-AC converter, photovoltaic, seven level, Quazi Z-source, harmonic distortion.

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1. INTRODUCTION

Current advances in Z-Source allied converters have resulted in a significant increase in their use in a variety of power electronic (PE) applications, including PV systems, hybrid electric cars, distributed power system, uninterruptible power supply, and others. Classical voltage source and current source inverters often struggle with limited output voltage and dependability; the Z-source inverter solves these issues [1]. Removing the dead zone between the switches improves reliability and lessens waveform distortion. Compared to a 2-stage conversion system, with buck-boost capabilities, it offers single-stage DC-AC power conversion, enhancing efficiency. The shoot-through duty cycle D_O is represented by an increase in the output voltage to that value. Turning on the switches for one or more phases for a time period equal to D_OT completes the shoot-through. In the literature, a number of shoot-through control techniques are discussed [2][3]. DC-DC and DC-AC power conversion are the two most popular uses for Z-source converters [4]. The qZSI, one of the various Z-source derived topologies, is the most often used because it is appropriate for distributed generation and offers constant input current, a reduced capacitance, and a shared DC-rail among source and load [5][6].

In contrast to conventional two-level inverters, multilevel inverters (MLIs) provide many advantages, such as lower harmonic distortion, greater voltage handling capacity, less switching losses, and the capacity to use low-voltage, rapid semiconductor switches [7]. In addition to the well-known MLI topologies, several other topologies have been designed to tackle problems including control complexity, capacitor voltage balance, and the number of switches. In this category, you'll find topologies like Cascaded H-Bridge (CHB), Neutral Point Clamped (NPC), and Flying Capacitor (FC). Additionally, efforts are being made to modify MLI for use with low voltage and power applications so that it may be integrated with distributed energy sources that operate on low voltage. On the other hand, MLI's poor output voltage gain is a major drawback. One way to overcome this limitation is by combining MLI with high-quality power conditioners that can increase the output voltage gain. Various DC-AC topologies and pulse width modulation (PWM) methods for DC-AC inverter control have been detailed in published works [8]– [14].

The family of Z-source-based MLI has been expanded to include several topologies in this context. The shoot-through must be fitted correctly, however, so that the average voltage output doesn't fluctuate. The study in question introduces a single-phase 3L-NPC converter that makes use of a grounded

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neutral point, 02 Z-source networks, and 02 sources [15]. A one DC source, one Z-source networks and 3-ph systems were later added to this design. A diode clamped Z-source inverter, which provides five levels of output, extends this idea. The problem with these topologies is that they are all susceptible to discontinuous input current. In a three-tiered system, in [16], the authors detail their work on a double qZs network design that supports a single-phase NPC qZSI. An LC-switched three-level NPC inverter with fewer passive components is shown in [17] for use in low- and medium-power applications. Three Z-source networks with a cascaded half-bridge inverter with a lowest number of switches are shown in a seven-level inverter in [18]. The voltage gain may be increased by including a connected inductor network with a switching inductor cell into the qZSI architecture, a new cascaded five-level inverter based on qZs is created, as described in [19]. A PV application with seven levels of operation has been reported using the qZSI in grouping with the CHB. According to [21], a five-level boost inverter is shown by means of a decreased passive component and two quasi-switched boost networks. Improved single-phase qZSI-based MLIs that achieve better output quality than traditional qZSI MLIs are detailed in the study in [22]. The shot-through and voltage-inversion functions are performed by these MLIs only by means of one leg. One further gain-oriented and inductor-light three-level inverter is presented in [23] by the developers of the aforementioned single-phase modified hybrid qZSI. The following is a synopsis of some MLIs derived from Z-sources: [24]. Based on what we can tell from the literature, the vast majority of Z-source based MLIs are really combinations of several standard MLI topologies with Z-source based networks. This allows for better voltage regulation, more control flexibility, higher output voltage and current, more reliability, and compatibility with low-energy, distributed energy sources. This work is aimed to propose a Quazi Z-Source Seven-Level inverter (qZS7LI) for photovoltaic applications. This topology has fewer switches than the existing qZs 7-Level inverters.

2. PROPOSED QUAZI Z-SOURCE SEVEN-LEVEL INVERTER (QZS7LI) TOPOLOGY

The recommended configuration, qZS7LI, is shown in *figure 1*. It comprises a seven-level T-type inverter and a cascade of qZs-based impedance networks. 02 inductors (L_1 and L_2) and 02 capacitors (C_1 and C_2) make up each qZs network's fundamental front-end unit. Included in the system's eight switches are two line-frequency H-bridge switches (S_3 and S_4). For shoot-through addition in each Z- network, high-frequency switches S_1 and S_2 are used. To obtain voltage levels, the H-bridge and the qZs networks are connected by two bidirectional switches, S_5, S_6 and (S_7, S_8). Three independent direct current sources—which may or may not be the same—are necessary. Maintaining a consistent peak dc-link voltage throughout all qZs networks, despite variations in input voltages, is necessary to provide a symmetrical seven-level output. There is a certain amount of the output voltage levels that are determined by the amount of fundamental units. The configuration works even with asymmetric voltages, as the shoot-through of each qZS can be controlled independently.

When the output voltage is in its positive half cycle, the switch S_4 remains on for all switching states, whereas the switch S_3 remains on for all switching states during the negative half cycle. Assume that every qZ source network is an elementary unit, with three qZ source. The switching states for the voltage level are stated as follows:

Switching state-1 activates the H-bridge's switch S_4, switch S_7, and body diode S_8 to provide an output voltage of $+V_{DC}$. Here, qZ source -I is active, whereas the other two are inactive, and output voltage equals qZs-I's dc link voltage. *Figure 2(a)* shows the present path and operation of switching state-1.

In *switching state-2*, the H-bridge's switch S_4, switch S_5, and body diode S_6 are in conduction to generate an output of $+2V_{DC}$. In this case, qZ source -I and qZ source -II are active, whereas qZ source -III is zero. *Figure 2(b)* depicts the current conduction route for switching state 2.

Switching state-3 activates the H-bridge switches S_1 and S_4 to provide an output voltage of $+3V_{DC}$. All qZs networks are currently operating. *Figure 2(c)* depicts the present switching process for state 3.

Switching state-4 activates the H-bridge switches S_2 and S_4 to provide zero output voltage. In this case, all qZs networks are in a zero state. *Figure 2(d)* depicts how switching state-4 works.

In *switching state 5*, the H-bridge's switch S_3, switch S_6, and body diode S_5 are in conduction to generate an output voltage of $-V_{DC}$. The qZ source -III is in an active state, although the additional two networks are in a zero state. *Figure 2(e)* depicts the current conduction route for switching state 5.

In *switching state-6*, the H-bridge's switch S_3, switch S_8, and body diode S_7 are in conduction, resulting in an output voltage of $-2V_{DC}$. In this case, qZ source -II and qZ source -III are active, whereas qZ source -I is at zero. *Figure 2(f)* depicts how switching state 6 works.

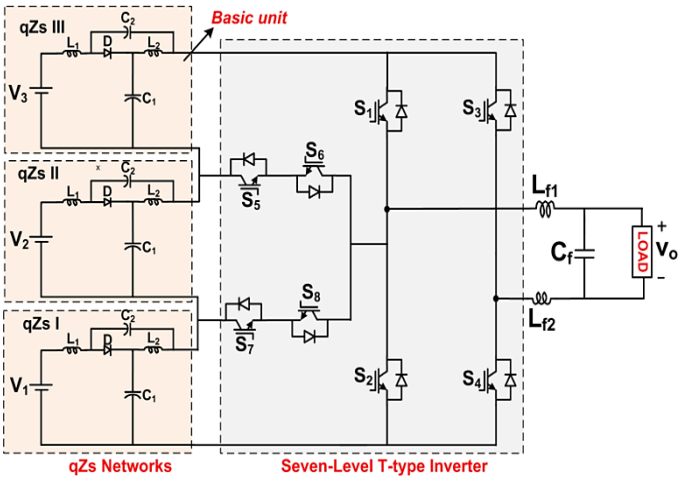

Figure1. Proposed Quazi Z-Source Seven-Level inverter

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Switching state-7 involves the conduction of switches S_3 and S_2 in the H-bridge to provide an output voltage of $-3V_{DC}$. The whole qZ source networks are now functioning. *Figure 2(g)* depicts how switching state-7 works.

Switching state-8: The zero-output voltage is provided by the H-bridge's switches S_3 and S_1, which are in conduction. In this case, every qZ source network is at zero. *Figure 2(h)* depicts how switching state-8 works.

Table 1: Switching states and the corresponding output voltage levels

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V_O
0	0	0	1	0	0	1	0	$+V_{DC}$
0	0	0	1	1	0	0	0	$+2V_{DC}$
1	0	0	1	0	0	0	0	$+3V_{DC}$
0	1	0	1	0	0	0	0	0
1	0	1	0	0	0	0	0	0
0	0	1	0	0	1	0	0	$-V_{DC}$
0	0	1	0	0	1	0	1	$-2V_{DC}$
1	0	1	0	0	1	0	0	$-3V_{DC}$

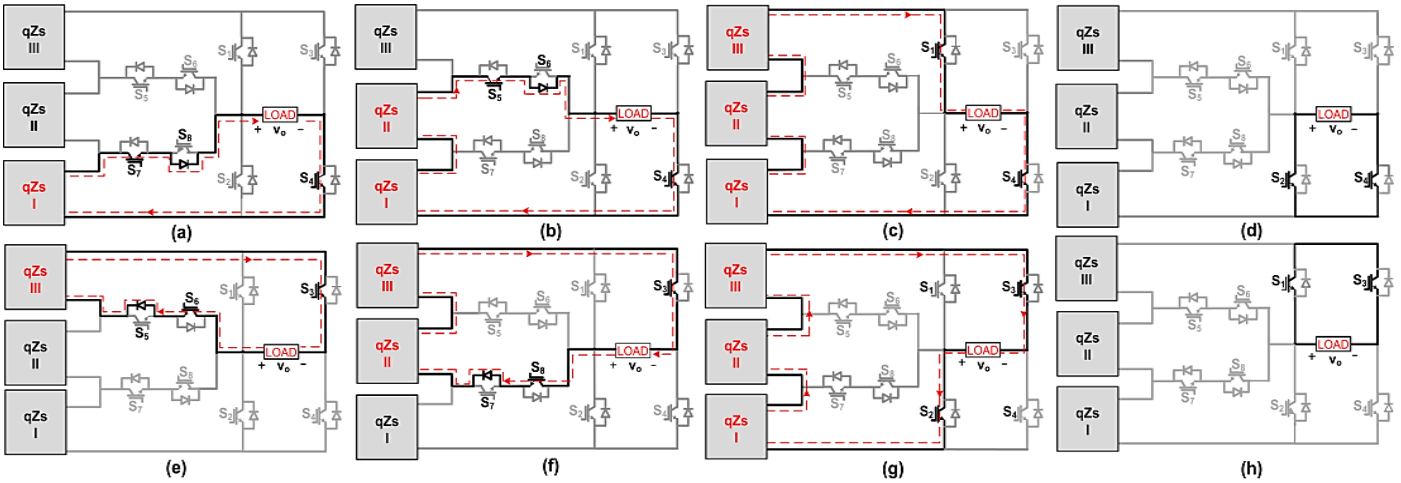

Figure 2. All Switching states (SS) of qZS7LI (a) SS-1; (b) SS-2; (c) SS-3; (d) SS-4; (e) SS-5; (f) SS-6; (g) SS-7; (h) SS-8

3. RESULTS AND DISCUSSIONS

Table 2: Circuit parameters

Parameter/Component	Attributes
Input Voltage range	40V-50V
Inductors	1mH
Output Voltage	110 V_{rms}
Capacitors	1000µF
LCL Filter	4mH, 1µF
Switching Frequency	10kHz
RL load	80 Ω, 10mH
Fundamental Frequency	50Hz

The theoretical research and working concept of the suggested arrangement are simulated using MATLAB program. Level-shifted Sinusoidal Pulse width modulation technique is employed for generation of control pulses to power switches. For better verification, the experimental and simulation runs are performed under similar conditions, following the parameters given in *table 2*. To obtain a 110Vrms output, all qZ source networks are operated with RL load of 80 Ω, 10mH and an input voltage of 40V with a 0.2 shoot-through duty cycle. The proposed inverter performance has evaluated through simulation and experimentation at a power rating of 250 W. The input voltage & current and the DC link voltage of the qZ source-I network during a 4-millisecond period are shown in *figures 3(a)* and *3(b)*, respectively, as simulated and experimental waveforms. The figure is also presented in a zoomed form. While in shoot-through mode the input current increases linearly, it drops while in active state. The shoot-through condition is characterized by pulses in the dc-link voltage across qZ source-I; however, when in the zero state, it remains stable. At steady state, the capacitor voltages V_{C1} and V_{C2} of the qZ source-II network, which are increased to about 58V and 18V, respectively are shown in *figures 4 (a)* and *4(b)*, are essentially constant. The actual and virtual waveforms of the inverter's filtered output voltage, output current, and voltage are shown in *figures 5(a)* and *5(b)*. During voltage level switching, the inverter's output voltage drops to V_{C1} from (V_{C1}+V_{C2}) instead. The size of the filter is somewhat increased as a consequence of this. The output current, filtered output voltage, and inverter output voltage are shown in *figure 6* together with their corresponding experimental and computed FFT spectra. The LCL Filter lowers the inverter's output voltage by reducing switching harmonics. The efficiency for the proposed inverter is better (around 92 %) due to lower switch count when compared to other existing topologies. The efficiency is

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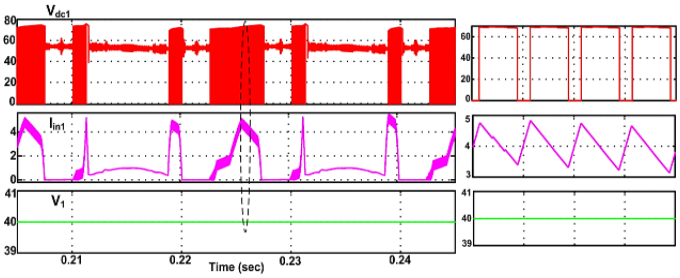
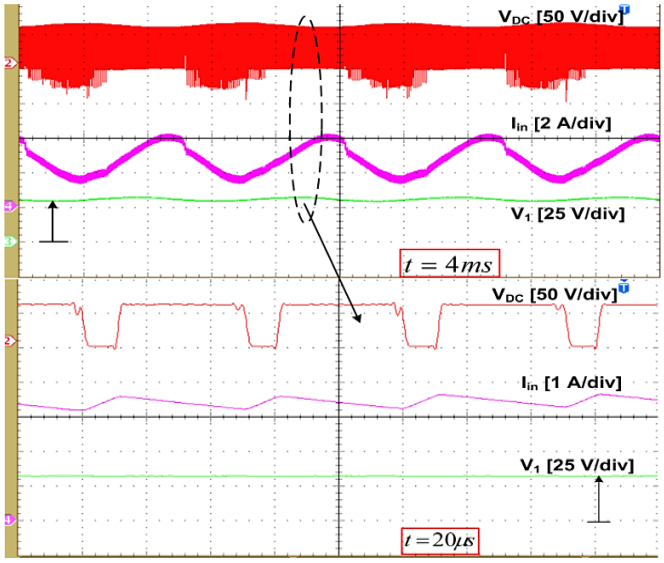
computed using Thermal Module in PSIM software. However, the efficiency of any configuration also depends on the type of switch selection, total blocking voltage and number of passive components and duty cycle. In General, the efficiency will be better at lower duty cycle due to reduced input current. Therefore, the efficiencies of different configurations cannot be compared.

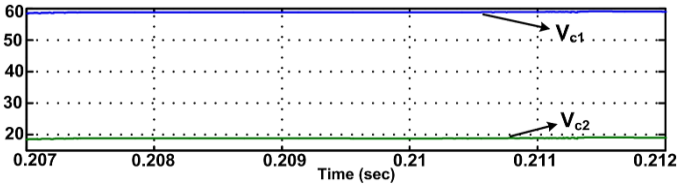


(a)

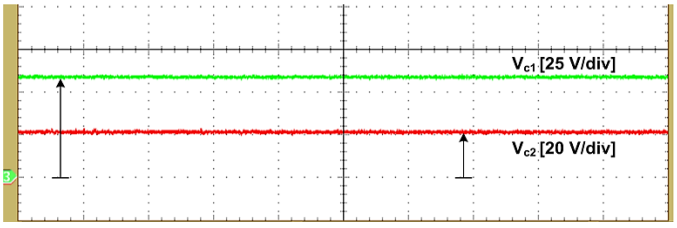


(b)

Figure 3. waveforms of the input voltage, input current, and DC link voltage in (a) simulation and (b) experiment

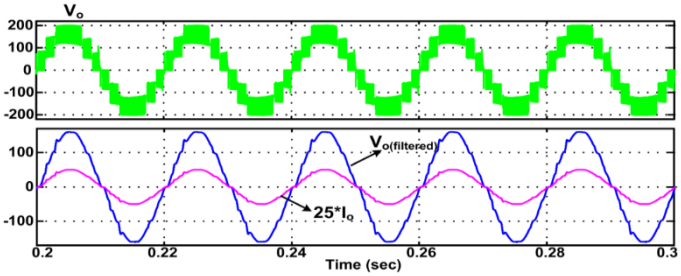


(a)

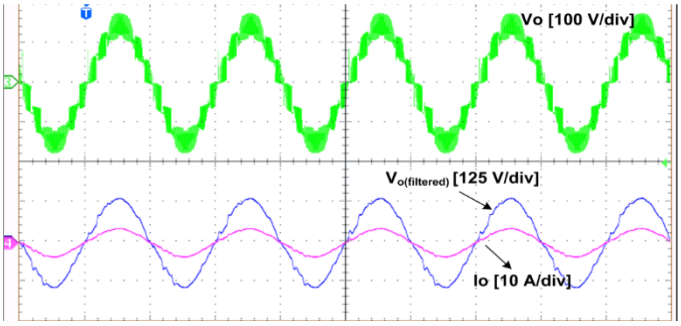


(b)

Figure 4. Waveforms of the capacitor voltages VC1 and VC2 in (a) simulation and (b) experimentation

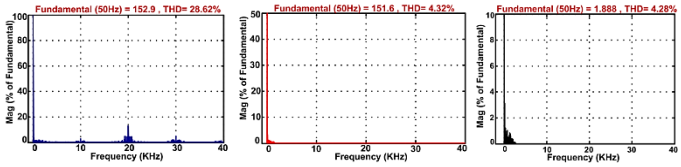


(a)

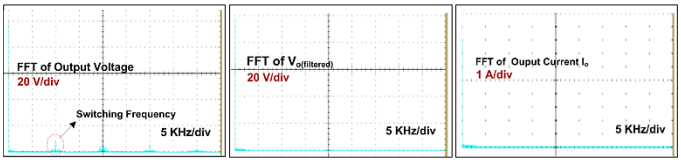


(b)

Figure 5. Capacitor voltage waveforms in (a) simulation and (b) experiments



(a)



(b)

Figure 6. The FFT spectra of output voltage, filtered output voltage and output current (a) Simulation and (b) Experimental

Table 3 compares the number of components needed for the proposed qZS7LI to the analogous 7L 7L transformer-based qZSI [26], 7L Cascaded Half-B qZSI [21] and CHB-qZSI [23]. *Figure 7* shows that the proposed inverter requires fewer switching devices than existing topologies with a higher number of levels. Assume V_{DC} represents the basic unit's peak dc connection voltage. A total blocking voltage of $18V_{DC}$ is achieved by the proposed qZS7LI and cascaded half-B qZSI, surpassing that of the transformer-based qZSI and CHB-qZSI. To provide consistent loss distribution, all switches in CHB-qZSI have a voltage stress of VDC. Due to its single input dc source, the transformer-based qZSI is only suitable for low-power, low-voltage applications. Its passive components are less than those of competing topologies. On the other hand, efficiency is decreased and control complexity is increased by including three HF Transformers.

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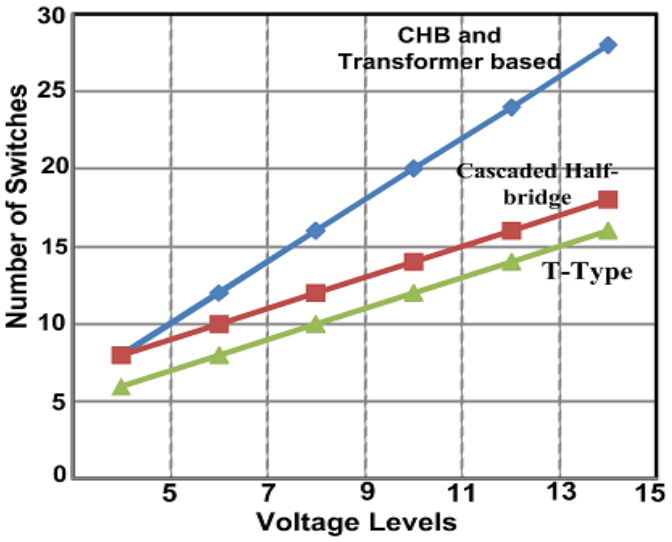

Figure 7. Number of power switches compared to voltage levels

Table 3: Comparing the proposed qZS7LI to the available 7LqZ source-MLI

Parameter	Proposed qZS7LI	Transformer -qZSI [25]	Cascaded Half-Bridge qZSI[21]	CHB-qZSI [23]
Switches	8	12	10	12
Inductors	6	2	6	6
Diodes	3	1	3	3
Capacitors	6	2	6	6
HF Transformer	0	3	0	0
Total Blocking Voltage	18VDC	12VDC	18VDC	12VDC
Input DC sources	3	1	3	3

4. CONCLUSION

A novel quazi Z-Source Seven-Level inverter (qZS7LI) is introduced, with decreased switch count and flexibility. The suitable PWM control systems are used based on shoot-through insertion, with just two switches in use to synthesize any voltage level. The switching stages for shoot-through and output level generation are also described. The qZS7LI performance is studied using simulation and experimental verification with the PWM control strategy has been presented. A concise comparison is constructed to emphasize the advantages of the suggested qZS7LI topology in contrast to standard existing similar 7L-qZ source MLI topologies. The proposed qZS7LI is very well suited for photovoltaic applications.

REFERENCES

[1] Y.P. Siwakoti, F.Z. Peng, F. Blaabjerg, P.C. Loh, and G.E. Town, Impedance source network for electric power conversion –Part I: A topological review, IEEE Trans. on Power Electron., 30(2015)699-716.

[2] F.Z. Peng, Z-Source Inverter, IEEE Trans.on Ind.Appl.,39(2003)504-510.

[3] Y.P. Siwakoti, F.Z. Peng, F. Blaabjerg, P.C. Loh, and G.E. Town, Impedance source network for electric power conversion –Part II: Review of control, IEEE Trans. Power Electron., 30(2015)1887-1907.

[4] P.C. Loh, D.M. Vilathgamuva, Y.S. Lai, G.T. Chua, and Y. Li, Pulse-width modulation of Z-Source inverters, IEEE Trans. Power Electron.,20(2005)1346-1355.

[5] M.K. Nguyen, Y.C. Lim, and Y.G. Kim, TZ-source inverters, IEEE Trans. Ind.Electron., 60(2013)5686-5695.

[6] P.C. Loh, F. Gao and F. Blaabjerg, Embedded Z-source inverters, IEEE Trans.Ind.Appl., 46(2010)256-267.

[7] M.K. Nguyen, Y.C. Lim, Y. H. Chang, and C. J. Moon, Embedded switched-inductor Z-source inverters, Journal of Power Electron., 13(2013)9-19.

[8] B. Hemanth kumar and Makarand M. Lokhande, "Investigation of switching sequences on a generalized SVPWM algorithm for multilevel inverters," Journal of Circuits, Systems and Computers (JCSC), vol.28, no.2, 1950036, Feb 2019

[9] B. Hemanth kumar and Makarand. M Lokhande, "An Enhanced Space Vector PWM for Nine-Level Inverter Employing Single Voltage Source," International Transportations Electrification Conference (ITEC), Pune, India, pp. 1-6, 13th to 15th Dec. 2017.

[10] Kumar, B.H. and Subburaj, V., Integration of RES with MPPT by SVPWM Scheme. Intelligent Renewable Energy Systems, pp.157-178, 2022. https://doi.org/10.1002/9781119786306.ch6.

[11] B. Hemanth Kumar, Makarand M. Lokhande, Raghavendra Reddy Karasani and Vijay B. Borghate. "An Improved Space Vector Pulse Width Modulation for Nine-Level Asymmetric Cascaded H-Bridge Three-Phase Inverter," Arabian Journal for Science and Engineering (AJSE), vol.44, no.3, pp 2453–2465, March 2019.

[12] B. Hemanth Kumar and Makarand. M Lokhande, "Analysis of PWM techniques on Multilevel Cascaded H-Bridge Three Phase Inverter," 2nd International Conference on Recent Developments in Control, Automation & Power Engineering (RDCAPE), Noida, India, pp. 465-470, 26th to 27th Oct. 2017.

[13] B. Hemanth Kumar and Makarand M. Lokhande, "Space Vector Pulse Width Modulation for Multilevel Inverter - A Survey," 4th IEEE International Conference on Convergence of Technology (I2CT), Mangalore, India, pp. 1-6, 27th to 28th Oct. 2018.

[14] F. Gao, P.C. Loh, F. Blaabjerg, R. Teodorescu, and D.M. Vilathgamuwa, Five-level Z-source diode-clamped inverter, IET Power Electron., 3(2010)500-510.

[15] O. Husev, C. Roncero-Clemente, E. Romero-Cadaval, D. Vinnikov, and S. Stepenko, Single Phase three-level neutral-point-clamped quasi-Z source inverter, IET Power Electron.,8(2015) 1-10.

[16] S. Manoranjan, and K. Sivakumar, A Three Level LC-Switching Based Voltage Boost NPC Inverter, IEEE Trans. Ind. Electron., 64(2017)2876-2883.

[17] M.R. Banaei, A.R. Dehghanzadeh, E. Salary, H. Khounjahan, and R. Alizadeh, Z-source-based multilevel inverter with reduction of switches, IET Power Electron., 5(2012)385-392.

[18] E. Babaei, M. S. Zarbil, and M. Sabahi, A New Structure of Quasi-Z-Source-Based Cascaded Multilevel Inverter, Journals of Circuits,Systems and Computers ,26(2017)175203.

[19] D. Sun, B. Ge, X. Yan, D. Bi, H. Zhang, Y. Liu, H. Abu-Rub, L. Ben-Brahim and F.Z. Peng, Modeling, Impedance Design and Efficiency Analysis of Quasi-Z Source Moduel in Cascaded Phtotovoltaic Power System, IEEE Trans. on Ind. Electron., 61(2014)6108-6117.

[20] M.K. Nguyen, and T.T. Tran, Quasi Cascaded H-Bridge Five-Level Boost Inverter, IEEE Trans. Ind. Electron.,64(2017)8525-8533.

[21] O. Husev, R. Strzelecki, F. Blaabjerg, V. chopyk, D. Vinnikov, Novel Family of Single-Phase Modified Impedance-Source Buck-Boost Multilevel Inverters with Reduced Switch Count, IEEE Trans. on Power Electron., 31(2016)7580-7591.

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Electrical and Electronics Research (IJEER)
Research Article | Volume 12, Issue 3 | Pages 756-761 | e-ISSN: 2347-470X

[22] A.V. Ho, and T.W. Chun, Single-Phase Modified Quasi-Z-Source Cascaded Hybrid Five-level Inverter, IEEE Trans. on Ind. Electron. 65(2018)5125-5134.

[23] O. Husev, F. Blaabjerg, C. Roncero-Clemente, E. Romero-Cadaval, D. Vinnikov,Y.P. Siwakoti, and R. Strzelecki, Comparison of Impedance-Source Networks for Two and Multilevel Buck-Boost Inverter Applications, IEEE Trans. on Power Electron., 31(2016)7564-7579.