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A Novel Open-Circuit Fault-Tolerant MMC with Multi-carrier PWM Techniques for Solar PV Applications

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ABSTRACT- Modular multilevel converters (MMC) have attracted much interest from researchers worldwide. It is a desirable solution due to important features such as modularity, low harmonic content at high output voltages, avoiding large capacitors and separate DC sources, easy scaling to any voltage level, and reduced voltage stress on switches, as well as being suitable for high and medium power applications, such as HVDC and motor drives. High-voltage applications require a cascade of hundreds of sub-modules. Depending on the type of sub-module selected for the application, the sub-module of the MMC may contain several switches. Depending on the MMC-based application, the converter typically needs to operate for a long period, two or three years, without interruption. MMCs can experience many electrical problems, including single line-to-ground faults, DC-bus short circuit faults, switch open circuit faults, and short circuits. A malfunction like this can damage the MMC and cause the system voltage to drop. Therefore, a robust fault-tolerant technique needs to be developed. Any fault-tolerant method can be divided into three phases: fault detection and localization, fault bypass mechanisms, and post-fault control. A major emphasis of this work is post-fault control measures to restore pre-fault voltage levels quickly. Our research has the potential to be applied in various high and medium power applications, such as HVDC and motor drives, where the reliability and performance of the power conversion system are crucial.

Keywords: Fault detection, Modular Multilevel converter, Phase Opposition Disposition, Total harmonic Distortion, Photovoltaic.

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1. INTRODUCTION

The area of modular multilevel converters (MMC) has recently gotten a lot of attention from scientists all over the world [1-3]. Modularity, low harmonic content at high output voltages, the absence of bulky capacitors and isolated DC sources, easy scalability at any voltage level, and low voltage stress on power semiconductor switches all contribute to it being a promising solution for high and medium power applications like HVDC and motor drives [3-5].

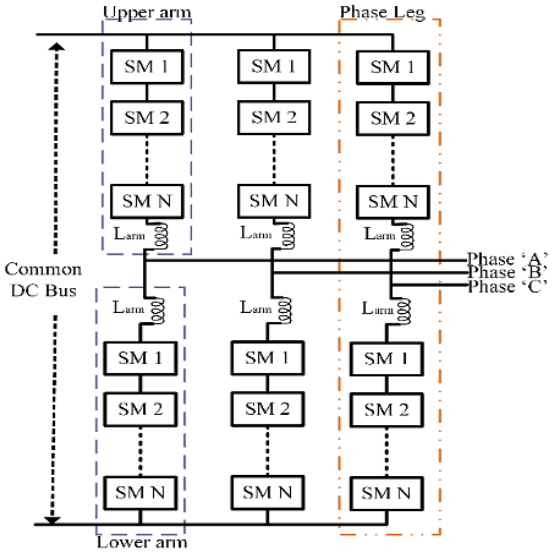

Figure 1. Topology of a three-phase with 'N' sub-modules in each arm of a phase leg.

Key advantages such as scalability, low output voltage THD, and common fault energy make MMC, a multi-cell Voltage source converter, a popular choice for high- and medium-

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voltage drives [6-7]. It improves the adaptability of operations that rely on a single DC supply. Fig. 1 depicts the MMC setup. The MMC leg is connected to the DC source or bus. To cancel out the current flowing through it, an MMC leg has two inductors and two arms, or upper and lower arms [8-9]. The output of a three-phase alternating current is routed through the upper and lower arm's midsection. Each "arm" consists of a cascaded series of "N" "sub-modules" (SMs) that work together to provide the desired amount of output at any given time [10-11]. The common bus voltage and the voltage rating of semiconductor devices enable the number of SMs connected in each arm to be sized.

The application considerably impacts the type of circuit and topology used in the sub-module. Some of the most popular types of sub-modules used include half-bridge, full-bridge, FC, NPC, CHB, and DC sub-module [12-13]. The various configurations of the SMs outlined above are depicted in *figure 2*. Connecting hundreds of sub-modules in series is necessary for high-voltage applications. Sub-modules may have more than one switch, depending on the type of sub-module used [14-15]. Most applications built using MMC technology necessitate the converter to run reliably for several years. A higher number of switches in an MMC system increases the probability of failure, lowering the system's reliability [16-18]. In the future, we must make significant progress in solving the reliability problem.

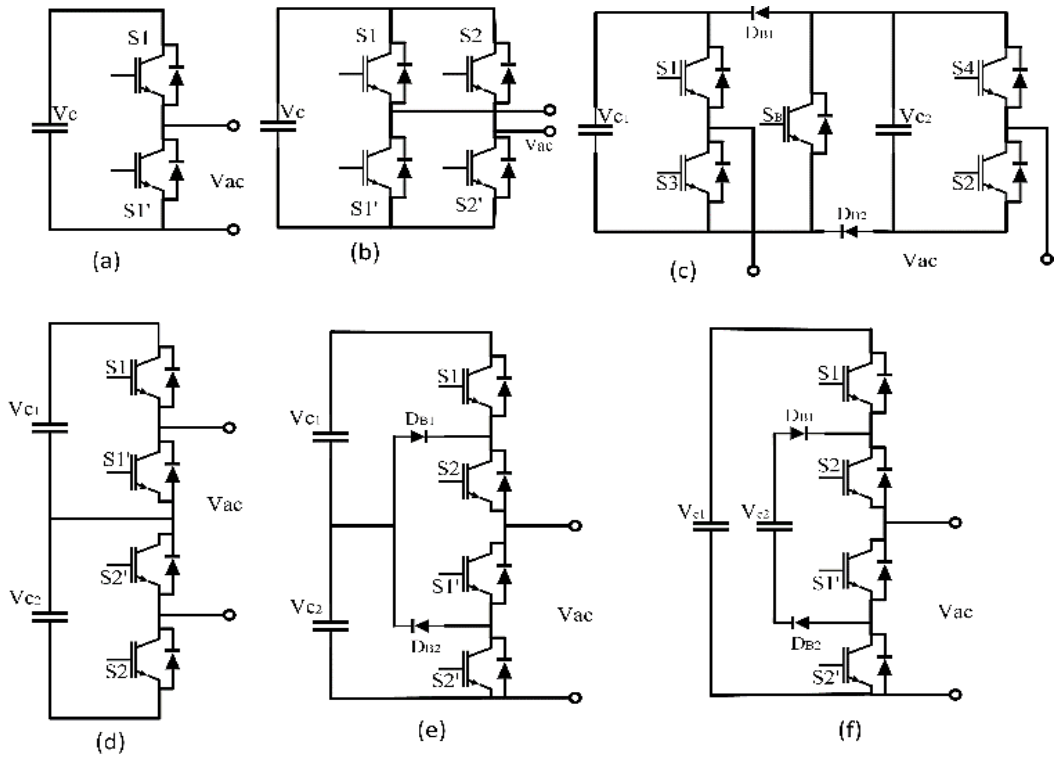

Figure. 2. Commonly used sub-modules (a) Half-Bridge module (b) Full-Bridge module (c) DC module (d) CHB module (e) NPC module (f) FC module

2. TYPES OF FAULTS IN MMC

In general, an MMC will experience four different kinds of faults:

- A faulty DC bus.
- An incorrect AC line to ground.
- A faulty switch.
- A defective switch opens or shorts the circuit.

Brief explanations of each defect are provided below, with an accompanying graphical representation in *figure. 3.*

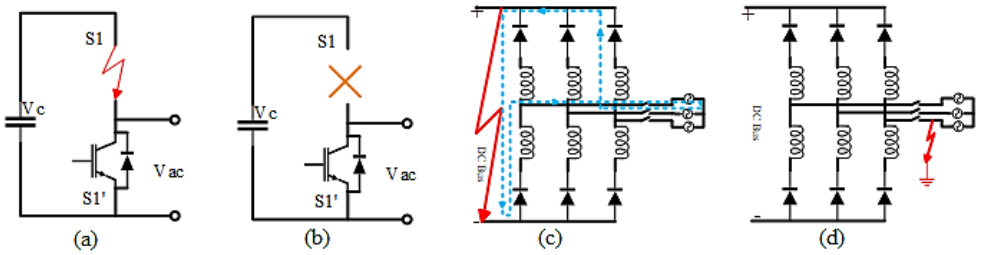

Figure 3. Various faults in MMC (a) Short-circuited switch (b) Open-circuited switch (c) short-circuited DC Bus (d) SLG fault on output side

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2.1. Switch Open circuit faults

To fully grasp the post-fault control procedures, one must first get the causes of open circuit faults. A solid fault-tolerant control system requires a deep understanding of these factors. Many factors, including mechanical or thermal stress, substantial variations in junction temperature, and improper operation of gate driver circuits, can cause genuine circuit faults in solid-state switching devices. Since there are fewer levels in the output voltage when there is a switch malfunction, the voltage and current are diminished. Due to the lack of a discharge route, the capacitor voltage also rises significantly. The capacitor in the sub-module can get fried as a result. As a result, researchers have seen a decline in the MMC system's dependability, which needs to be addressed.

2.2. Switch Short Circuit fault

Several factors, including excessive current, voltage, faulty gate drivers, and excessive switching temperature, contribute to switching short circuit problems in MMC. The normal short circuit withstands the time of the switches and withstands more than 10ms. So, the algorithm to identify switch short circuit failures needs to be quick to react. Whenever the switch's on-state voltage drops falls below the OEM-specified value, an SC fault is identified, and the associated SM circuit is isolated.

2.3. DC Bus Short Circuit fault

The source side of the MMC, the MMC can have a pole-to-pole mark. Capacitors in the sub-modules discharge during a malfunction, adding to the DC current and the arm current. *O* and *E* DC bus/arm causes the switches to be disabled. However, in an unregulated fashion, the DC bus is fed from the AC side grid via anti-parallel diodes of HB-SM. The converter and the motor *lo* in this scenario, the converter and the motor loads would be destroyed by the fault current flowing through the MMC and have a reliable fault ride-through capability.

2.4. Ride-through ground (SLG) faults

The output side of the MMC system is susceptible to SLG problems caused by events such as transformer insulation failure, transmission conductor cracking, etc. This places additional voltage stress on the switches and reduces power transfer capacity, lower voltage/ sags, and in the input side double-line frequency oscillations. Therefore, developing a strategy for detecting SLG faults, isolating them, and then controlling them once a fault has occurred is a crucial topic that needs more research. A drop in system voltage and faulty MMC operation could result from such an error. Because of this, it's critical to work on creating a plan that can withstand failures. There are three phases to any fault-tolerant strategy: identifying the problem, isolating it, and regaining control when the problem has been fixed.

3. MATHEMATICAL MODELING

In this section, the authors look at the modular multilevel converter's mathematical modeling. An equivalent circuit relationship between arm and line quantities is crucial to comprehending the system's behavior under static and dynamic settings. The following are the presumptions made in this evaluation:

(a) The sub-module capacitor is big enough to be treated as a reliable DC power source.
(b) Since there are more SMs in the MMC leg, we may ignore the voltage source's harmonic components.
(c) The characteristics of the several phases' legs are the same.
(d) Capacitor voltage is instantly balanced thanks to the arms' shared sub-modules.
(e) The amplitude of the three-phase voltage is the same, and the three-phase loads are comparable.

To simplify the analysis, each arm of a phase leg with N-SMs is treated as a single equivalent controlled voltage source. When at phase 'x' (*x a, b, c*) of MMC, the currents in the upper and lower arms are defined as follows:

$$i\_ux = i\_x/2 + i\_diffx \ (\ x\&a,b,c) \quad (1)$$

$$i\_lx = -i\_x/2 + i\_diffx \ (\ x\&a,b,c) \quad (2)$$

Where i_diffx in the above equation is the differential current in phase and is given by :

$$i\_diffx = -(i\_ux + i\_lx)/2 = i\_s/3 + i\_cirx(\ x\&a,b,c) \quad (3)$$

Where i_cirx is the circulating current in the phase leg x

The dynamic equations of the upper arm voltage are given by:

$$u\_s/2 + u\_xo - L\_arm\ (di\_ux)/dt - R\_arm\, i\_ux - u\_ux = 0 \quad (4)$$

$$u\_s/2 + u\_xo - L\_arm\ (di\_ux)/dt - R\_arm\, i\_lx - u\_lx = 0 \quad (5)$$

Differentiating the voltages introduced by the lower and upper arm sub-modules yields the AC output voltage. Therefore, it is manageable by adjusting the number of SMs in the arms. The DC-link capacitor's voltage rating can be calculated as follows:

$$U\_c = U\_s/N \quad (6)$$

4. SIMULATED RESULTS

4.1 Single Phase 5L-MMC with Phase shift PWM

The reference wave in this modulation system combines two sinusoidal signals. Sub-modules of the upper arm are based on the negative sinusoidal pulse, while those of the lower arm are based on the positive sinusoidal vibration. It has been proposed that a triangular carrier signal produces gate pulses. For the same number of SM in each leg, the same amount of carrier waves is needed. As a result, we've explored four distinct carrier signals. For the system under examination, the SM count in each arm is 4. Therefore, we phase shift each carrier signal by (360°)/N, or 90°. *Figure 5* depicts the PS-PWM system as well as the resulting waveforms.

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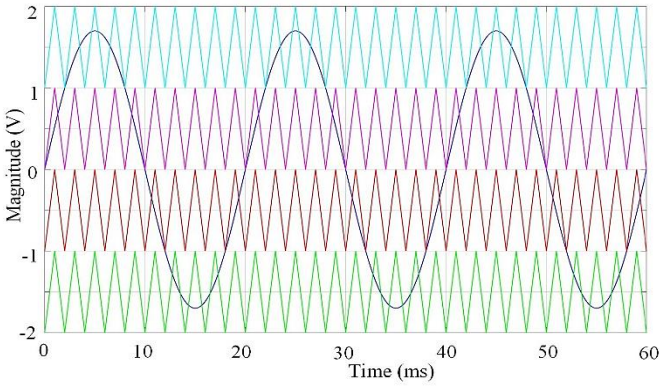

Figure 4. Phase shift PWM scheme for five level – MMC

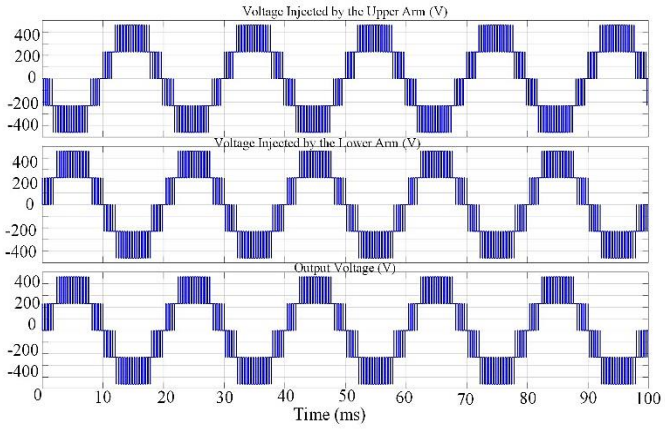

Figure 5. Simulated results of five level-MMC with PS-PWM

4.2. Single Phase 5L-MMC with POD-PWM

When using Phase Opposition Disposition (POD) PWM, the carrier signals are level-shifted in phase with the sinusoidal reference signal, making it a level-shifted PWM system. As seen in *figure 6*, the carrier waves in the lower half of the spectrum are 180 degrees out of phase, concerning those in the higher half. In *figure 7* shows the POD-PWM-obtained waveforms for MMC output.

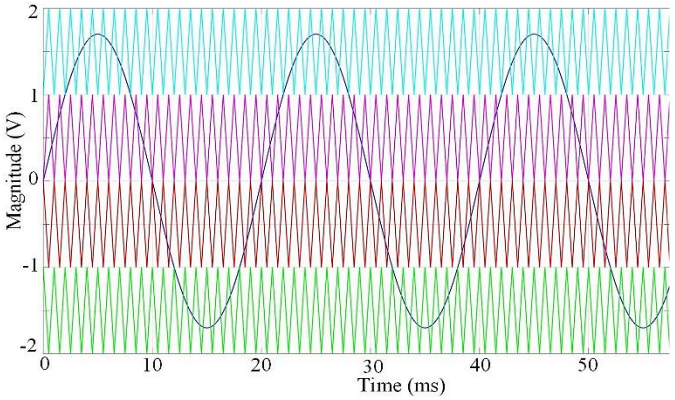

Figure 6. POD-PWM scheme for 5L-MMC

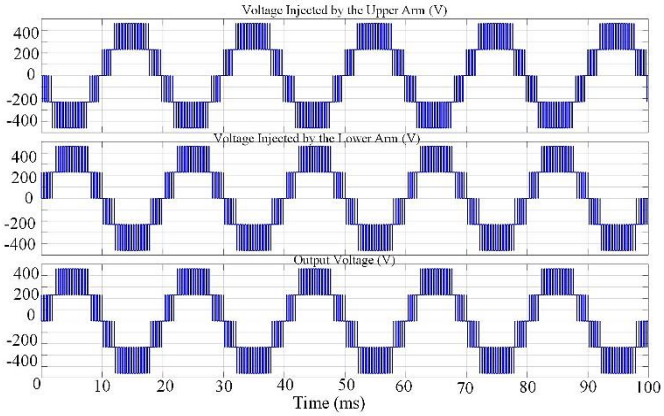

Figure 7. Simulation results of 5L-MMC with POD-PWM

4.3. 5L-MMC with APOD-PWM

Four carrier signals are used for each of the four SMs in an arm, making APOD-PWM a level-shifted PWM approach. The approach diverges from POD-PWM by using a 180-degree phase shift between alternating carrier signals. *Figure 9* depicts the APOD-PWM system and the resulting waveforms.

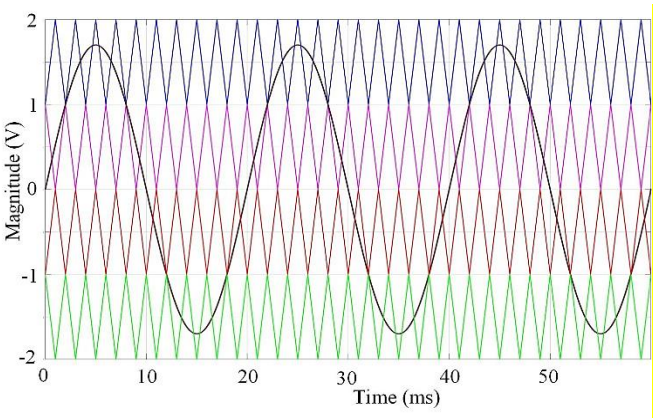

Figure. 8. APOD-PWM scheme for 5L-MMC

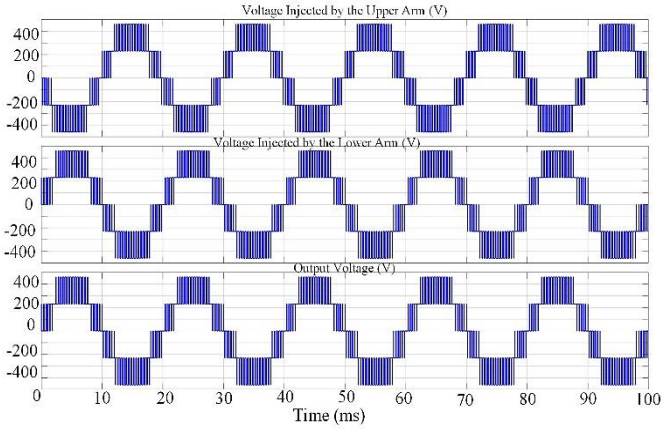

Figure 9. Simulated results of 5L-MMC with APOD-PWM

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4.4. Single phase 5L-MMC with Nearest Level Modulation

The number of SMs to be added to each arm of an NLM is determined so that the voltage produced by an MMC is very close to a sinusoid. We may calculate the required number of SMs by using the formula:

$$N = round\,(\ u\_m/U\_c\ ) \qquad (7)$$

Where U_c is the voltage across the SM capacitor around u_m is the amplitude of the modulation waveform. In *figure 10*, we see the POD-PWM-obtained MMC output waveforms.

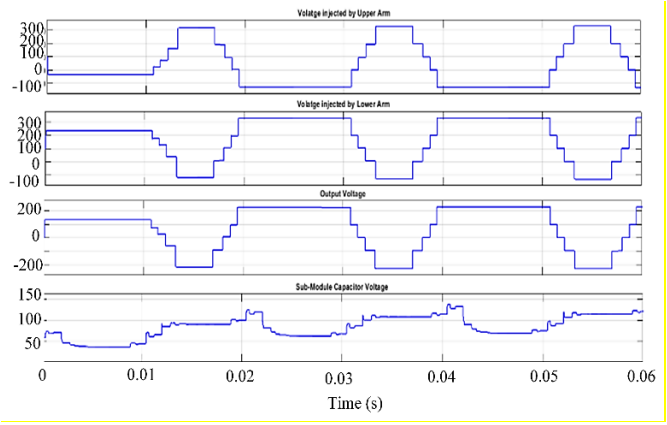

Figure 10. Simulation results of 5L-MMC with NLM-PWM

4.5. Three-phase 9L-MMC with PS-PWM

Figure 11 displays the Simulink model of the three-phase MMC with HBSM. A total of nine distinct voltage levels can be generated from the nine HBSMs that make up each phase leg's four arms.

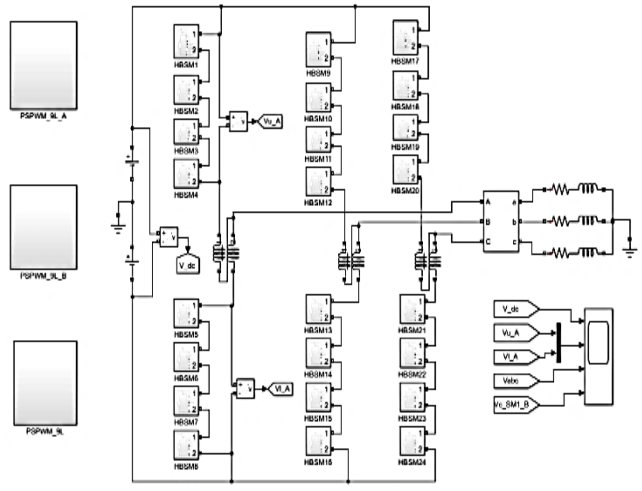

Figure 11. Simulink Model of three-phase HBSM-based MMC

Figure 12 displays the simulation results for a three-phase nine-level MMC using pulse width modulation. The sub-module capacitor voltage variance exceeds the 10% threshold, necessitating a proper capacitor voltage balancing technique and a strong fault-tolerant strategy.

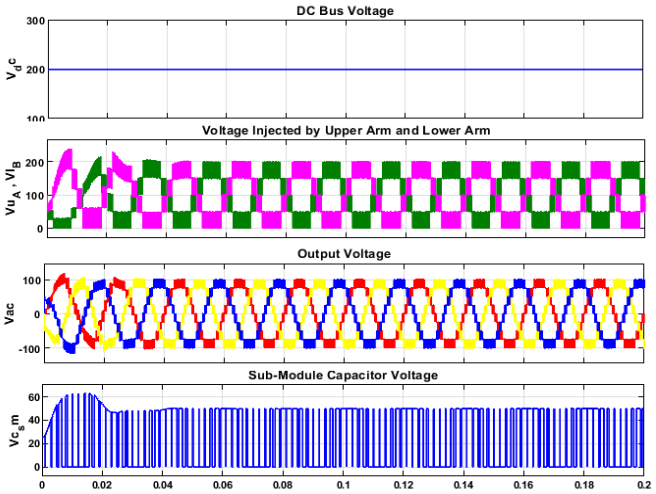

Figure 12. Simulation result of 9-level three-phase MMC with PS-PWM

4.6. Three phase 9L-MMC with PD-PWM

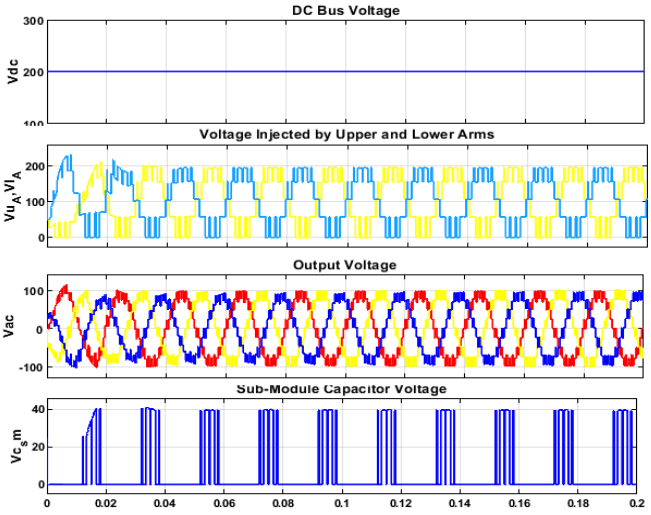

Figure 13. Simulation result of 9-level three-phase MMC with PD-PWM

Figure 13 displays the simulation results for a three-phase nine-level MMC using pulse width modulation. When compared to PS-PWM, the ripple voltage across the capacitor has decreased.

4.7 Fault-Tolerant Analysis

In the S_1 of the upper arm is subjected to OC fault at 0.3 secs. Fig.14 depicts Gate pulses for the switch S_1 from the upper arm. In MATLAB/Simulink, this error is caused by blocking the gate signal to the switches. The number of healthy SMs in the upper arm of the MMC phase leg falls to three, but the number in the lower peninsula of the phase leg remains the same as in the pre-fault state, namely four. As a result, as illustrated in *figure15*, voltage profiles across the upper arm and the lower arm begin to oscillate. As a result of these discrepancies, the output voltage drops following the fault, as seen in *figure 16.* A similar pattern can be seen in *figure 17*, which represents the output current waveform. After t = 0.3secs, the voltage produced by the upper arm begins to decrease.

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When one switch in the series switches is blocked, then the capacitor corresponds to the blocked switch, also isolated from the source. The voltage that actually appears across the blocked switch will be distributed between the remaining switches. The output voltage will be compensated accordingly. The output voltage is first dipped at 0.3 sec, and its profile is slowly recovered and reaches a steady state; the time taken to reach a steady state or original state entirely depends on the load nature. VSC-based HVDC systems are currently using this technology with redundancy. As discussed in the previous chapters the sub-modules can be of half bridge and full bridge. A half bridge is more familiar in VSC-HVDC technology, but a full bridge can be more reliable, but it is a bit expensive because of the greater number of switches. Normally, the cold reserve is 25%, let's say 20 SMs are required per leg, then approximately 25 SMs are incorporated for each leg.

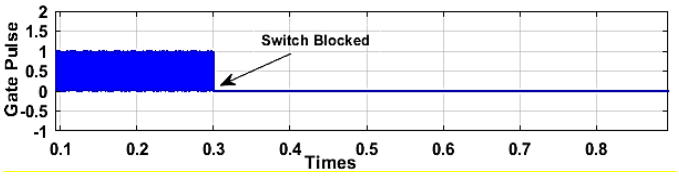

Figure 14. Gate pulses for the switch S1 from the upper arm

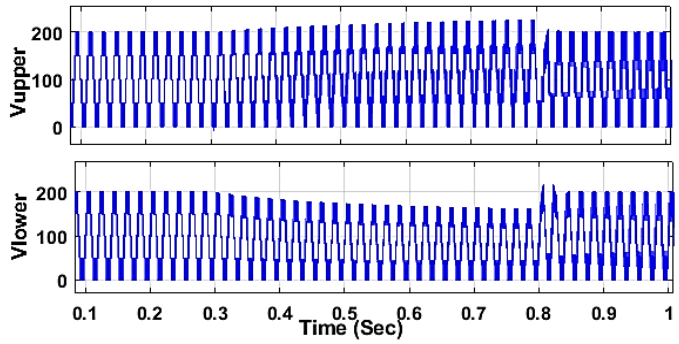

Figure 15. Voltage profiles across upper arm and lower arm

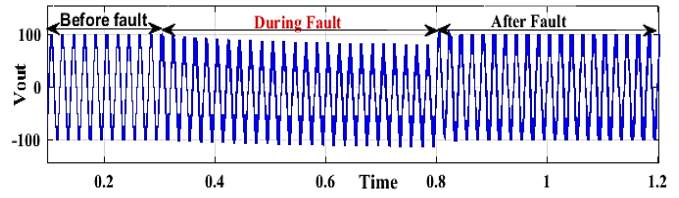

Figure. 16. Nine-level MMC output voltage profile at pre-fault, during fault and post-fault conditions

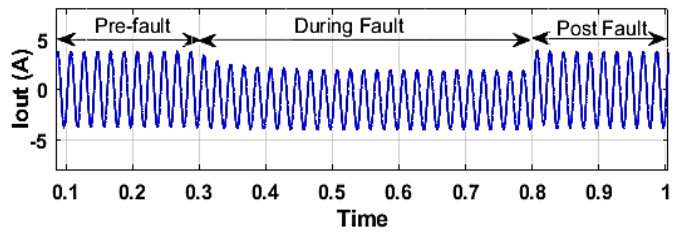

Figure. 17. Nine-level MMC output current profile at pre-fault, during fault and post-fault conditions

4.8. Performance Analysis

Table 1 below shows the output voltage's total harmonic distortion (THD) for several different PWM systems.

Table 1. MMC analysis under different modulation techniques

S.No	No. of Levels	Modulation technique	%THD
1	5	Phase shift	36.75 %
2	5	LS-POD	31.24%
3	5	LS-APOD	40.37%
4	5	LS-NLM	50.28%
5	9	LS-PS	15.29%
6	9	LS-PD	16..33%

From the data in the table above, it is clear that raising the number of discrete levels in the output voltage decreases the THD. Increasing the range of voltages allows for further reduction below the IEEE 519 std—threshold of 5%. POD-PWM was also found to have a reduced THD than alternative PWM systems when applied to 5L MM. When comparing methods, NLM was determined to have the highest THD. It has been found that the THD of the output voltage is greater when using an NLM approach with a low number of SMs [21]. As a result, projects with a greater number of SMs are ideal for the NLM approach. It has been determined that the voltage ripple from the capacitors is more than the acceptable 5%. To keep the MMC in a steady state under all circumstances, it is necessary to employ a control algorithm to equalize the voltage across the sub-module capacitors.

The switching losses of the proposed MMC with over modulation are quite minimal, whereas if grid integration is to be executed, then under modulation has to be considered. In the under modulation, that too in dynamic modulation case, the switching losses will be higher. The conduction losses entirely depend on the operating voltage and load. However, the switching losses and conduction losses of the proposed MMC are quite lesser as compared to classical MLI topologies with the same voltage levels in the output voltage. Here, a fault-tolerant capability can be executed with closed-loop control, and the same is not directly possible with classical MLIs.

5. CONCLUSION

In high-power applications, reliability is crucial. A strong control approach must be employed to restore the pre-fault voltage level after the various faults to improve MMC's dependability and widen its industrial usability. MMC has been compared quickly under several PWM systems like phase shift, POD and APOD techniques. The voltage across each upper leg and lower leg at each control technique is presented. Various fault-tolerant cases possible have been executed in this paper. THD is clearly reduced as the number of discrete levels in the output voltage is increased. As a result, the performance analysis demonstrates that the number of tales in the output voltage decreases as the number of tales increases. Furthermore, when a defective SM is identified, the system activates a redundant SM in the cold reserve (nearly 25%). The output voltage THD is quite minimal as compared with the recent

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literature. Using the MATLAB/Simulink platform, this work simulates the fault-tolerant technique given in this paper. The technician reaches pre-fault voltage levels after an open switch fault in the upper arm of the phase leg.

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