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Analysis of SEPIC Converter at Different Switching Frequencies

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ABSTRACT- Single Ended Primary Inductance Converter (SEPIC) which is commonly devoted as a switched power supply in many applications is presented in this work to conclude the effect of switching frequency on the output voltage time response, elements values, spectral analysis of output voltage and efficiency. For this goal, three circuits of SEPIC converters were designed at switching frequencies of 100KHZ, 400KHZ and 600KHZ. The operating conditions of the three circuits which include input voltage range, output voltage value, output voltage ripple and inductor ripple current are kept the same while the inductors and capacitors of the converters are calculated according to each switching frequency. The LTC1871 controller is utilized to produce a required duty cycle (D) to drive the converter. The implementation of the circuits was carried out using LTspice XVII. The results show that the higher switching leads to better time response of the output voltage with small values of passive components of the converter. However, the efficiency of the converter is decreased and the noise due to harmonics is increased. Therefore, the selection of switching frequency must be set accurately according to converter functions.

Keywords: Fast Fourier transform, Switched Mode Power Supply, DC-DC converter, SEPIC Converter, LT spice XVII Software.

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1. INTRODUCTION

Switched Mode Power Supply (SMPS) is included in many electronic devices and applications such as photovoltaic chargers, renewable distributed generation units and many appliances used in homes [1]. Several advantages might gained of using SMPS over other types of power conversion techniques, for in-stance, they are cheap, efficient and require small size[2]. DC-DC converters are the core of SMPS and the principle of operation of these converters depends on switching mode technique. In other words, the controller of such converters generates a Pulse Width Modulation (PWM) signal at a fixed switching frequency to be applied to the gate of the switch to turn it on and off. Therefore, the first step in designing a dc-dc converter is to choose a suitable switching frequency and that is required to calculate other component such as capacitors, inductors, efficiency…etc. [3].

Several concepts must be considered besides choosing the switching frequency of DC-DC converters. For instance, components values, losses, efficiency and Electromagnetic Interference (EMI), as the currents and voltages of these converters include harmonics which might interfere with other devices or stages [4].

Various topologies of DC-DC converters are utilized in SMPS and each type has its features to meet the load requirements at a specific application. Single Ended Primary Inductance Converter (SEPIC) is a forth order DC-DC converter which includes two capacitors and two inductors can be utilized in SMPS to gain some features over other types, i.e. it is non-inverting, non-pulsating, grounded, inexpensive, and has the ability to step up and step down the load voltage with an acceptable efficiency[5][6].

Many studies and research regarding modelling and analysing SEPIC converter are available in the literature. The radiated EMI and the ripple of output voltage of SEPIC converter are observed by changing the values and types of output capacitor as experimentally obtained in [7]. The results conclude that the EMI requirements to meet FCC standards can be achieved at specific capacitors. However, an LC filter is required with the converter to reduce the ripple according to SAEJ113 standard. In [8], symmetric and soft switching methods are devoted to reduce conducted EMI in SEPIC converters. The results validate the reduction of EMI level using symmetric method and this level might increase using soft switching. The effect of switching frequency with respect to the values of inductor and capacitor in DC-DC boost converter is covered in [9]. The findings approved that the converter size and loss can be reduced by using soft switching at higher frequencies.

Experimental analysis of GaN SC SEPIC converter to study the characteristics of EMI is presented in [10]. The study approved that the voltage between drain and source of the switch is the

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main source of noise. A snubber circuit based SEPIC converter is proposed for EV purposes in [11]. According to the study, a noise reduction is achieved at ringing frequency with the same efficiency. LabVIEW package is devoted in [12] to study the spectral analysis of two types of DC-DC converters. Saving implementation time and accurate results are some recommendations of using such pack-age.

This work presents the effect of switching frequency on the output voltage of SEPIC converter. For this aim, three circuits of SEPIC converters were designed according to three switching frequencies, *i.e.* 100,400 and 600 KHZ. The three circuits operate at the same operation conditions in Continuous Conduction Mode (CCM) to draw a conclusion in such case. These operation conditions include the input voltage range, the output voltage value, and the ripple values of inductor current and output voltage. LTspice XVII software which offered freely by Analog Devices, Inc. is used to implement and analyse the circuits. Additionally, LTC1871 controller is used to sense the output voltage and produce a PWM signal that drive the switch accordingly. The results that recorded and compared include Fast Fourier Transform (FFT) analysis and time response analysis of output voltage, components value of the converter and efficiency in both buck mode and boost mode operation of the converter.

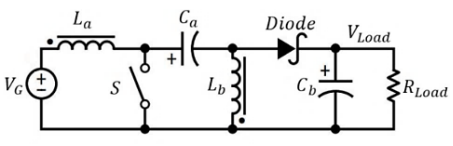
2. MODELLING AND ASSUMPTIONS OF SEPIC CONVERTER OPERATION

This section covers the modelling of SEPIC converter and all required assumptions for the calculation of the element's values

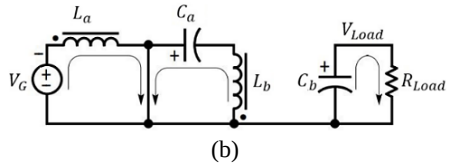
2.1. Modelling of SEPIC Converter

SEPIC converter circuit diagram as shown in *figure 1(a)* includes four storage devices, *i.e.* two capacitors and two inductors in addition to two semiconductor devices, *i.e.* an uncontrolled switch which is usually a Schottky diode (D) and a controlled switch (S) which is IGBT or MOSFET[13][14][15].

Depending on the switch state, as it controlled by a Pulse Width Modulation (PWM) signal at a specific switching frequency (fs), the circuit can be analyzed using circuit theory. The current paths of the converter when the switch is ON and OFF are shown in *figure 1(b)* and *figure 1(c).*



(a)



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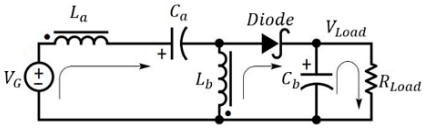

(c)

Figure 1. SEPIC Topology and current flow. (a) SEPIC Converter Topology, (b) current flow during switch on -time, (c) current flow during switch off –time

When the switch (S) is ON, the diode is open circuit as shown in *fig (1-b).* Therefore, the source voltage (V_G) equals to the voltage across the inductor (L_a) and hence:

$$V_G = V_{La} = L_a \frac{di_{La}}{dt} \quad (1)$$

Also, the voltage across the capacitor (Ca) equals to the voltage across the inductor (Lb), therefore

$$V_{Ca} = V_{Lb} = L_b \frac{di_{Lb}}{dt} \quad (2)$$

$$i_{Lb} = -C_a \frac{dV_{Ca}}{dt} \quad (3)$$

And because the voltage across the load (RLoad) and the capacitor (Cb) are the same, in fact they are connected in parallel hence,

$$\frac{V_{Cb}}{R} = -C_b \frac{dV_{Cb}}{dt} \quad (4)$$

In case of the switch (S) is OFF, the diode is short circuit as shown in Fig (1-c) and the equation that describes the source loop is

$$V_G = L_a \frac{di_{La}}{dt} + V_{Ca} + V_{Cb} \quad (5)$$

And the voltage across the capacitor Cb is

$$V_{Cb} = -L_b \frac{di_{Lb}}{dt} \quad (6)$$

While the current through the inductor La is

$$i_{La} = C_a \frac{dV_{Ca}}{dt} \quad (7)$$

Now, the equation that represents the load voltage (the voltage across the capacitor C_b) is

$$\frac{V_{Cb}}{R} = i_{La} + i_{Lb} - C_b \frac{dV_{Cb}}{dt} \quad (8)$$

2.2. Assumptions of Designing SEPIC Converter

The *equation 1* and *equation 8* can be analyzed using volt-second balance [16] approach for one cycle at steady state operation to calculate the voltage conversion ratio, inductors and capacitors values of the converter. If the forward voltage (V_{DF}) of the diode is considered, the duty cycle (D) of the converter expressed as:

$$D = \frac{V_{Load}+V_{DF}}{V_G+V_{Load}+V_{DF}} \quad (9)$$

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In this paper, the LTC1871 controller (*Figure 2*) is used generate a regulated PWM signal at different input voltage values with constant output voltage [17].

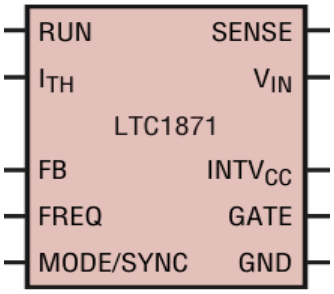

Figure 2. LTC1871 Controller

The switching frequency of the controller (which cover the range of 50 kHz-1MHz) can be adjusted by selecting a required external resistor (R_T) connected to FREQ pin. *figure 3* shows the required (R_T) for a given switching frequency.

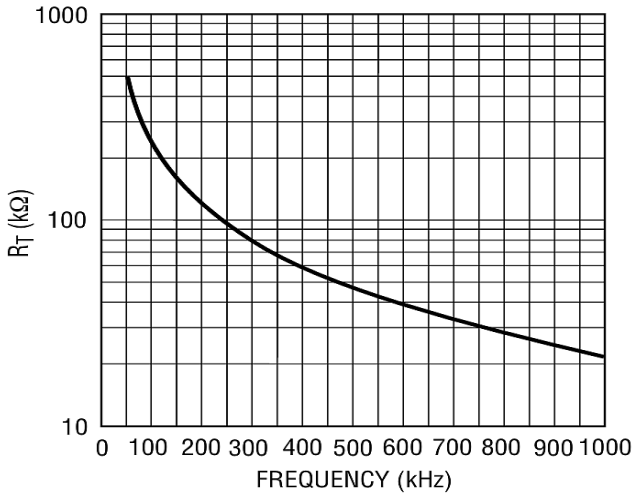

Figure 3. RT - Switching Frequency curve of LTC1871 controller

A fully detailed of SEPIC converter design using LTC1871 controller is presented [17]. According to *equation (9)*, the value of D determines the output voltage that might be at peak value as in *equation 10*.

$$V_{Load\_max} = V_G \frac{D_{max}}{1-D_{max}} + V_{DF} \frac{D_{max}}{1-D_{max}} - V_{DF} \frac{1}{1-D_{max}} \quad (10)$$

The currents in the inductors must be greater than the ripple current (Δi) to force the converter to operate at continuous conduction mode (CCM). Therefore, the peak currents I_{La_max} and I_{Lb_max} of the inductors L_a and L_b respectively can be calculated using *equation 11* and *equation 12*.

$$I_{La\_max} = (1 + \frac{\alpha}{2}) \cdot I_{Load\_max} \cdot \frac{V_{Load} + V_{DF}}{V_{G\_min}} \quad (11)$$

$$I_{Lb\_max} = (1 + \frac{\alpha}{2}) \cdot I_{Load\_max} \cdot \frac{V_{G\_min} + V_{DF}}{V_{G\_min}} \quad (12)$$

Where the value α in *equation 11* and *equation 12* refers to the fractional value of inductors ripple current with respect to peak value of input current which is typically from 20% to 40%.

The two inductors in this article are assumed to be identical [18]with the same ripple current (ΔI_ripple). Practically, a single core is utilized to hold the two inductors in such a case. The values of the inductors are calculated as in *equation 13.*

$$L_a = L_b = \frac{V_{G\_min}}{2 \cdot \Delta I_{ripple} \cdot f_c} \cdot D_{max} \quad (13)$$

The minimum capacitor (C_b) value that limit the voltage ripple (Δv_{ripple}) of 0.01is calculated by *eq.14*, while the choice of (C_a) depends on the source voltage beside the voltage ripple value.

$$C_b \geq \frac{I_{Load\_max}}{0.01 \cdot V_{load} \cdot f_c} \quad (14)$$

3. DESIGN AND IMPLEMENTATION OF SEPIC CONVERTER

The SEPIC converter is designed at three values of switching frequencies; *i.e.* 100KHZ, 400KHZ and 600KHZ in CCM. All three converters must provide an output voltage of 24V to the load of 10Ω.The input voltage range is (10V-30V) which covers both the buck mode and boost mode operation of the converter. The percentage ripple of the output voltage (Δv) and inductors current ripple (ΔIL) are assumed to be (2% & 40%) respectively.

A SEPIC circuit that presented by Linear Technology in [17]was devoted to implement the designed converters using LTC1871. *Table 1* summarize the calculated parameters of the converters at each switching frequency. The design is curried out using LTspice XVII as shown in *figure 4* [19].

The specifications of the selected switches for simulations purpose which are MBRS360 diode (Average Forward current=3A, Breakdown Voltage=60V) and IRF7811 MOSFET (N-channel, Vds=30V, Rds-on=0.0085Ω) of the converter are set using Spice Directives in LTspice XVII software. The values of R1 and R2 are calculated to apply about 1.2V with about (18nA-60nA) on feedback pin of the controller according to electrical characteristics of the controller. Each switching frequency is selected for the operation of the converter by selection the suitable R_T resistor according to the curve shown in *figure 3* and the values as listed in *table 1*. The output capacitor Cout includes two types connected in parallel; *i.e.* electrolytic and ceramic types and the capacitors are represented in *table 1* as Cout1 and Cout2 respectively.

Various measurements such as output voltage time response, spectral analysis of output voltage and efficiency in both buck mode and boost mode in addition to component values are recorded to draw a conclusion of the effect of switching frequency on the operation of SEPIC converter.

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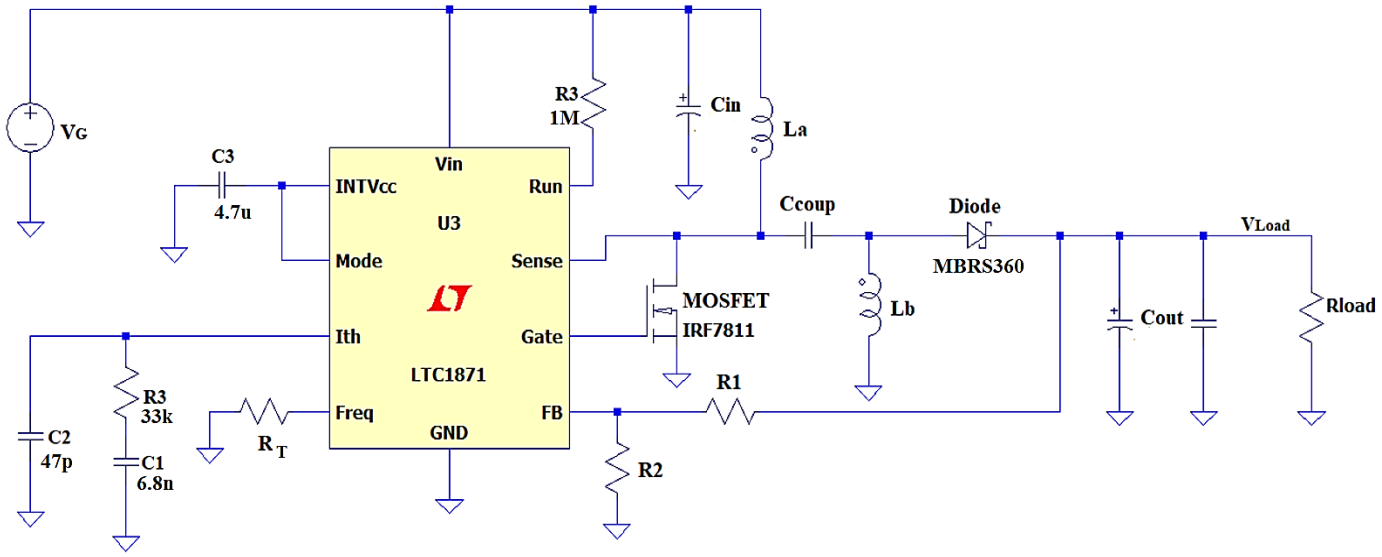

Figure 4. Implementation of SEPIC converter using LTC1871

Table 1. Parameters of SEPIC converter

Parameters/Switching frequency	100 kHz	400 kHz	600 kHz
Input Voltage (VG)	10-30	10-30	10-30
Output Voltage (VLoad)	24	24	24
Cout1(uF)	83.3	20.8	13.88
Cout2(uF)	10	10	10
Cin(uF)	47	47	47
Ccoup(uF)	10	10	10
La(uH)	18	4.5	3
Lb(uH)	18	4.5	3
Rload (Ω)	10	10	10
R_T (kΩ)	240	60	40
R1(kΩ)	200	100	90
R2(kΩ)	10.8	5.4	4.9

4. SIMULATION RESULTS AND DISCUSSION

The validation of the designed SEPIC converter is covered in this section. The converter operates at CCM and must provide a constant output voltage of 24V at the three values of switching frequencies in both modes of operation. FFT analysis which provided by LTspice XVII is used to study the spectra of output voltage of the converter at each switching frequency.

4.1. Buck and Boost Operation of SEPIC Converter

The effect of changing switching frequency on the time response of output voltage is shown in *figure 5* and *figure 6*. It can be concluded that the increase of switching frequency leads to improve the response and reduce the required time to reach the desired output voltage which is 24V in both modes of operation of the converter, for instance, in case of boost mode operation of SEPIC converter when the input voltage is 12V as shown in *fig. 5*, the time ranges of 0.8ms, 0.42ms and 0.38ms at switching frequencies 100KH,400KH and 600KHZ respectively are required to reach the desired output voltage. Similarly, as shown in *figure 6*, the time ranges of 0.55ms, 0.32ms and 0.29ms are required at switching frequencies 100KH,400KH and 600KHZ respectively to reach the output voltage of 24V in case of buck mode operation when the input voltage is 30V.

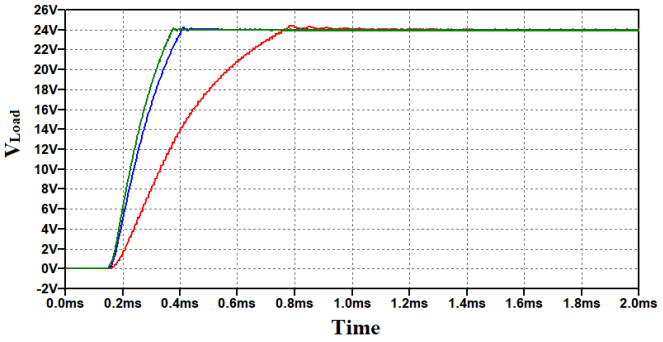

Figure 5. Output voltage time response (VLoad) of the converter at boost mode operation when VG=12V

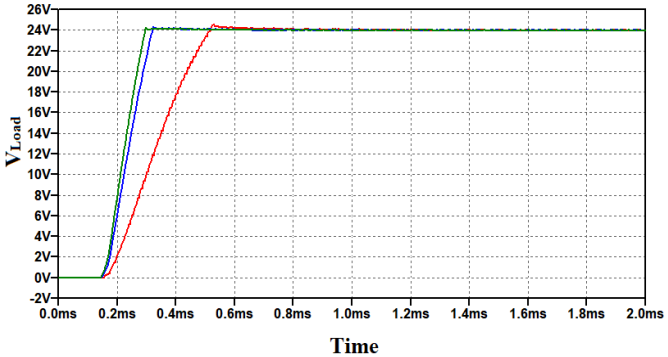

Figure 6. Output voltage time response (VLoad) of the converter at buck mode operation when VG=30V

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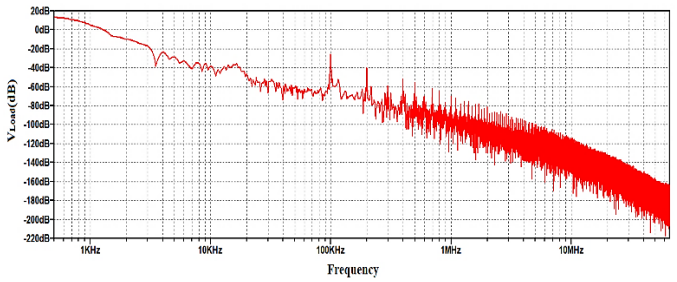
4.2. Spectral of Output Voltage at Boost Mode and Buck Mode of SEPIC Converter

The Fast Fourier Transform (FFT) analysis which is provided by LTspice XVII is used to conclude the effect of switching frequency of the output voltage of the converter at the two modes of operation [20]. For boost mode operation when the input voltage is 12V, the spectral analysis of the output voltage at the switching frequencies of 100KHZ, 400KHZ and 600KHZ is shown in *figure 7(a)*, *figure 7(b)* and *figure 7(c)* respectively. The output voltage includes harmonics of higher order at each switching frequency that must be considered in Electromagnetic interference (EMI) and Electromagnetic Compatibility (EMC) requirements.



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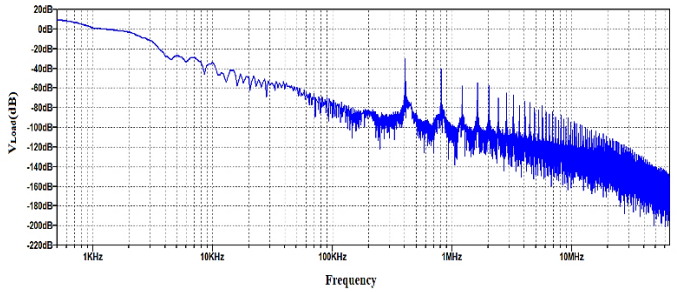

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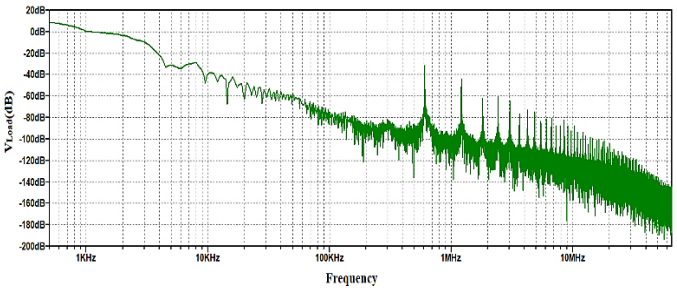


(c)

Figure 7. FFT plots of load voltage (VLoad) in dB when VG=12V at (a) fs=100KHz, (b) fs=400 KHz, (c) fs= 600 KHz

Additionally, the higher the switching frequency selected of the converter, the higher the level of harmonics produced as shown in *figure 8*. For instance, the noise generated by the converter at switching frequency of 600 KHz (Green colour) is higher than the noise generated at switching frequency of 100 KHz (Red colour) over the range of 40MHz to 65MHz.

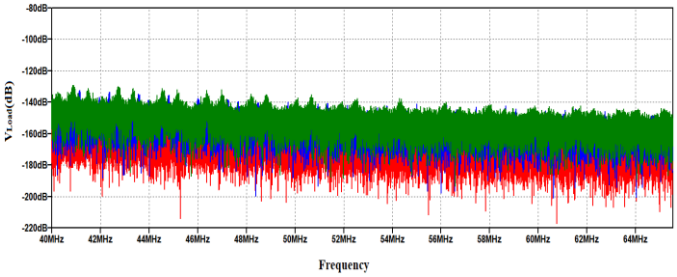
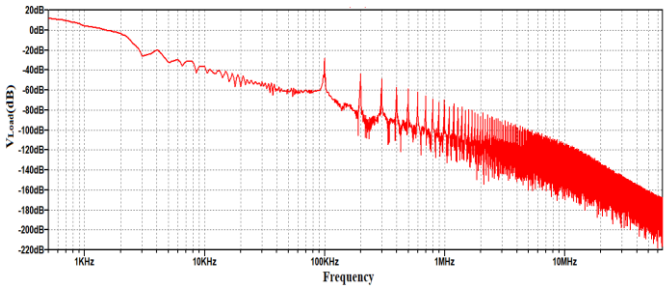
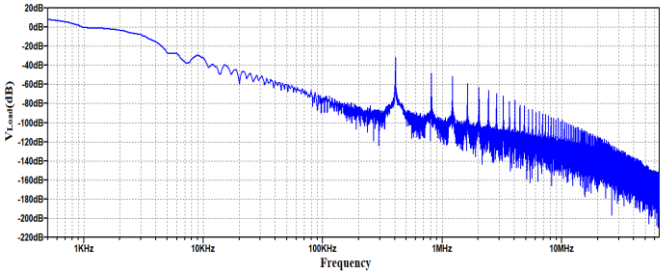


Figure 8. FFT plot of load voltage in dB when VG=12V at switching frequency of 100KHZ (Red colour), 400KHZ (Blue colour) and 600KHZ (Green colour)

Regarding the buck mode operation of SEPIC converter when the input voltage is 30V, *figure 7* shows the FFT plots of the output voltage at the selected switching frequencies. In other words, the spectral analysis of the output voltage the switching frequencies of 100KHZ, 400KHZ and 600KHZ are shown in *figure 9(a)*, *figure 9(b)* and *figure 9(c)* respectively. The noise is also included in the output voltage at all switching frequencies and this noise at the higher level in case of higher value of switching frequency as shown in *figure 10.*



(a)



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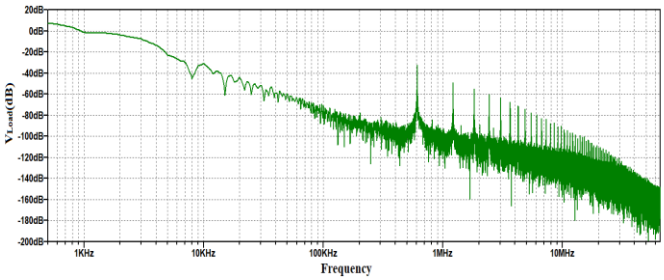

(c)

Figure 9. FFT plots of output voltage (VLoad) in dB when VG=30V at (a)fs=100KHz, (b) fs=400 KHz, (c) fs= 600 KHz

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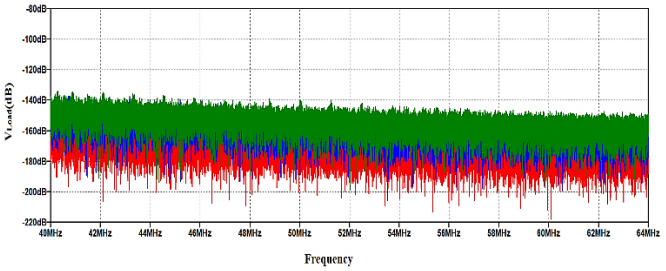

Figure 10. FFT plot of output voltage in dB when VG=30V at switching frequency of 100KHZ (Red colour), 400KHZ (Blue colour) and 600KHZ (Green colour)

4.3. Converter Efficiency at Boost Mode and Buck Mode

LTspice XVII can provide an efficiency report which include the input power, the power dissipated at each element of the converter and the output power in addition to efficiency of the converter. The values of the efficiency of the converter at each switching frequency and input voltage are recorded in *table 2*. It can be seen that the efficiency decreases from 98.7% when the switching frequency is 100KHZ to 93.4% at 600KHZ of switching frequency at boost mode operation. The same effect of increasing the switching frequency appears in buck mode operation of SEPIC converter when VG is 30V.i.e, the efficiency of the converter drops from 97.2% to 93.2% at switching frequencies of 100KHZ and 600KHZ respectively as shown in *figure 11*.

Table 2. Efficiency of SEPIC converter at buck and boost modes

Switching frequency/ parameters	100 KHz		400 KHz		600 KHz	
Input voltage	12	30	12	30	12	30
Output voltage	24	24	24	24	24	24
Efficiency	98.7	97.2	94.3	94.4	93.4	93.2

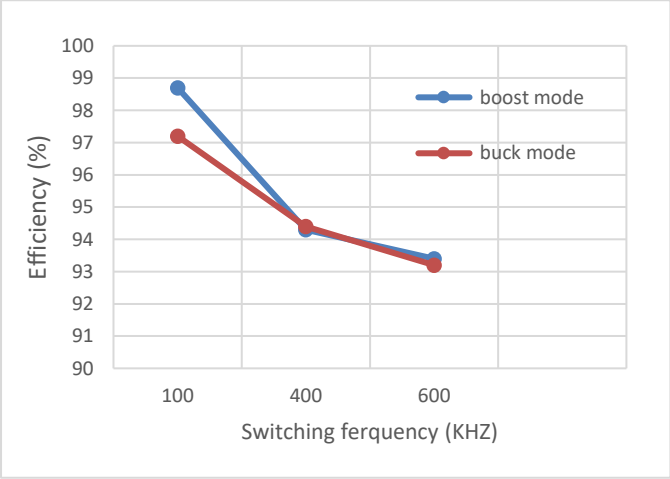

Figure 11. Efficiency of SEPIC converter at buck mode and boost mode

5. CONCLUSIONS

SEPIC converter; as one topology of DC-DC converters that can be employed in SMPS applications, is designed in three circuits to summarize the effect of switching frequency in CCM. The requirements of the operation of the three circuits are considered the same. In other word, the input voltage range and the output voltage of the converter are (12V-30V) and 24V respectively. An LTC1871 driver was used to produce a PWM signals according to the feedback signal of the load voltage. The circuits are implemented and simulated via LTspice XVII. The findings demonstrate that a better response of output voltage can be achieved at a higher switching frequency in addition to reduction of components values, i.e. the values of capacitors and inductors of the converter. However, more noise and lower efficiency of the converter are validated at higher switching frequency. This analysis is helpful guide to the designers of DC-DC converters and can be considered when selecting the switching frequency.

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