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Design and Implementation of Direct Torque Control of IPMSM Drive using Three-Level Inverter and FPGA for Electric Vehicle

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ABSTRACT- This study introduces the design and implementation for Direct Torque Control (DTC) of Field Programmable Gate Array (FPGA) based Interior Permanent Magnet Synchronous Motor (IPMSM) with Space Vector Pulse Width Modulation (SVPWM) configuration inverter for Electrical Vehicle (EV). In contrast to conventional DTC, a new DTC algorithm of drive system is proposed that endowed unified torque/flux responses with precise control levels of multiple voltage vectors. The proposed drive unified inverter states for obtaining faster dynamic torque. Consequently, the DTC scheme inspected with suppresses steady state torque ripples. The main design features of the IPMSM drive are self-regulated flux and hardware implementation for EV. The comparative analysis is made between the Simulink and real time results. Further, the ripple content of torque and flux of proposed real time of the drive is examined numerically with Simulink drive that an average ripple minimization of 60% for torque flux under load conditions is found that is achieved by FPGA. Therefore, the obtained experimental results clearly show the significance of the FPGA platform that the drive attained precise and effective torque control in both steady and dynamic conditions for EV. The DTC ensures efficiently controlled vehicles. This paper represents the proposed control methods that ensure both safety and stability in EV using DTC. This paper summarizes how the new DTC technique effectively reduces flux and torque ripples through FPGA control.

Keywords: Direct Torque Control (DTC), Field Programmable Gate Array (FPGA), Interior Permanent Magnet Synchronous Machine (IPMSM), Space Vector Pulse width modulation (SVPWM), Adaptive Fuzzy Logic Interfacing System Controller (AFLISC), Self-Regulated Reference Flux (SRRF), Electric Vehicle (EV), Xilinx ISE software.

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1. INTRODUCTION

The evolution of digital processing units and power semiconductor components are bright side for research and development in multilevel motor drive applications [1-3]. In fact, Multilevel inverter-based motor drives are commonly employed in high-power, safety-critical applications such as aircraft, robotics, ship propulsion, locomotives, and electric vehicles. By increasing the number of levels and enhancing power control capabilities, these systems reduce stress on power semiconductor switches and improve fault tolerance [4].

However, the accelerated development of multilevel inverters such as three level SVPWM and strongly improved DTC approaches, the performance of motor drives with respect to the torque and flux ripples for the most at a high number of levels is utilized that is giving the significance to amplify the research for DTC scheme of industrial drive applications [5-7]. The extension of multilevel inverters and DTC topologies are used for better control of stator-flux linkage and torque for motor under any operating conditions for Electric vehicle [8]. Lead-acid batteries are still utilized in modern cars, primarily for starting and auxiliary power. However, electric vehicles rely on Li-ion batteries due to their higher energy density and longer lifespan.

Indirectly driven EVs use electric motors to power the vehicle through in-wheel or wheel motors. In this research, the focus is on a pure EV configuration featuring two directly driven wheel motors installed within the driving wheels [9-10]. These independent wheel motors allow for rapid and precise control, resulting in improved stability and robustness in vehicle chassis and motion control compared to indirectly driven EVs [11]. Subsequently, a new DTC approach is proposed for IPMSM driven by multilevel inverter. This approach incorporates the SRRF system. This SRRF is combined with AFLISC, a powerful control approach with the features of learning mechanism of adaptive fuzzy logic system [12,13]. The AFLISC also provides feedback for the IPMSM drive. In this

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DTC framework, the more precise flux control reduces current harmonic distortions and enhances the overall efficiency of the drive.

In fact, it is very troublesome to integrate and execute the design on the FPGA. Usually, several researchers have surveyed hardware development by using the MATLAB Simulink and Xilinx system generator approach that are associated with the problems: slower simulation times and required expertise hardware resources. The Verilog Hardware Description Language (VHDL) is used for digitalization of the proposed DTC algorithm [14,15]. VHDL is well-suited for the integration and application of complex systems due to its ability to model and simulate each component of a digital system at a high level of abstraction. It offers essential features for modular design, making it an effective choice for such tasks [16,17].

In reference [18], the authors developed a DTC method for IPMSM and focused on torque ripple reduction. In this paper, the proposed methodology offers unified torque/flux responses with precise control over multiple voltage vectors, while also addressing the reduction of flux ripples. In reference [19], this work proposed with fuzzy based DTC of Induction motor for EV application and the performances analysis of electromagnetic torque behaviors of the Conventional DTC and Fuzzy based DTC have been evaluated and compared. In this paper, a model was developed using a new FPGA-based DTC technique for IPMSM, aimed at reducing torque and flux ripples while ensuring reliable operation.

The proposed DTC algorithm of an IPMSM drive based on multilevel inverter vectors are to be implemented for consideration of significant features of FPGA. The synthesis procedure of the controller involved a detailed analysis of the stability regions coupled in each mode. From this, a set of switching guidelines was derived to facilitate transitions between the different modes of their respective controllers [20,21].

This approach ensures asymptotic stability and accurate reference input tracking within the entire constrained switched closed-loop system of the IPMSM drive. As a result, the proposed optimal architecture effectively facilitates resilient torque and speed control of the motor under various operating conditions within a Xilinx ISE software environment. Ultimately, the FPGA-based controller of a laboratory prototype IPMSM drives with neutral-point clamped three-level inverter is devolved and the experimental results of IPMSM drive realized with FPGA clearly demonstrated.

This manuscript is organized as follows: Modelling of IPMSM is represented in *section 2*. In *section 3* and *4*, the implementation of the proposed control scheme for justification of proposed DTC that incorporates the implementation of SRRSF and Control technique for three levels inverter respectively. In *section 5* the implementation of FPGA scheme and in *section 6* the results and discussion describe the experimental realization of FPGA for proposed DTC for IMPSM drive and followed by the conclusion in *section 7*.

2. MODEL OF IPMSM

The proposed DTC scheme of IPMSM drive in real-time implementation is described through the schematic diagram that is shown in *figure 1*. It is characterized by its straightforward implementation, rapid dynamic response, and robustness to variations in rotor parameters. The control algorithm is derived from the projected torque and stator flux magnitudes [22], which are characterized as follows.

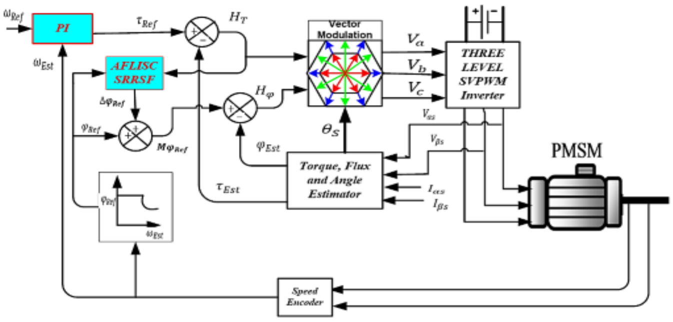

Figure 1. Schematic block diagram of proposed DTC for IPMSM for Electric vehicle

$$U_s, dq \;=\; R_s i_s, dq + \frac{d}{dt}\varphi_s, dq + \mathcal{F}\varphi_s, d \qquad (1)$$

$$\mathcal{F} = \begin{bmatrix} 0 & -\omega_r \\ \omega_r & 0 \end{bmatrix} \qquad (2)$$

$$\varphi_s, dq \;=\; [\varphi_{sd} \quad \varphi_{sq}]^T \qquad (3)$$

$$U_s, dq \;=\; [U_{sd} \quad U_{sq}]^T \qquad (4)$$

$$i_s, dq \;=\; [i_{sd} \quad i_{sq}]^T \qquad (5)$$

The predicted electromagnetic to expressed as equation:

$$T_e \;=\; \frac{3P}{2}\left(\varphi_{sd} i_{sq} - \varphi_{sq} i_{sd}\right) \qquad (6)$$

Where p is number of poles and these dynamic system equations are utilized to adopt for any PMSM such as Surface PMSM (L_q=L_d) and Interior PMSM (L_q>L_d). However, the vector of stator flux is expressed:

$$\varphi_s, dq \;=\; \mathcal{G} i_s, dq + \varphi_r, dq \qquad (7)$$

3. IMPLEMENTATION OF DTC SCHEME

In the DTC approach, stator flux plays a significant role in enhancing the stability and efficiency of the IPMSM. The motor operates from no load to full load, but the flux can cause significant torque ripples and operates at constant flux, leading to increased core losses that may reduce overall system efficiency. To achieve the desired performance in motor control, the SRRSF is proposed for the multilevel vector fed DTC of the IPMSM [12]. The SRRSF is based on the torque hysteresis controller and the reference flux hysteresis regulator, illustrated in *figure 2*. Additionally, SRRSF is implemented using Fuzzy Logic interfacing approach [13].

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The AFLISC is utilized to ensure a stable and robust system. It integrates two key components: an AFLC and learning approach. The feedback information obtained from the learning operation is used to refine the AFLC. In fuzzy controller, a scaling factor tuning technique is applied [11,20]. Three scaling factors are preferred based on two inputs, torque error (HT = TRef - TEst) and reference flux and one output which is automatically corrected reference flux. These scaling factors are consistently adjusted until they meet the conditions necessary for an interfacing system to achieve the desired control effectiveness of the IPMSM in both stable and variable states. *figures 3 (a), (b), and (c)*, along with *table 1*, illustrate the membership functions of the Intelligent Fuzzy Controller, incorporating scaling factors defined by the linguistic rules presented in the table.

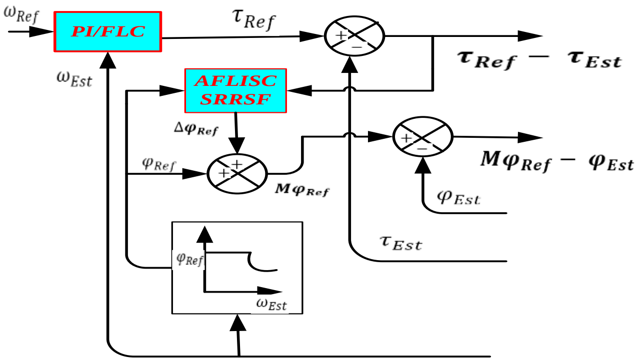

Figure 2. Proposed control technique

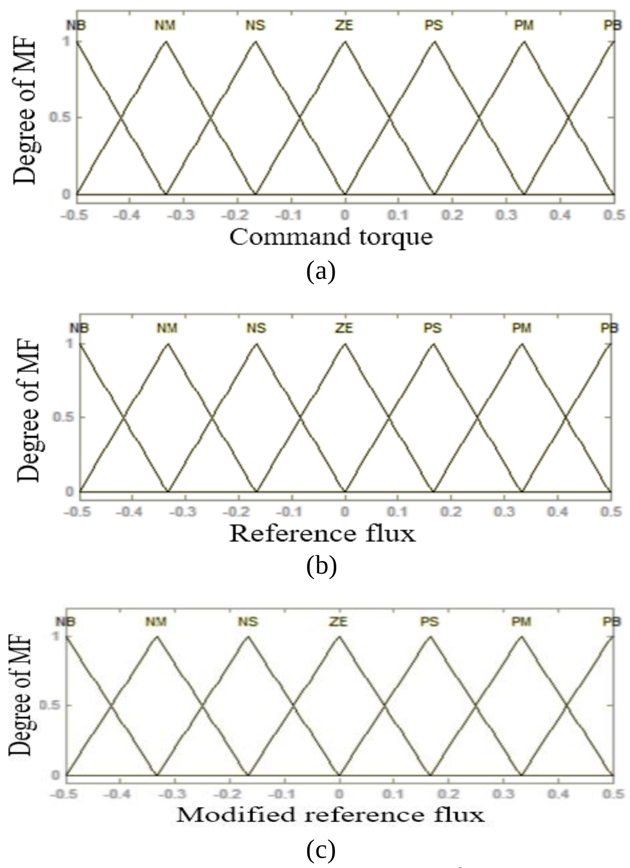

Figure 3. Scaling Factor based on membership functions: (a) torque error (b) Reference stator flux (c) modified stator flux

Table 1. **Fuzzy Control Rules**

$\Delta e_s/e_s$	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	ZE
NM	NB	NB	NB	NM	NS	ZE	PS
NS	NB	NB	NM	NS	ZE	PS	PM
ZE	NM	NS	NS	ZE	PS	PM	PB
PS	NM	NS	ZE	PS	PM	PB	PB
PM	NS	ZE	PS	PM	PB	PB	PB
PB	ZE	PS	PM	PB	PB	PB	PB

4. THREE LEVEL NPC – SVPWM TECHNIQUE

The multilevel inverter configuration is more feasible for medium and high-power industrial applications because of built-in features: (i) it increases the number of output levels from the inverter (ii) it reduces burden on semiconductor devices, (iii) it minimizes THD in stator winding currents and voltages. However, it encounters the challenge of uneven voltage distribution across the DC link capacitors. To address this issue, the SVPWM technique is implemented to generate voltage vectors that effectively balance the capacitor voltages [24,25].

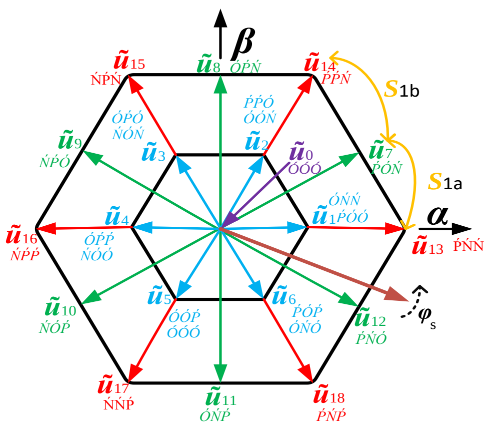

Figure 4. Representation of multi active vectors

A unified torque/flux is obtained through a straightforward calculation process, directly reflecting the control effects based on the active voltage vectors [26]. The multiple active voltage vectors are illustrated as in *figure 4*. The multilevel voltage vectors are expanded into an infinite set of virtual vectors with variable magnitudes in the same direction as the original vectors, achieved through duty cycle modulation. This approach enhances control precision and minimizes torque and flux ripples.

The uniform expression for the voltage vectors is conveyed as follows:

$$v_n(d_n) = \begin{cases} \frac{2}{3} v_{dc} d_n e^{j\theta_n} \\ \frac{1}{3} v_{dc} d_n e^{j\theta_n} \\ \frac{1}{\sqrt{3}} v_{dc} d_n e^{j\theta_n} \end{cases} \quad (8)$$

Where n is number of active voltage vectors, d_n represents the duty cycle of active voltage vector for v_n and $d_n \in [0, 1]$, θ_n exhibits the angle between v_n and the α-axis. However, the evaluations of torque and flux responses are defined with variation of d_n and θ_n that are illustrated as follows:

$$T_{en}(d_n, \theta_s) = \frac{v_{n,\beta}(d_n, \theta_s)}{^2/_3\, v_{dc}} \quad (9)$$

$$\varphi_n(d_n, \theta_n) = \frac{v_{n,\alpha}(d_n, \theta_s)}{^2/_3\, v_{dc}} \quad (10)$$

In accordance with IPMSM, the change rates of T_{en} and φ_n is rearranged and

$$\frac{d}{dt} T_e = \frac{2\,K\,v_{dc}}{3}[T_{en}(d_n, \theta_s) - e] \quad (11)$$

$$\frac{d}{dt}|\varphi| = \frac{2\,v_{dc}}{3}[\varphi_n(d_n, \theta_n)] \quad (12)$$

whereas, $e = \frac{\omega_r|\varphi|}{\frac{2}{3}v_{dc}}$

The following expression can be attained by simplifying the above equations:

$$\frac{d}{dt} T_e \propto [T_{en}(d_n, \theta_s) - e] \quad (13)$$

$$\frac{d}{dt}|\varphi| \propto [\varphi_n(d_n, \theta_n)] \quad (14)$$

Therefore, the values of $T_{en}(d_n, \theta_s) - e$ and $\varphi_n(d_n, \theta_n)$ each voltage vector are proportional to the rate of change of torque and flux, respectively. Therefore, the torque and flux control effects of each active voltage vector are represented by the evaluation functions Ten and φn. Moreover, the torque and flux ripples in the steady state are diminished effectively; smooth vector switching and synthesization are confirmed using the SVPWM principle.

5. IMPLEMENTATION OF FPGA SCHEME

A typical modern FPGA offers designers programmable logic blocks that include the combinational logic and flip-flops for use in their designs. Additionally, manufacturers validate that logic is often used alongside memory, so they typically integrate varying amounts of static RAM within their chips. Clock conditioning has also evolved standard, with built-in support for Delay Locked Loops (DLLs) and Phase Locked Loops (PLLs) on the same silicon chip [20]. Moreover, an FPGA does not operate in isolation; it must be easily integrated with external signals. To facilitate this interfacing, FPGA suppliers have made significant enhancements to the adaptability of the input/output sections surrounding the chip pads, allowing each chip pad to function as an input, an output or both.

The range of supported electrical specifications are comprehensive and innovative strategies for optimizing bandwidth such as clocking data on both sides of the clock are commonly implemented.

6. RESULTS AND ANALYSIS

To verify the performance of the proposed DTC for the three-level NPC inverter driving an IPMSM, we developed the following laboratory prototype.

(a) System Chip control consisting of SPARTAN 6 FPGA platform board (cont. EP2C70F896C6), 68416 LEDs, 1152000 b of on-chip RAM, 150 hw, 18-b embedded multipliers, 36 DSP.

(b) The regulatory circuit includes a dead-band circuit, voltage and current sensor circuits and DC power suppliers.

(c) 3-ϕ IPMSM, 1kW, 8 pole, 230 V,5 A, and 3000 r/min with 0.662 N-m braking torque that consists of an optical sensor and a functional graph for the hardware FPGA implementation of the three-level NPC inverter driving the IPMSM is illustrated in *figure 5*.

(d) Three level neutral point clamped inverter power circuit which consists of 12 number of IGBT inverter (SEMIKRON make, 1200 V, 2 pole MCB, 25A and 20 kHz) is utilized to control of IPMSM which develops the switching pulses for suggested DTC approach that inverter phase voltages are shown in *figure 6*.

The experimental results for the proposed IPMSM drive with the three-level NPC inverter were obtained using a YOKOGAWA digital oscilloscope. This setup featured a real-time interface and utilized an appropriate sampling frequency to ensure high-quality signal capture, particularly for the phase currents and the electromagnetic torque measured by a 2500 pulses/rev encoder. The figures below illustrate the effectiveness of the FPGA model-based control scheme for the advanced experimental setup, highlighting performance analysis across different operational modes of the IPMSM drive. This includes steady-state conditions, no-load speed tests, and load application speed variations.

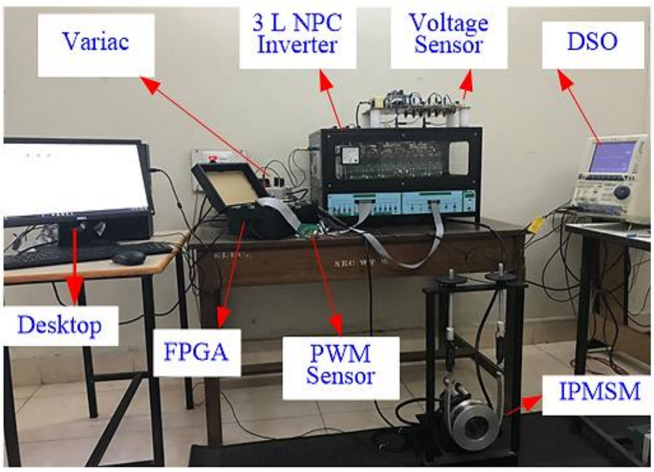

Figure 5. Laboratory experimental Setup

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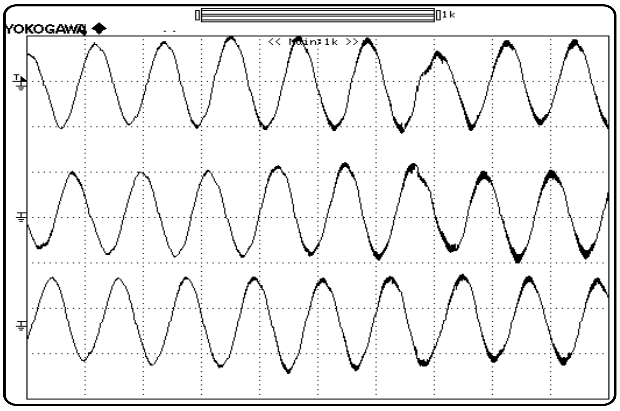


Figure 6. Stator phase voltages

Essentially, *figure 7*. represents the rotor speed in startup state (0 – 500 rpm) by successively increasing of speed pattern 500 → 1000 → 1500 → 2000 → 2500 that demonstrated with a quick and effective response. However, the real and estimated speeds are in superposition, with the estimation error converging to zero. The steady state of the IPMSM is evaluated without introducing load torque, and the fast dynamic response of the electromagnetic torque is observed, along with low ripple levels in the flux components, attributed to the use of the SVPWM-NPC inverter. However, the effectiveness of FPGA based proposed scheme of the drive is illustrated by comparison of performance indices under variable speed with no load test that are presented as in *figure 8*.

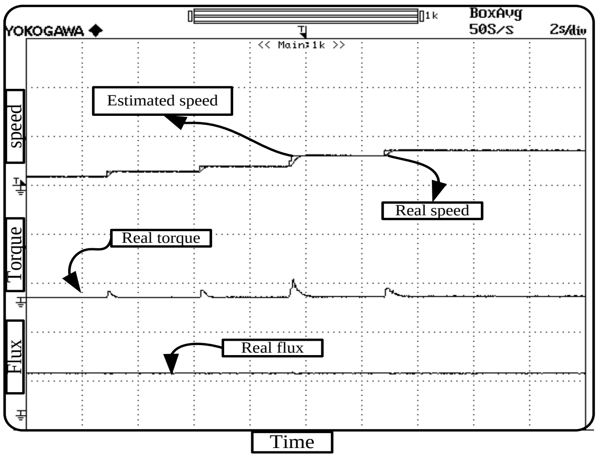
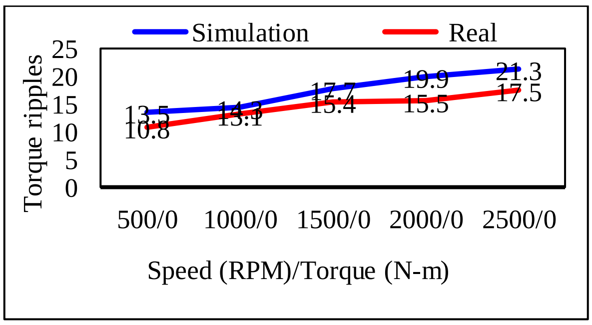
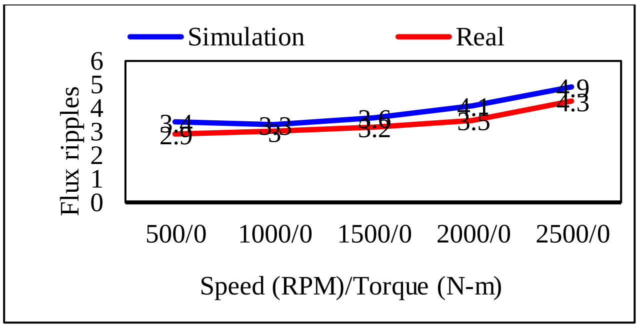


Figure 7. Startup state: real and estimated rotor speed, torque and flux without load



(a)



(b)

Figure 8. Evaluation of ripples for IPMSM under variable speed and no load:(a) torque ripples and (b) stator flux ripples

The next test is the speed of IPMSM started at (0→1500 rpm) and the real speed track a step is elevated from 1500→2500 RPM and then load torques of 1.5 N m and 2 Nm are introduced twice for every speed state that confirmation is represented as in *figure 9*. In this context, the speed responses of the FPGA based IPMSM drive demonstrate rapid load disturbance rejection, with the estimated speed aligning closely with the actual speed during reference variations, and the estimation error consistently converging to zero. The experimental results clearly indicate that the torque and flux responses of the proposed algorithm are smooth, ensuring stable motor operation. Subsequently, the performance quantitative indices of torque and flux ripples for the proposed FPGA control approach for the IPMSM are detailed in *figure 10*.

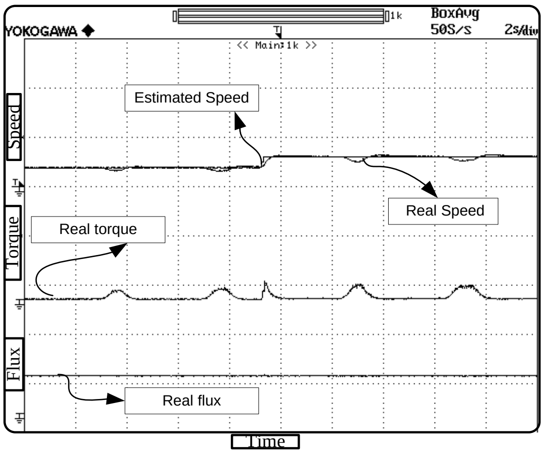
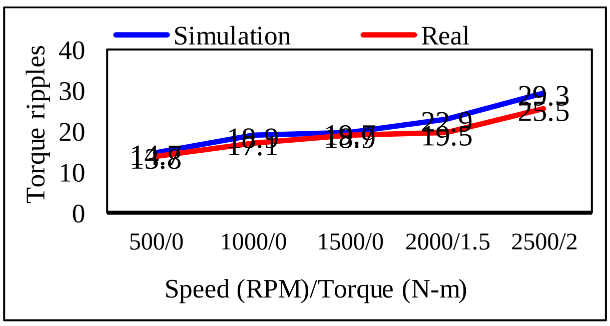
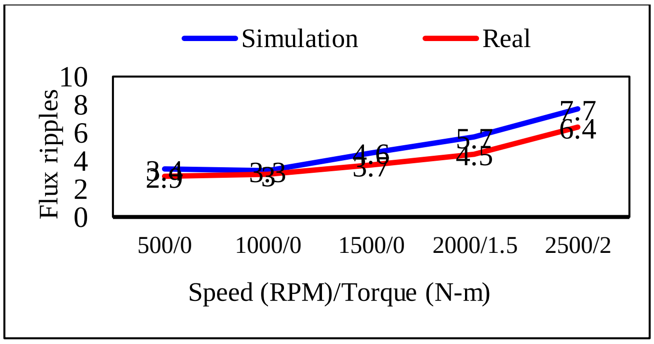


Figure 9. Start-up IPMSM with load torque twice: real and estimated rotor speed, torque and Flux



(a)



(b)

Figure 10. Comparison of ripples for IPMSM under a variable speed and applied twice load: (a) torque ripples and (b) stator flux ripples

To attain the more smoothness and faster dynamic torque responses of the system, the proposed laboratory experimental IPMSM drive is feasible and tested under variable speed with variable load. The drive is operated under sequentially increasing speed pattern 500→1000→ 1500→ 2000→ 2500 during variation of the variable load torque such as 0 N-m to 2.5 N-m. is applied for comprehensive speed range that testimony is represented in *figure 11*. It observed that the response of torque, estimated speed and stator flux of proposed IPMSM drive is performed with smooth steady state operation during the load changes. Further, it found that the magnitude of ripples in the flux and torque is diminished effectively with SVPWM-NPC Inverter configuration. These experimental performances of the proposed FPGA based IPMSM drive are clearly citing that it consists of good accuracy and high efficacy. Similarly, the comparative analysis is made for evaluating the effectiveness of FPGA based IPMSM drive that is illustrated with the performance indices under variable speed and variable load test that are presented in *figure 12*.

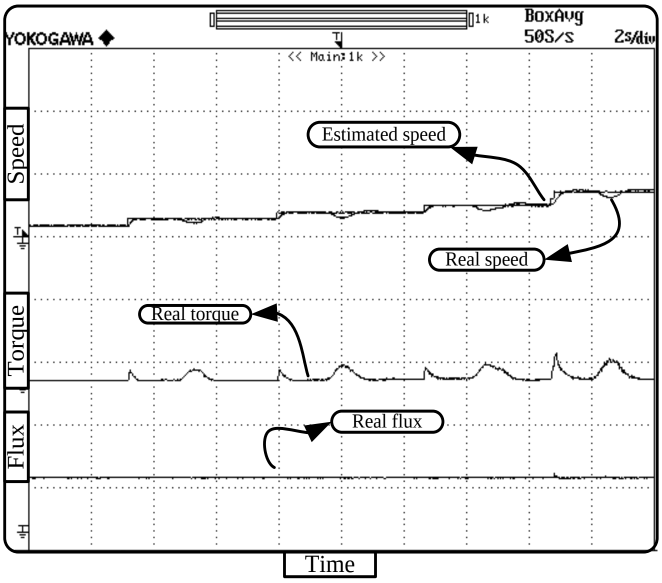
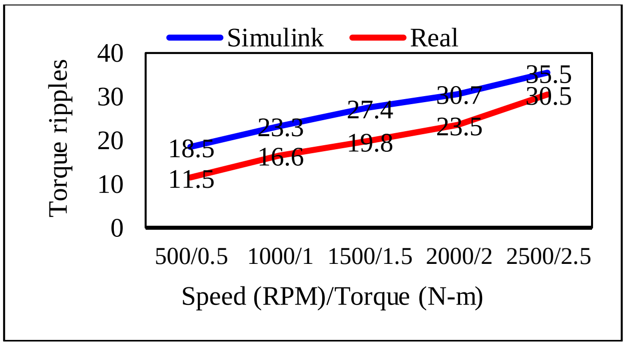
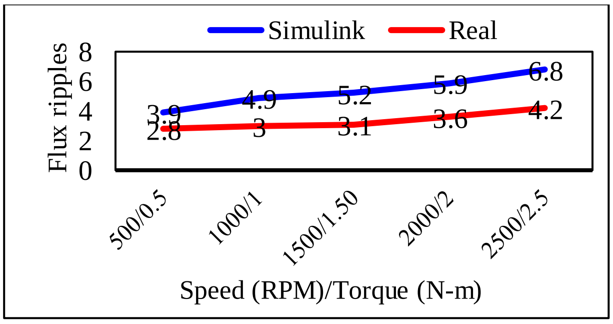


Figure 11. Startup IPMSM with variable speed and load: Real and estimated rotor speed, torque and Flux



(a)



(b)

Figure 12. Comparison of ripples for IPMSM under variable speed and variable load: (a) torque ripples and (b) stator flux ripples

By comparing the results of reference [18] with those presented in this paper, we can conclude by using the following table that,

Table 2. Comparison of results

	Reference [18]	Presented paper
Torque Ripples	Reduced	Reduced
Flux Ripples	Not done	Reduced
DTC technique	Reducing the torque pulse for the DTC method by using an artificial neural network	Reducing the torque pulse and flux pulse using new DTC method with FPGA based SVPWM
Load conditions	Not done	Analyzed under both no-load and load disturbance conditions

7. CONCLUSION

This paper presents a laboratory prototype for implementing a new DTC system for an IPMSM drive, utilizing a three-level NPC inverter for electric vehicles. The proposed control system architecture is successfully realized on an FPGA platform with efficient resource utilization and rapid execution times. The performance of the MLI fed IPMSM drive is analyzed under both no-load and load disturbance conditions using SVPWM techniques, which enhance its suitability for solar electric vehicle applications. The proposed system significantly reduces voltage THD as well as torque and flux pulsations. Experimental outcomes demonstrate that the rotor accurately traces the electrical reference speed under various operating situations. Collectively, these findings confirm the

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effectiveness and reliability of the suggested FPGA-based control framework for the IPMSM drive. The DTC models also enhance driving wheel speed with high precision on curved or sloped roads.

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