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Hybrid Design of Phase Frequency Detector Applied in Phase Locked Loop to Eliminate Dead and Blind Zones

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ABSTRACT- This paper presents a hybrid design and simulation of a Phase Frequency Detector (PFD) which eliminates the effects of the blind and the dead zones for a charge-pump phase-locked loop (CP_PLL). These parameters limit the detection range of the PLL since they occur at zero and 2π phase differences respectively. Two XOR gates have been added to the conventional D-Flip-flop PFD to eliminate both parameters simultaneously. The proposed system has been simulated using Multisim 14.3 and tested using a 10 MHz input frequency. The simulation results show the system is free of dead and blind zones.

Keywords: Phase-locked loop (PLL), Phase Frequency Detectors (PFD), Dead zone, Blind zone.

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1. INTRODUCTION

Phase-locked loop (PLL) plays a vital role in data transmission, especially in wireless communication systems including 5G, Bluetooth, GSM, etc. Due to the circuit complexity and operation frequency rising, PLL has been widely applied in many high-speed designs, such as synchronization and demodulation circuits [1], Clock recovery [2], noise and jitter reduction [3], frequency synthesizers [4], and microprocessors [5]. The traditional PLL method based on a charge pump (CP) is shown in Figure 1. It mainly includes a phase frequency detector (PFD), a charge pump (CP), a loop filter (LF), and a voltage-controlled oscillator (VCO). In the figure, $\omega_{in}(t)$, ω_{out}, $\varphi_{in}(t)$, and $\varphi_{out}(t)$ represent the angular frequencies and phases of the input and output signals, respectively.

PFD system relies on feedback which helps detect errors and sensing [6]. While designing the charge pump and PFD, many issues arose like dead and blind zones, timing and current mismatch, overlap capacitances, and reset path delays. Another significant and most important issue is the phase noise added by these two blocks. Therefore, PLLs are being focused on in research for their challenging aspects such as no dead and blind zones, low phase noise, and less reference spur as well as minimum power consumption. Regarding the conventional PFD, which is composed of two D Flip-Flops (DFF), dead and blind zone solving have been highly concentrated in literature since it occurs near zero phase differences (phase locking state) and maximum phase differences respectively. Researchers have proposed designs with constant delay in the reset path to find dead zone values of 3π/8, 4π/9, and π/11 [7-9], respectively. In [10] a differential PFD was adopted to achieve a dead zone of π/10. However, none of the literature mentioned the behavior of the blind zone. Both the dead and blind zones were reduced by incorporating a variable element in the proposed design of the PFD [11, 12]. Recently researchers have proposed new methods to eliminate the blind and dead zones at very limited frequencies [13-16].

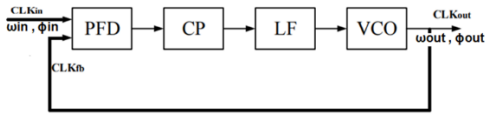

Figure 1. Block diagram of PLL

Therefore, this issue is still of interest to many researchers by finding new methods to eliminate blind and dead zones. In this article, we will demonstrate a novel technique that concentrates on eliminating the dead and blind zones of the conventional PFD using two XOR gates and two AND gates.

2. PHASE FREQUENCY DETECTORS (PFD)

A phase detector is a logic circuit, analogue multiplier, or frequency mixer that is used to generate a voltage signal [17, 18]. The PFD is used to detect the frequency and phase between the input reference signal and the feedback from the VCO compared to phase detectors, which can detect only phase differences. Figure 2(a) illustrates the design of edge-sensitive

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conventional PFD. Two NAND gates and two edge-triggered D-flip-flops (DFFs) have been used to provide a reset path for a set of high-value outputs. The PFD works in three states: down (UP=0, DN=1), UP (UP=1, DN=0), and the third state, which is the initial state (UP=0, DN=0), as shown in *figure 2(b)*.

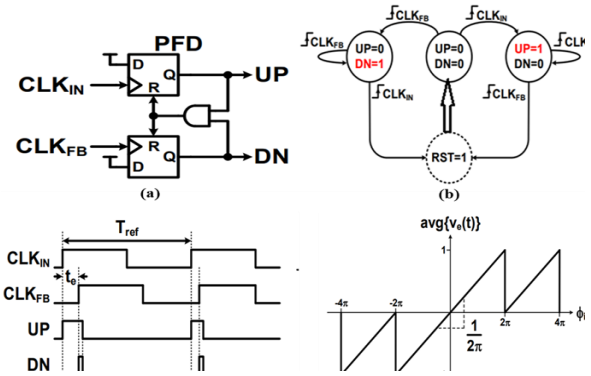

Figure 2. (a) Design of PFD, (b) Finite state machine of PFD, (c) Waveform of PFD, and (d) Transfer characteristics of PFD.

Figure 2(c) shows the waveform assuming the CLKin leading the CLKfb. First, the outputs (UP and DN) are low state (0V). When a rising edge from CLKin arrives, the upper DFF is turned on to move the PFD to the first state (UP=1, DN=0). When the feedback CLKfb rises up after time (te) the lower DFF is triggered forcing the PFD to transfer to the second state (UP=1, DN=1). Having done that, the NAND gate output goes low resetting both DFFs and forcing the PFD to return to the initial condition. Figure 2(d) shows the output characteristics of the conventional PFD. This type of detector allows for a wide frequency locking range since it is linear over the range of -2π to 2π phase deference. PFD suffers from the presence of dead zone that occur near zero phase difference. Which can be defined as the maximum phase differences that cannot be detected by PLL [19]. Figure 3 shows the transfer characteristics of the system. Note that when the phase difference is small, the PFD pulses cannot propagate effectively to the charge pump. Thus, a dead zone ($Ø_{DZ}$) will be formed which causes an increase in oscillation and low loop gain.

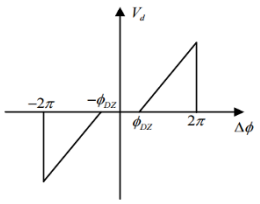

Figure 3. Transfer characteristics of PFD with dead zone

Blind zone (TBZ) is the other drawback of conventional PFD which occurs near ±2π phase differences as shown in Figure 4(a). The total blind zone in any single cycle is given by Eq. (1).

$$TBZ = T_{DFF} + T_{RST} + 2\ td. \quad (1)$$

Where TDFF is the propagation delay of DFF, TRST is the RST TO Q delay of DFF, and td is the propagation delay of the NAND gate. The PFD cannot respond to the delay signal rising edge which leads to a drop signal. This leads to a missing edge leaving the next rising edge to drive the loop in the wrong direction and deliver wrong information to the VCO. The presence of the blind zone reduces the phase difference detection range as shown in Figure 4(b). The blind zone ($Ø_{BZ}$) and maximum detection range (MDR) were calculated based on Eq. (2) and Eq. (3),

$$\phi_{BZ=2\pi\frac{T_{BZ}}{T_{REF}}} \quad (2)$$

$$MDR = 4\pi - 2\phi_{BZ} = 4\pi\left(1-\frac{T_{BZ}}{T_{REF}}\right) \quad (3)$$

Where T_{BZ} and T_{REF} are the time of the blind zone and period of the input reference($CLKin$) respectively. The worst case happens; when the blind zone $Ø_{BZ}$ reaches the π phase differences the locking range would be halved. So, the maximum locking frequency (f_{max}) is based on Eq. (4).

$$f_{max} = \frac{1}{2.T_{BZ}} \quad (4)$$

Therefore, this PFD mainly has non-ideal effects of the blind zone leading to a reduction in the detection range and consequently limiting the maximum operating frequency.

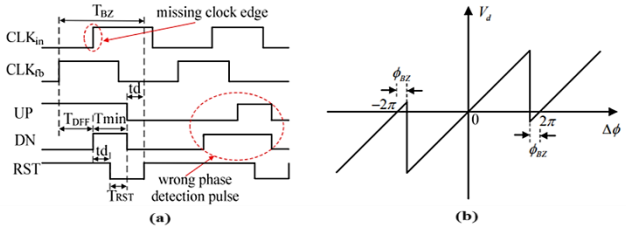

Figure 4. (a) PFD waveform with different sources of the blind zone, and (b) Transfer characteristics of PFD

3. XOR PHASE DETECTOR (PD)

The XOR PD is simply an exclusive OR (XOR) gate. As the phase difference between the inputs varies, so does the width of the output pulses. Therefore providing a dc level proportional to the phase difference (ΔØ) [20]. The operation of the XOR gate is simply comparing the phases of the two input signals and producing pulses at the rising and falling edges of the inputs [21]. Those pulses represent and are proportional to the phase difference between the two inputs as shown in *figure 5*.

The XOR PD is a linear device, but if it was in phase and the error was greater than 180◦, it would lose its linearity [22]. In this article two XOR gates are going to be used in conjunction with the D-type PFD to eliminate the dead and the blind zones which will be explained in the next section.

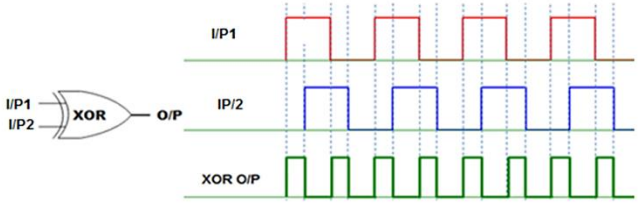

Figure 5. The XOR gate input and output pulses

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4. METHODOLOGY

In this article, we proposed a new method to eliminate both dead and blind zones of conventional PFDs at the same time. Figure 6 and Figure 7 illustrate the block diagram and flowchart of the proposed method. For blind zone elimination, both PFD (UP and DN) outputs are input to XOR1. The output of this gate is the real phase difference after extracting different parts of the blind zone which can be estimated based on Eq. (5).

$$T_{BZ} = T_{DFF} + T_{RST} + 2\,td \quad (5)$$

The XOR gate is a level-sensitive device (needs to cross a threshold voltage VT to change state) which causes a gate propagation delay (D) that leads to a dead zone equal to this delay. This delay can be used to count for the dead zone of the CP. To overcome this dead zone the DN channel is delayed by D and input with a direct UP channel to XOR1. The added Delay introduces a D blind zone at the maximum phase difference. To solve this blind zone the UP channel is also delayed by D and input with the direct DN channel to XOR2 [23]. The output of XOR1 and XOR2 are input with the UP and DN to AND1 and AND2 respectively to ensure that the lag channel is off during locking acquisition. Multisim 14.3 will be used to simulate the proposed system [24].

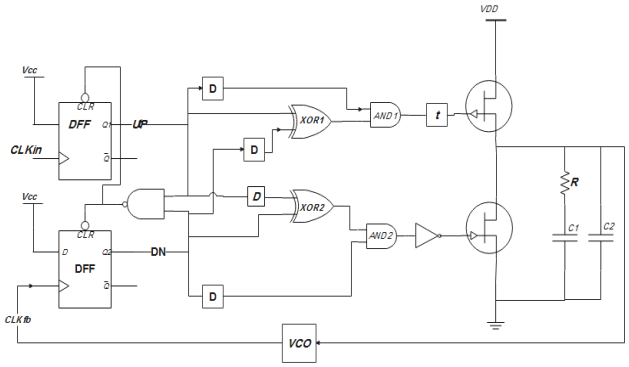

Figure 6. Proposed system block diagram

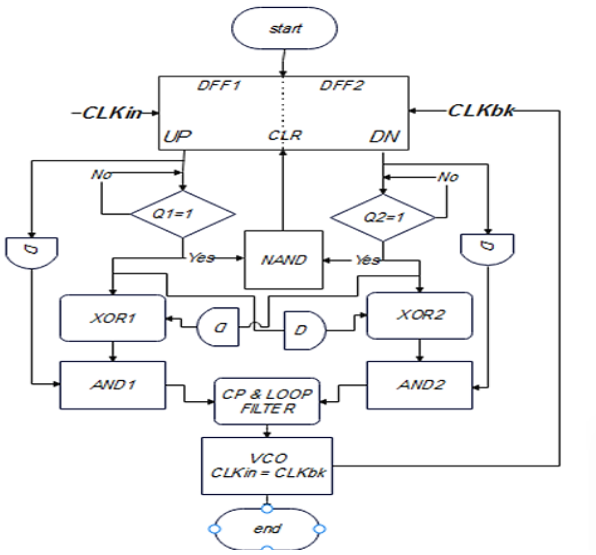

Figure 7. Proposed system flow-charts

5. SYSTEM SIMULATION, RESULTS, AND COMPARISON

Figure 8 and Figure 9 show the simulation system with the corresponding signals of different parts. It can be seen from the second figure that for the case when CLKin lead and CLKfb lag, the output of XOR1 is the true phase difference between both signals after extracting all delays introduced by the DFF, NAND, and RST (TBZ). It can also be seen that the output of AND2 (lag channel) is zero, eliminating this channel delay.

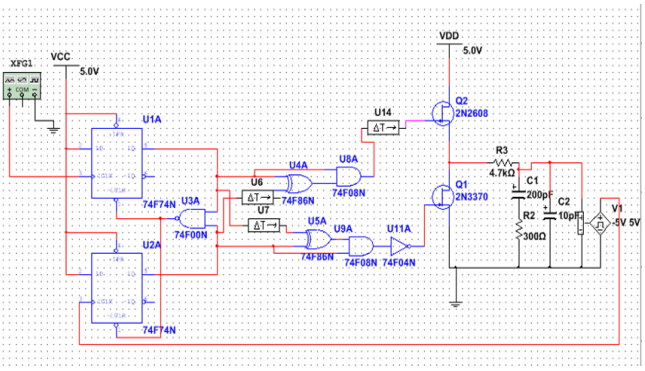

Figure 8. Proposed system simulated circuit

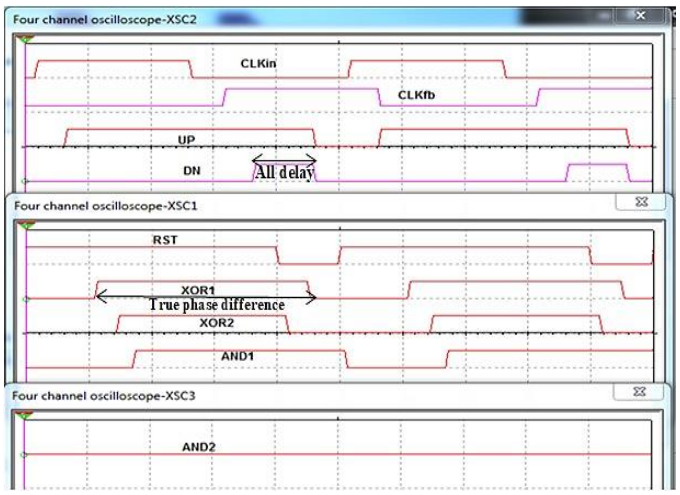

Figure 9. Structure corresponding waveforms of the proposed system with the CLKin lead the CLKfb signals. The output of XOR1 represents the true phase difference between both signals after extracting all delays introduced by the DFF, NAND, and RST

As far as the dead and blind zones are concerned in this article both tests will be carried out as follows:

For the dead zone test which occurs near zero phase differences. A 10 MHz reference signal has been input to both DFFs of the PFD with zero phase differences. Figure 10 shows the corresponding waveforms of the different parts of the system. As shown the outputs of XOR1 and XOR2 are pulses of the same width equal to the added delay (ΔT=D). During these pulses, no currents are supplied to the loop filter since both transistors are on during this time. This ensures that the system is free of dead zones.

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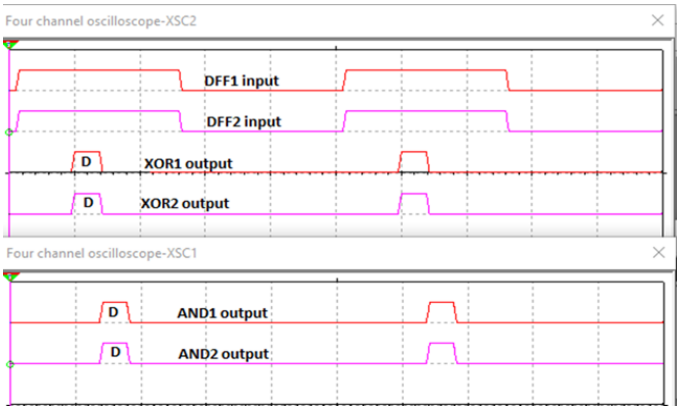

Figure 10. Corresponding waveforms of dead zone test using 10MHz input signal with zero phase difference. The outputs of XOR1 and XOR2 are pulses of the same width (D). During these pulses, no currents are supplied to the loop filter since both transistors are on during this time

For the blind zone test which occurs near 2π phase differences figure 11. The 10MHz (period =100ns) has been applied to both inputs of both DFFs with the input to DFF2 being delayed by 100 ns. After the 100ns this channel enters the blind zone since it's pushed forward by the added delay (D) but it's insensitive to the second triggering edge. During this time the DN channel is still out of the blind zone since it's pulled back by the added delay (D). Up on the rising edge of this channel, the UP channel is triggered down. It can be seen from figure 11 that the outputs of XOR1 and XOR2 are equal to (100ns + D) and (100ns – D), respectively. Also, it can be seen that the output of AND1 is the same as that of XOR1 which drives the charge pump. The output of AND2 is zero since the lag channel has no contribution to CP since the corresponding transistor is off during this process. The figure shows that the second edge of the UP channel will be missed but during the next cycle the frequency of the VCO will change and a new process will be carried out. This ensures that the system is free of blind zone.

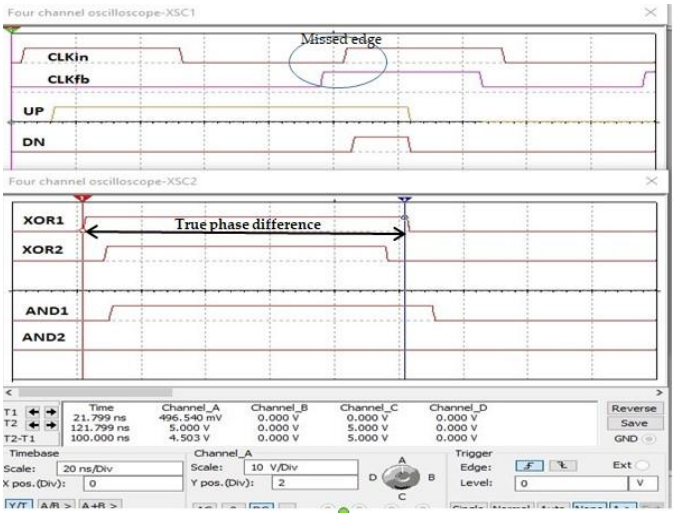

Figure 11. The corresponding waveforms of blind zone test using 10MHz input signal. The second edge of the UP channel is missed but during the next cycle the frequency of the VCO will change and a new process will be carried out.

Figure 12 shows the locking condition when the input reference CLKin is equal to free running frequency of the VCO and in phase. The outputs of AND1 and AND2 are equal pluses representing delay D added to the two XOR gates. This is the only case when both signals appear together in the locking process. Any way no currents flow to the loop filter since both transistors are on during

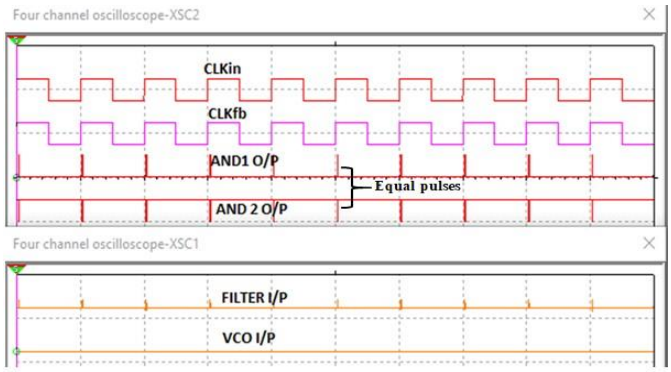

Figure 12. The corresponding waveforms for input signal CLKin equal to the free-running frequency of VCO CLKfb. The outputs of AND1 and AND2 are equal pulses supplying no current to the loop filter

Another test should be done on the simulation system to check for the locking ranges. A frequency range of (100 KHz to 2.2 MHz) was applied to the system with a 1.15 MHz free-running frequency of the VCO. The system locks for all the bands of frequencies which prove that it's free of dead and blind zone. In *table 1*, the performance parameters of different designs are presented. Most of the recently published research concentrated on using CMOS technology to minimize the delay of the PFD in their systems due to the high switching speed. This improved either the dead or blind zone but not eliminated them simultaneously. In this article the conventional PFD has been used with simple design using TTL logic for 10MHz input signal. The delays of both channels are canceled by the XOR gate which frees the system from the effects of the dead and blind zone simultaneously. For higher frequencies ECL logic can be used.

Table 1. Performance parameters of the different designs studied

Reference	Technique	Frequency	Dead zone	Blind zone
[7]	Latch-based architecture PFD (CMOS)	1 GHz	π/11	Not measured
[10]	Constant delay-element in the reset path (CMOS)	50Hz-1GHz	π/10	Not measured
[12]	Variable delay-element in the reset path (CMOS)	3.5GHz	110.5ps	Not measured
[24]	90nm standard CMOS PFD	5GHz	25ps	Not measured
Proposed system	Conventional PFD using TTL logic	10MHz	FREE	FREE

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6. CONCLUSION

In this paper, we proposed a novel design of a phase frequency detector applied in PLL to eliminate the dead and blind zones. An improved structure of PFD by two XOR gates has been used to eliminate non-ideal effects such as dead and blind zones respectively. This technique extends the phase difference detection range and enhances the operating frequency of the PLL. Multisim 14.3 has been used to simulate the proposed system. The simulation system was tested using 10MHz input signal. The simulation results show the system is free of dead and blind zones. It was also tested for the range of (100 KHz-2.2 MHz), which achieved fast locking over the whole range. The proposed system will be implemented using TTL and ECL logic circuits to verify the simulation result for low and high frequencies respectively.

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Competing interests: The authors have no relevant financial or non-financial interests to disclose.

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