FOREX Publication
Open Access | Rapid and quality publishing

International Journal of
Electrical and Electronics Research (IJEER)
Research Article | Volume 13, Issue 1 | Pages 37-43 | e-ISSN: 2347-470X

Modelling and Simulation of Multi-Level Inverters Utilizing Alternate Phase Disposition (APOD) PWM Modulation in MATLAB/Simulink

Kammampati Suresh[1] and Dr. A. Raghu Ram[2]

[1]*PhD Scholar, Department of Electrical and Electronics Engineering, JNTU Hyderabad, Telanagana, India, sssureshk2@gmail.com*
[2]*Professor, Department of Electrical and Electronics Engineering, JNTU Hyderabad, Telanagana, India*

***Correspondence:** *sssureshk2@gmail.com*

ABSTRACT- In recent times, the growing demand for enhanced industrial applications and the rise of Electric Vehicles (EVs) have led to a requirement for higher power equipment. Certain applications, such as medium voltage motor drives and utility systems, now demand the utilization of medium voltage and megawatt drivers. To address these needs, the concept of multi-level inverter topologies has been introduced, particularly for medium and high-power applications. The evolution of multilevel converters, starting with three levels to achieve elevated power levels, has given rise to various topologies. These converters utilize a progression of force semiconductor switches and various lower voltage DC sources to integrate a flight of stairs voltage wa veform, in this manner empowering higher power change. While the PWM inverter has shown exemplary execution, issues like consonant bends have been seen in two-level inverters A viable solution to these challenges involves increasing the number of voltage levels, a feat accomplished by multilevel inverters. The traditional approach often leads to high switching losses and suboptimal drive performance. This paper proposes an effective alternative by introducing more levels to mitigate harmonics, thereby enhancing drive performance. The results of this approach were analysed using MATLAB/Simulink.

Keywords: Harmonic distortion, Multilevel Inverters, Pulse Width Modulation, DC bus Voltages.

ARTICLE INFORMATION

Author(s): Kammampati Suresh and Dr. A. Raghu Ram;
Received: 21/10/24; **Accepted**: 20/03/25; **Published:** 30/03/25;
E- ISSN: 2347-470X;
Paper Id: IJEER240431;
Citation: 10.37391/ijeer.130106
Webpage-link:
https://ijeer.forexjournal.co.in/archive/volume-13/ijeer-130106.html

Publisher's Note: FOREX Publication stays neutral with regard to Jurisdictional claims in Published maps and institutional affiliations.
.

1. INTRODUCTION

The utilization of switching converters, in particular DC to AC PWM inverters, has increased across a variety of different industries. This is due to the fact that they have the ability to reduce the amount of energy that is consumed, increase the efficiency of the system, improve product quality, and require significantly less maintenance. The notion of multilevel converters was first introduced in 1975, marking the beginning of a concept that can be utilised in a variety of different applications. The term "multilevel" was initially utilized for the first time thanks to the three-level converter. It resulted in the creation of a number of different multilayer converter topologies. Creating multilayer waveforms can be accomplished by the use of fundamental approaches that include connecting standard converters in parallel or series. In order to combine a stairwell voltage waveform, staggered converters are utilized. These converters make use of a movement of power semiconductor switches that are connected to distinct lower voltage dc sources. This enables the converters to deliver a greater power output than they would have been able to otherwise. These direct current voltage sources could be capacitors, batteries, or any number of different power sources that are friendly to the environment. The compensation of force changes brings these sources together to achieve a high result voltage, with the evaluated voltage of the switches being determined solely by the dc voltage sources that are associated with them. Circuit designs for inverters typically include transistors and other semiconductor switches that have power ratings that are more than enough. As a result of their high-power handling capability and controllability over a wide range of firing angles, thyristors, and more specifically silicon-controlled rectifiers (SCRs), are utilized in bigger systems. Whenever they are not linked to a transformer, SCRs produce square waveforms, which allows them to have a straightforward ON and OFF behavior. Through the use of Fourier analysis, periodic waveforms are represented as the sum of infinite sine waves, with the fundamental component having a frequency that is identical to that of the initial waveform. Harmonics, which are integral multiples of the fundamental frequency, are the sine waves that are represented by the other sounds in the series.[1] – [3].

Research aims at laying down the basic guidelines for multilayer inverters to increase the efficiency of power conversion and to eliminate harmonic distortion in industrial applications. This research intends to look at different topologies of MLI, how they function, and the likelihood of obtaining good output waveforms through commutation of more than one DC source with smaller voltages. Besides, it will lead to the way to solve the challenges that traditional inverters

FOREX Publication
Open Access | Rapid and quality publishing
International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 13, Issue 1 | Pages 37-43 | e-ISSN: 2347-470X

deal with: high switching losses and harmonic distortion. To do that, the investigation shall be supported by modeling and simulation techniques.

Organization of the Article:

- *Section 2*: Discusses the fundamentals of MLI.
- *Section 3*: Explains the methodology and simulation approach.
- *Section 4*: Presents the results and compares them with existing literature.
- *Section 5*: Concludes the study and suggests future research directions.

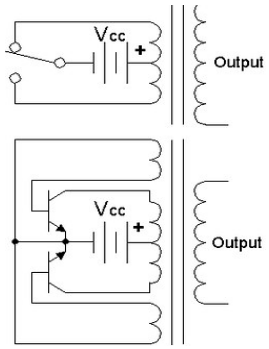

Figure 1. Basic circuit diagram of inverter

2. MULTILEVEL INVERTERS

In multilevel converter topologies, three levels are the most fundamental voltage level attainable. A converter demonstrates versatility by utilizing bidirectional switches as both a rectifier and an inverter. The inherent capability of a multilevel converter lies in its capacity to generate numerous output voltage levels, aptly termed multilevel. The total harmonic distortion (THD) converges to zero as the quantity of levels approaches an infinite value. Nevertheless, the attainable number of voltage levels is subject to limitations imposed by various constraints, including issues related to voltage imbalances, voltage clamping requirements, and considerations of both principal and operating costs.

Three primary structures of multilevel converters are used in industrial contexts. These incorporate arrangements with flowed H-spans using free DC sources, diode-cinched arrangements, and frameworks utilizing flying capacitors. While all these multilevel converter types benefit from multilevel voltage source inverters, their distinct structures and associated limitations render them more suitable for specific applications.

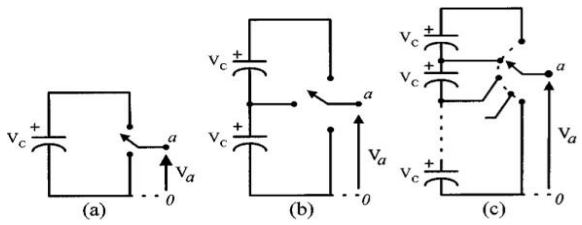

Figure 2. The inverter's single-phase leg can be configured with (a) two levels, (b) three levels, or (c) n-levels

2.1 Diode-Clamped Multilevel Inverter

The diode-clamped inverter is a frequently employed multilevel topology. It utilizes diodes as clamping devices to control the DC bus voltage and attain stepped output voltage. This inverter configuration segments the inverter capacitors into three levels with the assistance of a three-level diode clamp. Using two DC capacitors associated in series, C_1 and C_2, the DC transport voltage is uniformly dispersed across three voltage levels. The presence of clipping diodes, specifically DC_1 and DC_2, permits each changing gadget to persevere through the DC voltage, distinguished as V_{dc}.

The expected general DC connect voltage, named Vdc, controls the midpoint to be half of the complete DC interface voltage, guaranteeing that every capacitor conveys a voltage of Vdc. The making of three remarkable levels in the resulting voltage of the diode-cinched converter is conceivable exclusively through various exchanging states connected to the rating of the DC connect capacitor voltage. Two switches can be dynamic in the three-level converter at some random time. Figure 3 portrays the circuit for a diode-braced inverter, including both a three-level and a five-level inverter. The switching states for the three-level inverter are briefly outlined in *table 1*[4]-[6].

Table 1. Triggering analogy for single leg of the three-level converter

Switch Status	State	Pole Voltage
S_1=ON,S_2=ON S_1'=OFF,S_2'=OFF	S=+ve	V_{ao}=Vdc/2
S_1=OFF,S_2=ON S_1'=ON,S_2'=OFF	S=0	V_{ao}=0
S_1=OFF,S_2=OFF S_1=ON,S_2=ON	S=-ve	V_{ao}=-Vdc/2

Table 2. Diode-clamped six-level inverter voltage levels and corresponding switch states

Voltage V_{a0}	Switch State									
	S_{a5}	S_{a4}	S_{a3}	S_{a2}	S_{a1}	$S_{a'5}$	$S_{a'4}$	$S_{a'3}$	$S_{a'2}$	$S_{a'1}$
$V_5 = 5Vdc$	1	1	1	1	1	0	0	0	0	0
$V_4 = 4Vdc$	0	1	1	1	1	1	0	0	0	0
$V_3 = 3Vdc$	0	0	1	1	1	1	1	0	0	0
$V_2 = 2Vdc$	0	0	0	1	1	1	1	1	0	0
$V_1 = Vdc$	0	0	0	0	1	1	1	1	1	0
$V_0 = 0$	0	0	0	0	0	1	1	1	1	1

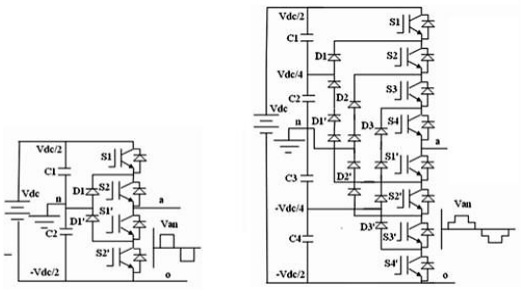

Figure 3. Configuration of the diode-clamped inverter at various levels

FOREX Publication
Open Access | Rapid and quality publishing
International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 13, Issue 1 | Pages 37-43 | e-ISSN: 2347-470X

Figure 4 depicts a three-level inverter's balanced phase voltage and line voltage. The line voltage is calculated by adding the phase voltages V_a and V_b. The three-level inverter produces a 5-level staircase waveform in the output line voltage, whereas the five-level converter yields nine levels in the line voltage. An N-level diode-clamped converter exhibits N levels in output phase voltages and 2N-1 levels in line voltage. In a steady state, an N-level diode-clamped inverter can block a voltage of Vdc/N_1. Despite each switching device's ability to block voltage Vdc, blocking the reverse voltage necessitates various ratings of blocking diodes.

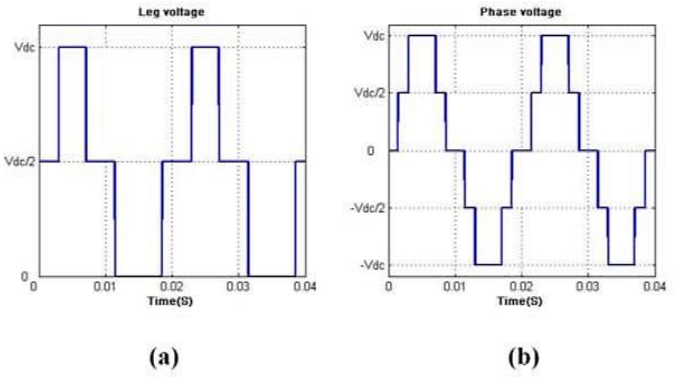

Figure 4. Phase voltage and line voltage of diode-clamped inverter three-level

For each leg of an N-level diode-braced inverter, it is typical to have 2(N-1) switching semiconductor devices, (N-1) * (N-2) clipping diodes, and (N-1) DC interface capacitors. With an increase in the voltage levels, the output voltage quality improves, approaching a waveform closely resembling sinusoidal. However, in high-level inverters, the critical aspect becomes balancing capacitor voltages. The required number of switching devices and diodes escalates with the number of levels, posing challenges for practical implementation. While utilizing PWM tending to the diode invert recuperation of clipping diodes turns into a critical plan concern. Despite being more complex in structure than the two-level inverter, the functioning of the system remains very simple.

2.2. Capacitor Clamped Structure

The diode-clipped inverter and the capacitor-cinched inverter, which is more often referred to as a flying capacitor inverter, have basic commonalities regarding their operation. Conversely, capacitors supplant bracing diodes in this course of action. The flying capacitor comprises exchanging cells braced by capacitors, interconnected in series. This geography consolidates a stepping stool design of DC side capacitors, each with an extraordinary voltage. However, the voltage steps in the output are still there because of the voltage contrast that exists between two capacitor legs that are next to one another. Presented in *figure 5* are graphical representations of capacitor-caught inverters with three levels and five levels respectively [7].

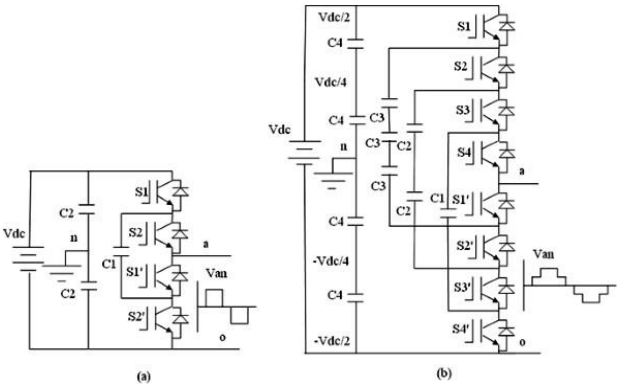

Figure 5. Several configurations of capacitor-clamped multilevel inverter circuit devices. Panel (a) shows a 3-level inverter, while panel (b) shows a 5-level inverter.

2.3. Cascaded Multilevel Inverter

The Series H Bridge Inverter, likewise perceived as the standard mode inverter (CMI), stands apart as a flexible geography in staggered inverters, tracking down applications across a wide range. Its measured quality and flexibility make it especially important in high-power situations, for example, shunt and series associated Realities regulators. One of its outstanding elements is the ability to produce almost sinusoidal voltage waveforms by reconciling different unmistakable voltage levels. The CMI's adaptability is evident in its capacity to build VAR fundamentally (volt-ampere responsive) without requiring a total redesign of the power stage. Moreover, its vigorous activity permits it to endure individual H-span converter disappointments through the fuse of extra H-span converters [8].

$$V(\omega t) = \frac{4V_{dc}}{} \sum[Cos(n\theta) + Cos(n\theta_2) + \ldots + Cos(n\theta_s)] \frac{Sin(n\omega t)}{n} \qquad (1)$$

Where n=1,3,5,7……

The magnitudes of the Fourier coefficients when normalized with respect to V_{dc} are as follows:

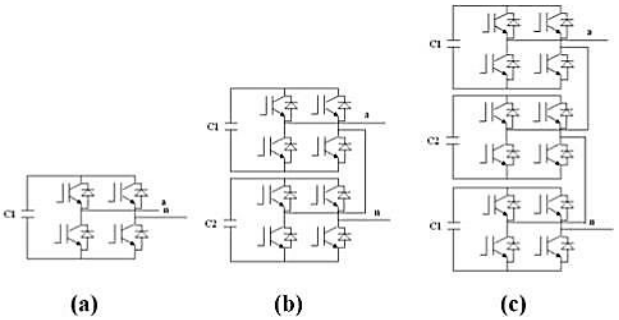

Figure 6. Monophasic configurations of cascaded inverters (a) 3-level (b) 5-level, (c) 7- level

A succession of single-stage full extensions shapes an inverter stage. A three-stage Flowed Staggered Inverter (CMI) comprises three indistinguishable stage legs made by the series association of H-span converters. These legs can create different result voltage waveforms, empowering the adjusting of AC framework stages — a capacity not present in other

FOREX Publication
Open Access | Rapid and quality publishing
International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 13, Issue 1 | Pages 37-43 | e-ISSN: 2347-470X

Voltage Source Converter (VSC) geographies with a standard DC connect. Because of its setup of series power transformation cells, this geography considers helpful adaptability in both voltage and power levels. Each full-span converter's DC connect supply is independently given, commonly cultivated through diode rectifiers taken care of by disconnected optional windings of a three-stage transformer. In medium-voltage frameworks, stage-moved transformers can supply the phones, guaranteeing high power quality at the utility association [9].

A hybrid approach integrating a 5-Level Cascaded H-Bridge Inverter with a 12-pulse thyristor rectifier demonstrates superior THD reduction. This methodology balances harmonic suppression with efficiency improvements, proving effective in high-power applications such as renewable energy integration and industrial motor drives.

3. FUNCTIONING OF THE CMLI

The configuration of the converter relies on the arrangement of single-stage inverters connected in series, with each equipped with separate direct current sources. Figure 7 illustrates the circuit schematic for various configurations of single-leg Multi level inverters. The resulting stage voltage is obtained by aggregating the voltages produced by these separate cells. A 3-level H-bridge inverter generates three output voltages from each individual inverter module: +Vdc, 0, and -Vdc. This is accomplished by sequentially alternating the capacitors to the source. The output has three levels: Vdc, Zero, and +Vdc. In the five-level configuration, the output voltage steps are -2V, +Vdc, 0, -Vdc, and +2VdcThe output voltage of the seven-level inverter spans from -3Vdc to +3Vdc. The flight of steps waveform closely resembles a sinusoidal shape, even without any constriction [10]-[12].

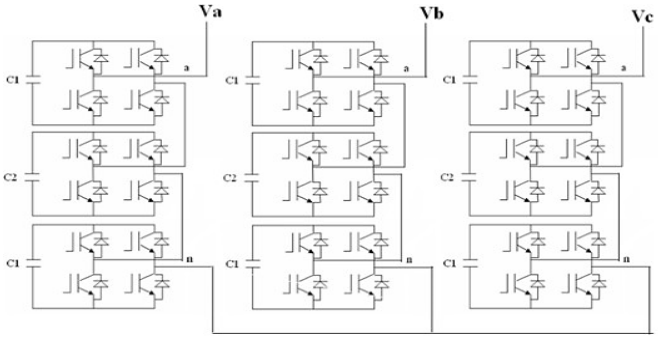

Figure 7. Y-configured three-phase 7-level cascaded H Bridge inverter

3.1 Modulation Techniques for MLI

Pulse Width Modulation, also known as PWM, is the most efficient method for achieving constant voltage battery charging. This is accomplished by switching the power devices that are controlled by the solar system controller. Take into consideration a waveform such as this: it is a voltage switching between 0v and 12v. When the solar array is regulated by pulse width modulation (PWM), the current from the array decreases in accordance with the condition of the battery and the requirements for recharging. It should come as no surprise that, given that the voltage is at 12 volts for precisely the same amount of time that it is at 0 volts, a "suitable device" that is attached to its output will perceive the average voltage and believe that it is being supplied with 6 volts, which is exactly half of 12 volts. Consequently, we are able to change the 'average' voltage by adjusting the magnitude of the positive pulse's breadth.

In the same vein, if the switches maintain the voltage at 12 for three times as long as it is at 0v, the average will be three-quarters of 12v, which is equal to 9v, as seen below. Furthermore, if the output pulse of 12v only lasts for twenty-five percent of the whole period, then the average will be. We are able to change the average voltage by modulating, or increasing or decreasing, the amount of time that the output is at 12 volts (also known as the width of the positive pulse). "Pulse width modulation" is what we are now doing. When talking previously, mentioned that the output needed to feed "a suitable device." Based on this, a radio would not function properly since it would see 12 volts followed by 0 volts, and it would most likely not function properly. The pulse width modulation (PWM) method is a suitable choice for controlling motors because a device like a motor would respond to the average [13]-[20].

3.2 Scheme for Alternate Phase Opposition Disposition in Pulse Width Modulation (APOD)

In the alternate phase opposite direction (APOD) adjustment, each adjacent transporter waveform is phase-shifted by 180 degrees in relation to its next transporter. A PWM signal is generated when the amplitude of the carrier wave exceeds that of the reference signal. The number of basic transporter waves in this strategy is contingent upon the quantity of levels present in the staggered inverters [21]. While WTGs and PVs provide intermittent power and their output cannot be controlled, DEGs can enhance system reliability. The Lyapunov stability method is a widely employed approach for determining the stability characteristics of nonlinear electrical systems [22]. A Discontinuous PWM (DPWM) strategy with frequency modulation is also reduce vibrations in asynchronous machines. The DPWM approach significantly decreases the harmonic distortion in motor drives while maintaining efficiency, offering an alternative to conventional continuous PWM methods in high-power inverter applications [23].

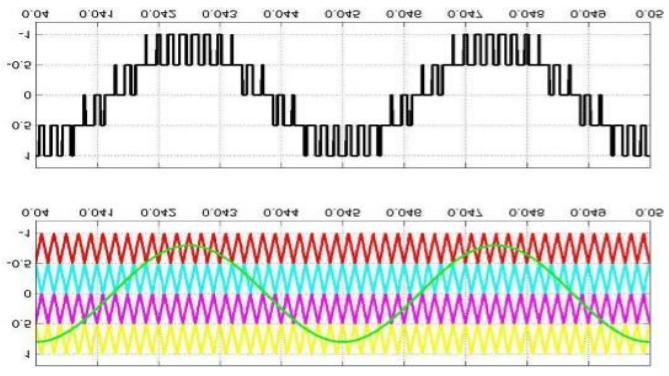

Figure 8. Modelling of carrier-based Pulse Width Modulation (PWM) scheme utilizing Amplitude and Phase-Shifted Overlapping Discrete (APOD) technique

FOREX Publication
Open Access | Rapid and quality publishing
International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 13, Issue 1 | Pages 37-43 | e-ISSN: 2347-470X

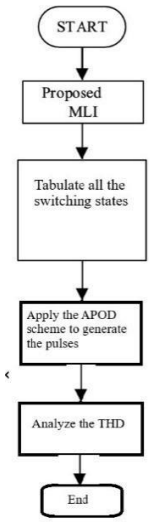

Figure 9. Flowchart for Proposed Methodology

4. MATLAB DESIGN AND SIMULATION RESULTS

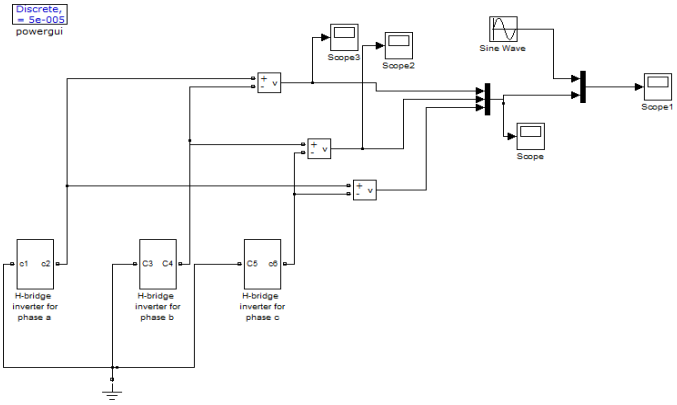

Figure 10. MATLAB design of cascaded Three-phase Three-level Inverter

The above circuit consists of three H-bridge inverters for three phases a, b, and c. Three voltmeters connected across two phases to measure line voltages and scopes to display output voltage wave forms. Sine wave and Mux are used to compare the output waveforms.

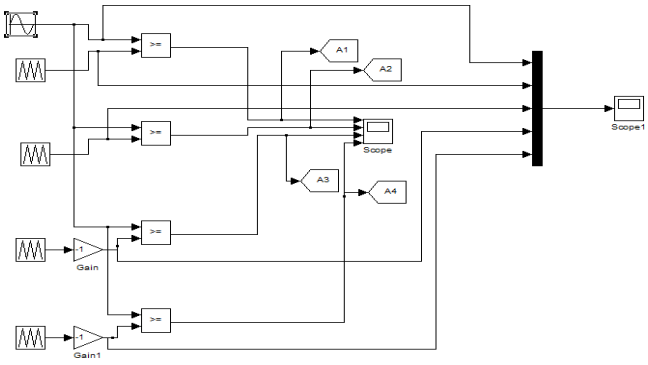

Figure 11. MATLAB design for generate trigger pulse for cascaded 3phase Five-level Inverter

The above figure is a subsystem circuit in which consists of a sine wave generator as a Reference wave and repeating sequence as a Carrier wave. These two waves are given to a comparator to produce a pulse comparing the amplitudes of two waves. Goto ports are used to connect trigger pulses to IGBT's of H-bridge.

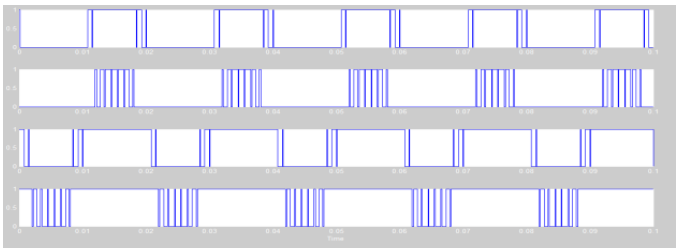

Figure 12. Trigger pulse generated for cascaded three-phase five-level inverter

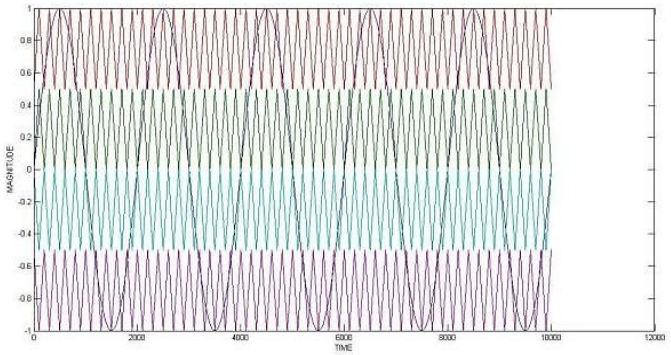

Figure 13. Simulation of sine pulse width modulation using APOD Scheme

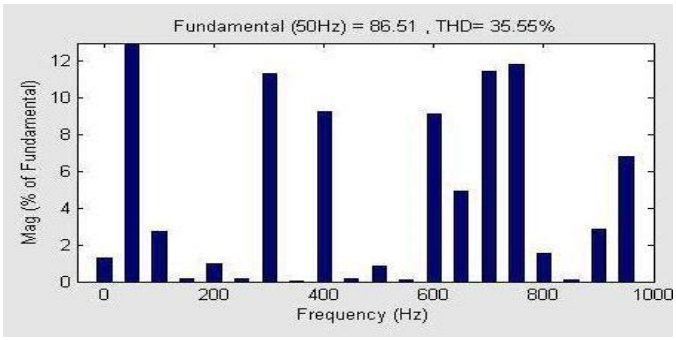

Figure 14. THD of five level cascade H-bridge Converter line Voltage

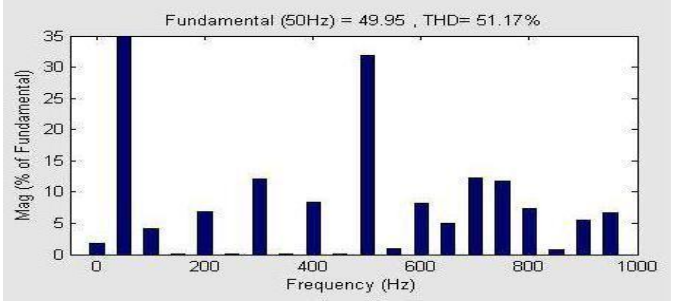

Figure 15. In a converter with five levels of diode clamping, to THD of the phase voltage as measured by the converter.

FOREX Publication
Open Access | Rapid and quality publishing
International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 13, Issue 1 | Pages 37-43 | e-ISSN: 2347-470X

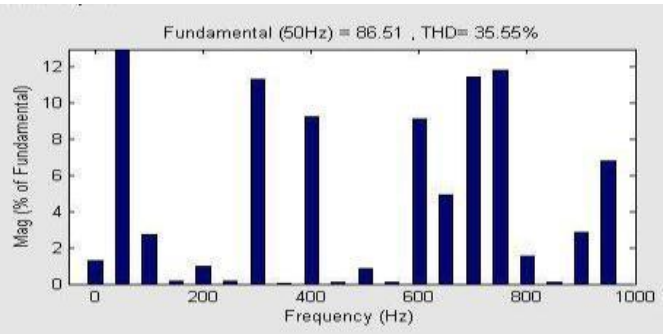

Figure 16. Five-level diode clamped converter line voltage THD

A number of topologies are shown by graphical plots of the inverter phase voltage and line voltage, which are part of the simulation results. However, to present a more extensive understanding, the results are now described as being as follows: It is observed from the waveforms of the output for each of the various MLI topologies that THD decreases as the number of levels increases. Plotted and presented in comparison to other similar works are the values of THD of various inverter topologies. The 5-Level Cascaded H-Bridge inverter THD is 35.55%, as presented in Table 1. It is slightly below the 36.00% that was also reported in previous research. Likewise, the 5- Level Capacitor Clamped inverter is capable of obtaining a THD of 24.33%, which is noticeably lower than the 25.10% also obtained in previous attempts. With a THD of 15.67%, the 5-Level Diode Clamped inverter performs the best, beating the 16.20% that was originally measured in earlier study. The results of this study prove that the approach that was suggested is efficient in minimizing harmonic distortion. In addition, an examination of the effect of modulation index and switching frequency on waveform quality is conducted within this study. To compare its performance for the sake of benchmarking, the APOD-PWM technique proposed is compared with other PWM schemes. As found out, incorporating more levels and better modulation technique gives a significant improvement in the efficiency of the inverter as well as the quality of the waveform it generates.

Table 3. Design parameters for cascaded H-bridge multilevel inverter

S. No.	Parameter	Values
1	Input voltage	130 V
2	Load	2 R = 50 Ω
3	Switching frequency	2 kHz
4	Modulation index	0.8

The design parameters for the cascaded H-bridge multilevel inverter as mentioned in *table 3* indicate an optimized setup for efficient power conversion. With an input voltage of 130V, the inverter operates within a medium-power range, ensuring a stable DC supply. The resistive load of 50Ω suggests balanced operation, facilitating reliable power delivery. A switching frequency of 2 kHz strikes a balance between minimizing switching losses and improving output waveform quality. The chosen modulation index of 0.8 ensures that the inverter operates at 80% of its maximum output voltage, optimizing performance while maintaining low harmonic distortion. Overall, these parameters contribute to efficient voltage control, stable operation, and minimized losses in the inverter system.

Table 4. Comparison of THD for Various MLI Topologies

Topology	THD (%) (Proposed Study)	THD (%) (Previous Studies)
5-Level Cascaded H-Bridge	35.55	36.00 [1]-[3]
5-Level Capacitor Clamped	24.33	25.10 [1]-[3]
5-Level Diode Clamped	15.67	16.20 [1]-[3]

The total harmonic distortion (THD) values in the table4 highlight the improved performance of the proposed study compared to previous studies for different 5-level multilevel inverter topologies. The 5-level cascaded H-bridge inverter shows a slight reduction in THD (35.55% vs. 36.00%), indicating a minor improvement in output waveform quality. The 5-level capacitor-clamped topology demonstrates a more noticeable reduction in THD (24.33% vs. 25.10%), suggesting better harmonic suppression. The 5-level diode-clamped inverter achieves the lowest THD (15.67% vs. 16.20%), making it the most effective among the three topologies in minimizing harmonics. Overall, the proposed study enhances harmonic performance across all topologies, contributing to improved inverter efficiency and power quality.

5. CONCLUSION

This paper discussed about MATLAB/Simulink of Alternate Phase Disposition (APOD) PWM modulation to explore MLI topologies. Their waveform quality and harmonic distortion performance was the primary concern. Total harmonic distortion (THD) decreases significantly as the count of an inverter's levels increases, improving performance. The Cascaded H-Bridge and Capacitor Clamped topologies contained more harmonics compared to the 5-Level Diode Clamped inverter, which had the lowest THD value of 15.67%. Comparing the new method to previous studies validated its accuracy and effectiveness. The study also studied how modulation index and switching frequency affect output waveforms, highlighting the benefits of optimizing modulation techniques. The APOD-PWM method improved inverter performance and reduced switching losses. To improve inverter efficiency, future research can optimize modulation, include machine learning-based predictive control, and investigate hybrid topologies. Practical implementation and experimental validation of simulated results would provide deeper insights into real-world applications, ensuring MLI reliability and scalability in industrial and renewable energy systems.

REFERENCES

[1] Rodriguez, J., Lai, J.-S., & Peng, F. Z. (2002). Multilevel inverters: a survey of topologies, controls, and applications. IEEE Transactions on Industrial Electronics, 49(4), 724-738.
[2] Kouro, S., Malinowski, M., Gopakumar, K., Pou, J., Franquelo, L. G., Bin

FOREX Publication
Open Access | Rapid and quality publishing
International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 13, Issue 1 | Pages 37-43 | e-ISSN: 2347-470X

Wu, Rodriguez, J., Perez, M. A., & Leon, J. I. (2010). Recent advances and industrial applications of multilevel converters. IEEE Transactions on Industrial Electronics, 57(8), 2553-2580.
[3] Marzband, M., Gomes, C., & Fernando, T. (2012). Multilevel inverter: A review of literature. Renewable and Sustainable Energy Reviews, 16(5), 3586-3599.
[4] Nabeel, F., & Mekhilef, S. (2016). Recent advances in multilevel inverter: A review. Renewable and Sustainable Energy Reviews, 56, 354-362.
[5] Dasgupta, S., & Sahoo, S. K. (2016). A comprehensive review of multilevel inverter topologies. Renewable and Sustainable Energy Reviews, 62, 1193-1210.
[6] Banaei, M. R., Zolghadri, M. R., & Seyedi, H. (2018). A review of multilevel inverter topologies and applications. Renewable and Sustainable Energy Reviews, 81, 1814-1827.
[7] Carrasco, J. M., Franquelo, L. G., Bialasiewicz, J. T., Galvan, E., Guisado, R. C., Prats, M. A., & Leon, J. I. (2006). Power-electronic systems for the grid integration of renewable energy sources: A survey. IEEE Transactions on Industrial Electronics, 53(4), 1002-1016.
[8] Ghosh, A., & Qu, Y. (2009). Power electronics and motor drives in electric, hybrid electric, and plug-in hybrid electric vehicles. IEEE Transactions on Industrial Electronics, 56(11), 4496-4507.
[9] Peng, F. Z. (2003). Z-source inverter. IEEE Transactions on Industry Applications, 39(2), 504-510.
[10] Gopakumar, K., Nabeel, F., Franquelo, L. G., Leon, J. I., & Rodriguez, J. (2011). Recent advances and industrial perspectives of multilevel converters. IEEE Transactions on Industrial Electronics, 58(9), 3973-3985
[11] Malinowski, M., Gopakumar, K., Rodriguez, J., & Pérez, M. A. (2010). A survey of cascaded multilevel inverters. IEEE Transactions on Industrial Electronics, 57(7), 2197-2206.
[12] Zargari, N., Yatim, A. H. M., Rahim, N. A., & Ping, H. W. (2010). A review of control strategies for voltage-source inverters in variable-speed wind energy conversion systems. IEEE Transactions on Industrial Electronics, 57(8), 2581-2593.
[13] Liu, C., Wu, B., & Kang, Y. (2015). A review of three-phase multilevel inverter topologies. IEEE Transactions on Industrial Electronics, 62(3), 1742-1754.
[14] Mohammadi, J., Nor, K. M., & Radzi, M. A. M. (2013). A review of recent advances in multilevel inverter. Renewable and Sustainable Energy Reviews, 21, 834-852.
[15] Aghazadeh, A., & Bakhshai, A. (2015). A review of flying capacitor multilevel inverter (FCMLI): Topologies, applications, and control strategies. IEEE Transactions on Power Electronics, 30(1), 15-36.
[16] Kouro, S., Cortes, P., Vazquez, S., Kouro, H., & Rodriguez, J. (2012). Model predictive control—A simple and powerful method to control power converters. IEEE Transactions on Industrial Electronics, 59(1), 158-169.
[17] Ebrahimzadeh, A., Hajizadeh, A., & Toliyat, H. A. (2014). A comprehensive review on cascaded H-bridge multilevel inverter: Topology and applications. IEEE Transactions on Industrial Electronics, 61(3), 1281-1295.
[18] Mathews, M., Ramesh, B., & Sreedhar, T. (2022). Minimization of THD in Nine Level Cascaded H-Bridge Inverter Using Artificial Neural Network. *International Journal of Electrical and Electronics Research*, 10(2), 45-52.
[19] Naayagi, R. T., & Ramachandran, K. (2015). A survey on multilevel inverter topologies and control strategies. International Journal of Engineering Research and Applications, 5(2), 1-7.
[20] Sadoughi, M., Pourdadashnia, A., Farhadi-Kangarlu, M., & Galvani, S. (2021). Reducing Harmonic Distortion in a 5-Level Cascaded H-bridge Inverter Fed by a 12-Pulse Thyristor Rectifier. *International Journal of Electrical and Electronics Research*, 9(4), 112-119.
[21] Farhadi Kangarlu, M., & Saffari, H. (2014). A comprehensive review on voltage source inverters topologies and control strategies. Journal of Power Technologies, 94(1), 47-60.
[22] S. Penta, S. Venkateshwarlu, and K. N. Sujatha, "Lyapunov based Control Strategy for DFIG based Wind Turbines to Enhance stability and Power," Int. J. Electr. Electron. Res., vol. 11, no. 4, pp. 898–903, 2023, doi: 10.37391/ijeer.110403.
[23] Ruiz-Gonzalez, A., Heredia-Larrubia, J. R., Perez-Hidalgo, F. M., & Meco-Gutierrez, M. (2024). Discontinuous PWM Strategy with Frequency Modulation for Vibration Reduction in Asynchronous Machines. *International Journal of Electrical and Electronics Research*, 12(1), 78-85.