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Investigation of Discontinuous PWM Schemes for Power Loss Minimization in SiC Three-Phase Inverter

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ABSTRACT- SiC inverters are considered highly attractive in power electronic applications such as electric vehicles, industrial motor drives, and photovoltaic (PV) systems. These SiC-based inverters present greater thermal conductivity, enabling operation at higher temperatures, frequencies, and voltages with reduced losses. This study utilizes the PLECS platform to analyze and simulate power losses in SiC inverter under two decided assumptions. In the first case, at high modulation indices, DPWMMAX, DPWM1, and DPWM2 demonstrate approximately 43% lower power losses compared to other techniques. In the second case, at low power factors, these same modulation schemes show approximately 35% reduction in power losses. Among the studied techniques, DPWM2 shows superior performance in terms of minimizing power losses across both cases.

Keywords: Pulse width modulation (PWM), Discontinuous pulse width modulation (DPWM), Silicon carbide (SiC).

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1. INTRODUCTION

There have been lots of research and development regarding the improvement of performance and minimization of losses of three-phase inverters using discontinuous pulse width modulation (PWM) technique over the past few decades. An important contribution in this regard is the formulation of a generalized discontinuous pulse width modulation method, namely GDPWM technique with simple and effective structure, which outperforms existing state of the art waveform, switching loss and overmodulation performances [1,2]. The paper gives several analytical techniques to find out the optimal modulation signals for the carrier-based PWM schemes for three-phase voltage inverters to achieve the above results, for both balanced and unbalanced voltages [3]. These techniques allow for a precise control and optimization of the inverter. For example, by reducing the switching losses in the power converters [4]. The optimal switching frequency of discontinuous pulse width modulation (PWM) is studied, and the analytical rules are derived and experimentally verified to minimize the semiconductor losses due to switching. The switching losses can therefore be cut in half compared with the continuous PWM [5]. In addition, a high efficiency discontinuous pulse width modulation technique for active power filters (APFs) called GD-PWM is proposed. GD-PWM dynamically adapts the duration of the shaping clamp for each change of the instantaneous current vector position. This leads to significant suppression of the switching losses in APFs [6,7]. Hence this contribution presents a novel direct digital technique to optimize the quality of discontinuous pulse width modulation (DPWM) implementation on embedded systems to minimize the switching losses of the inverter, which is particularly suitable in embedded control systems, showing the advantages of free from load power factor, working securely in the both steady-state and dynamic conditions, and efficient computation [8]. The algorithm's effectiveness has been confirmed by both simulations and experiments SiC power modules show promise in power-electronic systems owing to their superior performances, high blocking voltages and fast switching ability.

This paper describes the design of a three-phase high-efficiency SiC inverter, characterizes the switching performance of the inverter through experiments, and investigates the limitations of the switching performances of SiC MOSFETs in a three-phase PWM inverter for induction motor drives [9,10]. It further looks at two different kinds of hybrid switching devices, both of which integrate SiC and Si active switches, which are expected to provide higher efficiency than the conventional Si devices [11]. The paper further carries out analysis on the application of SiC-based inverter on high-speed motor applications, where it is seen that the inverter loses can be significantly reduced while also improving the motor's efficiency [12,13]. Other research considerations are focused on reducing ripple current, analyzing power losses and efficiency, online monitoring of SiC power MOSFETs, and evaluation of various PWM types on losses as well as on thermal stresses in SiC power modules. [14-17]. A new carrier-based discontinuous pulse width modulation (DPWM) technique for neutral-point diode clamped (NPC) three-level inverter is proposed to minimize the common mode voltage (CMV) and switching losses [18]. Experimental results obtained for SiC-based 2L-VSI motor drives indicate the effectiveness of generalized carrier-based PWM methods. The modified space vector approach for DPWM, MSL-DPWM, increases the inverter efficiency and reduces the THDs and the

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CM current in the motor drives in the V/f control. These reductions are more significant in low power factors [19]. This paper presents the parallelization of Si IGBT and SiC MOSFET together in very main drive inverters for electric vehicles. Power loss analyses include models for circuit and power loss, aided by a multi-objective mathematical model to equip identification for device selection and load power design. Also, the reported topology offers lower power losses and higher efficiency [20]. The article presents a novel carrier selection strategy for a voltage source inverter, reducing dc-link capacitor current via GDPWM [21,22]. This paper presents an analytical formulation for predicting the efficiency of three-phase inverters using SiC MOSFETs. Experimental validation shows the designed inverter achieves over 99% efficiency [23]. this study presents a comprehensive overview of various discontinuous pulse-width modulation techniques and reducing losses, and improving efficiency in Sic three-phase inverters. A study was conducted to investigate the impact of switching frequency and power factor on power losses in Sic three-phase inverters using PLECS platform, opening up new possibilities for advanced power electronic systems and applications.

2. BASIC OPERATION OF PULSE WIDTH MODULATION

a reference signal voltage (Vref) is utilized for comparison with triangular carriers. The intersection points between Vref and the carrier wave determines the timing of the rising and falling edges of the output pulse voltage. This method allows for accurate approximation of the reference voltage, as the comparison is made directly between the reference signal and the carrier signal as shown in *figure 1* to obtain the gate pulses for the inverter drive. The modulation index is determined by dividing the peak amplitudes of reference signal and the carrier signal.

$$m = \frac{Vref}{V\ carrier} \qquad (1)$$

3. DISCONTINUOUS PULSE-WIDTH MODULATION SCHEMES

The implementation of the DPWM technique produces the least switch losses. This consists of a reference signal voltage (Vref) which is compared to triangular carriers for the evaluation of the timing of the output pulse voltage. The reference signal Vref derives its synthesis from injecting Ving with its corresponding fundamental signal. Ving is given by *equation (2)*, and according to the value of *k*, different DPWM techniques can also be synthesized.

$$Ving = k(1 - \max) + (1 - k)(-1 - \min) \qquad (2)$$

max: maximum of instantaneous fundamental three phase signals (Va, Vb, Vc)

min: minimum of instantaneous fundamental three phase signals (Va, Vb, Vc)

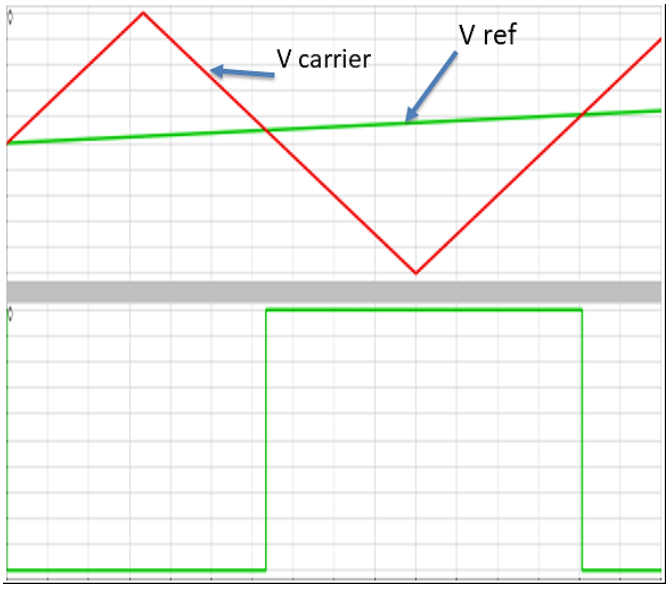

Figure 1. Operation of pulse width modulation

3.1. DPWMMAX Scheme

This technique is implemented by substituting the value of K equal to one in *equation 2*, resulting in an injected signal combined with a fundamental signal as shown in *figure 2*. To obtain a control signal for comparison with a carrier signal.

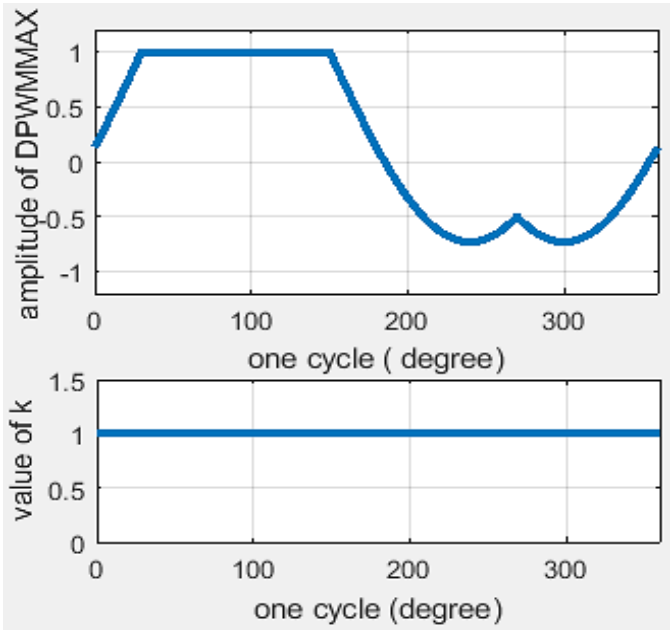

Figure 2. Control signal for DPWMMAX technique at *m=1* and value of *k*

3.2. DPWMMIN Scheme

This technique is implemented by substituting the value of K equal to ZERO in *equation 2*, By combining the injected signal with a fundamental signal, as depicted in *figure 3*, a control signal is generated for the purpose of comparing it with a carrier signal.

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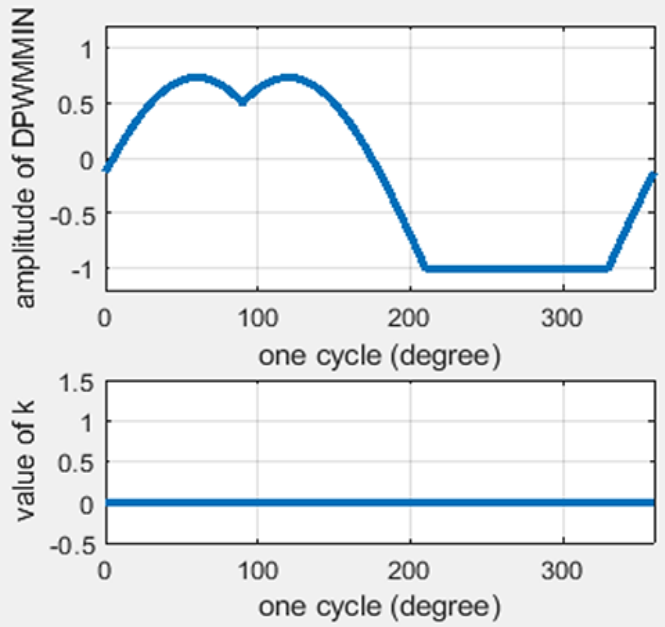

Figure 3. control signal for DPWMMIN technique at m=1 and value of *k*

3.3. DPWM1 Scheme

This technique is then realized by substituting a K value represented as a pulse, as shown in *figure 4*, into *equation 2*. The control signal, as shown in *figure 4*, is a combination of injected signal with the basic, which is to compare it with a carrier signal.

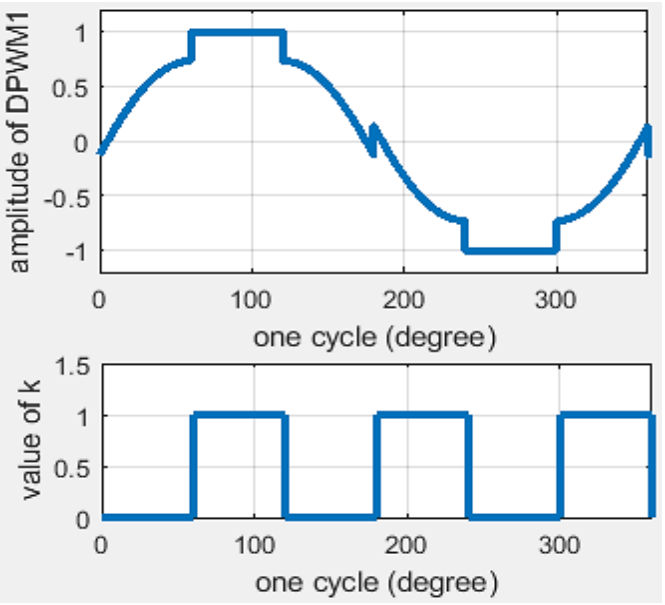

Figure 4. control signal for DPWM1 technique at m=1 and value of *k*

3.4. DPWM2 Scheme

The method involves substituting the desired *K* value, as represented by the pulse in *figure 5*, into *equation 2*. Following this, the combination of injected signal and basic signal gives rise to a control signal, as depicted in *figure 5*. Input from the control signal is then used along with a carrier signal for comparison.

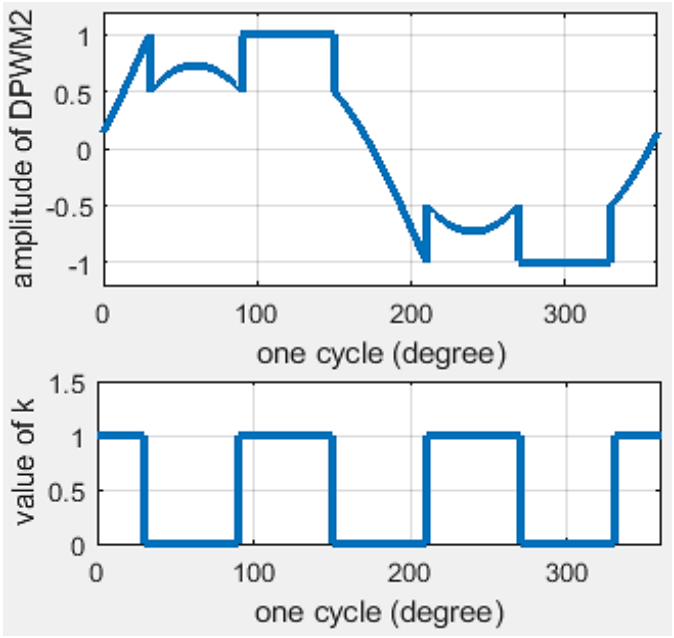

Figure 5. control signal for DPWM2 technique at m=1 and value of *k*

3.5. DPWM3 Scheme

This technique extracts the pulsatile K value from *equation 2* by substitution as shown in *figure 6*. The merging of the injected signal with the fundamental signal acts as a means to generate a control signal. In *figure 6*, this control signal is displayed which will compare with a carrier signal.

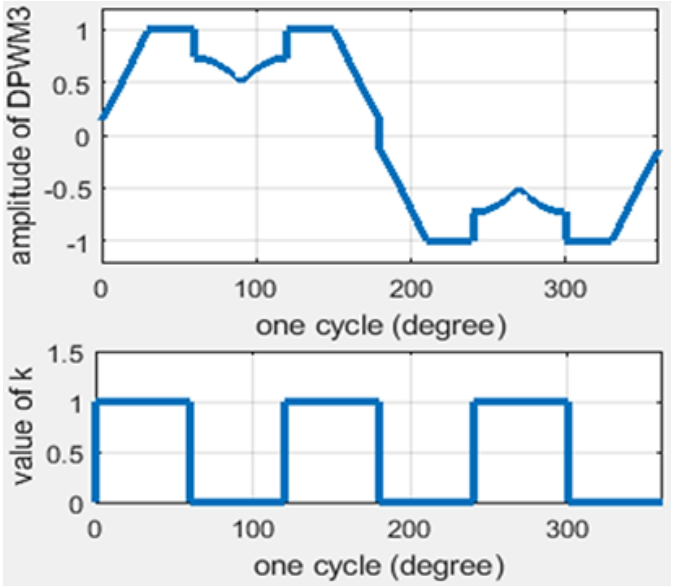

Figure 6. control signal for DPWM3 technique at m=1 and value of *k*

3.6. DPWM4 Scheme

This method is done by putting the changing *K* value, seen in *figure 7*, into *equation 2*. The mix of the added signal and the main signal, shown in *figure 7*, results in a control signal. *Figure*

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7 illustrates this control signal, which is used to compare with a carrier signal.

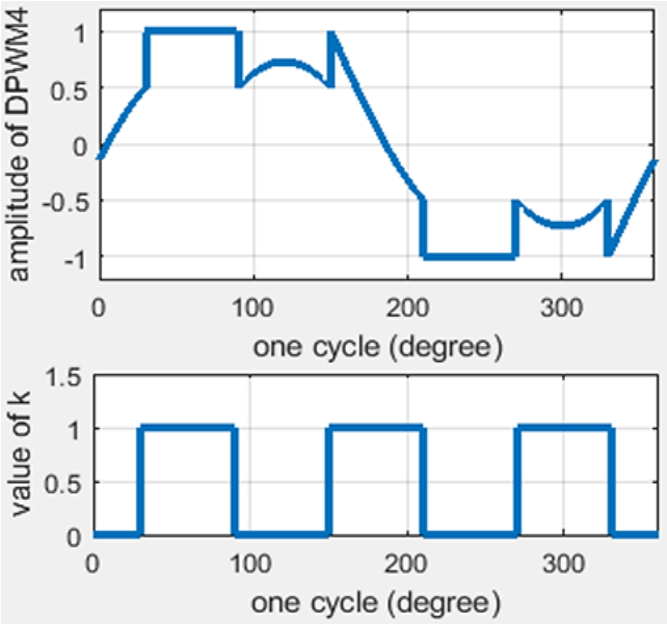

Figure 7. control signal for DPWM4 technique at m=1 and value of k

4. CALCULATION SWITCHING AND CONDUCTION LOSSES USING THERMAL MODELLING

Switching losses occur because devices do not change from on-state to off-state instantly. During these transitions, high current and voltage values happen, causing power losses. In other simulation programs, determining switching losses can be hard due to the need for very detailed semiconductor models. Also, tiny simulation time-steps are required because each switching transition lasts only a few hundred nanoseconds. The PLECS platform addresses this issue by using the fact, in a given circuit, the current and voltage during transitions, as well as total losses energy, mostly rely on the conditions before and after switching and the temperature of the device. Additionally, users can add custom function arguments in the Turn-on loss and Turn-off loss sections of the thermal editor, which can be shown as 3D look-up tables. These losses are calculated using 3D look-up tables represented in the Figure 8 as a 3D surface for the SiC MOSFET (C3M0280090D) and its diode body. The power loss model for the SiC MOSFET (C3M0280090D) and its diode body was derived from the manufacturer's datasheet and application notes. For the (C3M0280090D) device, the switching and conduction losses are characterized using the manufacturer-provided equations and curves. In simulation these particular losses are determined by means of the above presented tables by linear interpolation and only in the domain of the input values, where they are valid enhancing either on state current or pre switching and post switching current or voltage as well any achievable junction temperature. Should an input value be beyond the range, PLECS will extrapolate on the first or the last pair of index values for the losses.

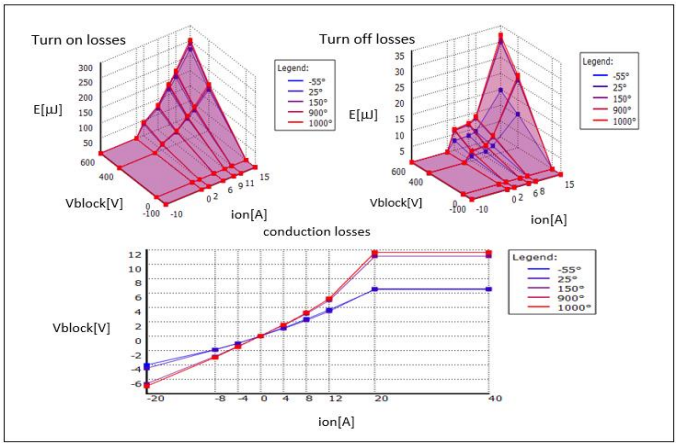

Figure 8. Switching and conduction losses

5. SIMULATION

A simulation was conducted for a circuit using a platform PLECS in two. In the first case, the power factor remained constant at unity with varying modulation index for each technique. In the second case, the power factor varied and modulation index remained constant at unity for each technique. The simulation parameters were as follows in *table 1*.

Table 1. The parameters of simulation

Parameters	values
Value of dc supply	310V
Three-phase R-L load connected in star configuration	R=10Ω , L=10mH
Ambient of temperature	50º Celsius

6. RESULTS & DISCUSSION

6.1 First case

The results indicated six different 3D surface plots labelled as DPWMMAX, DPWMMIN, DPWM1, DPWM2, DPWM3, and DPWM4 as shown in *figure 9*. X-axis appears to be a continuous variable ranging from 0 to 1. This would represent a modulation index. Y-axis is, representing different frequencies (1 kHz to 2 MHz). This indicates switching frequencies.

• *Z-axis ranges from 0 to 600*. This would represent power losses in watt. In the first case, all DPWM approaches exhibited higher losses at greater modulation indices and switching frequencies. When the switching frequency is below 100 kHz, all the schemes examined generally levels of power losses. The DPWM2 scheme appears to have lower power losses than the others. In contrast, the DPWM4 scheme seems to have slightly higher power losses compared to the other schemes being evaluated in this frequency region. However, DPWMMAX, DPWM1 and DPWM2 demonstrated a less gradual rise in losses compared to other techniques. Specifically, at the peak power losses points above 100 kHz, these three schemes achieved a 43% reduction in power losses compared to the other

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approaches. Furthermore, within this higher frequency range above 100 kHz, the DPWM2 scheme specifically exhibited slightly lower power losses than both the DPWMMAX and DPWM1 techniques. Alternatively, DPWMMIN, DPWM3 and DPWM4 exhibited considerably steeper increases in power losses at higher frequencies above 100kHz. These strategies likewise showed higher sensitivity, with losses sharply climbing alongside modulation index changes and switching frequencies. The results presented in *table 2* demonstrate that for first case.

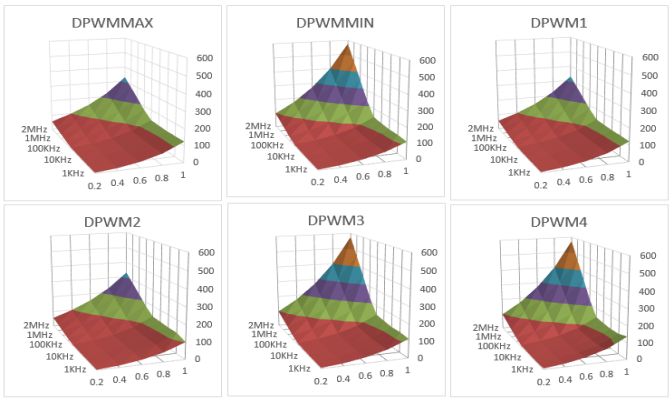

Figure 9. The results of first case

Table 2. Power loss reduction percentages for first case

Schemes	Low modulation index and switching frequency	medium modulation index and switching frequency	High modulation index and switching frequency
DPWMMAX	7%	19%	43%
DPWMMIN	9%	0%	0%
DPWM1	9%	19%	43%
DPWM2	17%	19%	43%
DPWM3	9%	0%	0%
DPWM4	0%	0%	0%

6.2 Second case

The results indicated six different 3D surface plots labeled as DPWMMAX, DPWMMIN, DPWM1, DPWM2, DPWM3, and DPWM4 as shown in figure 10 as second case. X-axis representing different frequencies (1 kHz to 2 MHz). This indicates switching frequencies. Y-axis is appearing to be a continuous variable ranging from 0 to 1. This would represent a power factor.

• *Z-axis ranges from 0 to 3000*. This would represent power losses in watt. When the switching frequency is below 100 kHz, all DPWM schemes Shows the highest power losses at lower power factors. DPWM2 Show less losses than among all schemes at lower power factors and higher power factor. DPWM2 Show about 25% less than DPWM4 and DPWM2 show about 12% less than DPWM1 at lower power factor 0.2 and switching frequency 1KHz. DPWM2 Show about 17% less than DPWM4 and DPWM2 show about 8% less than DPWM1 at higher power factor 0.8 and switching frequency 1KHz. When the switching frequency is above 100 kHz power losses increase. However, DPWMMIN, DPWM3, DPWM4 schemes Shows the highest power losses at lower power factors, DPWMMAX, DPWM1, DPWM2 show maximum reduction of power losses about 35% compare with other DPWM schemes at 0.4 power factor and 2MHz switching frequency. DPWMMAX, DPWM1, DPWM2 show maximum reduction of power losses about 45% compare with other schemes at unity power factor and 2MHz switching frequency. The results presented in *table 3* demonstrate that for second case.

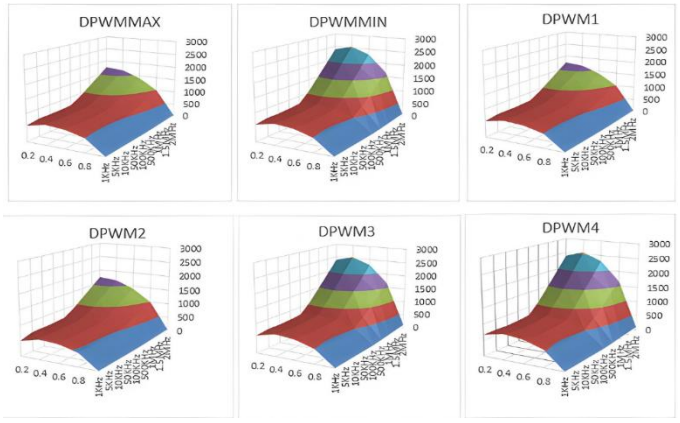

Figure 10. The results of second case

Table 3. Power loss reduction percentages for second case

Schemes	Low power factor and switching frequency	High power factor and low switching frequency	Low power factor and high switching frequency	unity power factor and high switching frequency
DPWM MAX	15%	8%	35%	45%
DPWM MIN	12%	9%	0%	0%
DPWM1	16%	10%	35%	45%
DPWM2	25%	17%	35%	45%
DPWM3	11%	8%	0%	0%
DPWM4	0%	0%	0%	0%

7. CONCLUSIONS

The analysis of these 3D surface plots provides insights into the performance of different DPWM strategies concerning modulation index and switching frequency. DPWMMAX, DPWM1 and DPWM2 appear to offer lower power losses, making them suitable for efficiency-critical applications. DPWMMIN, DPWM3 and DPWM4 might be less desirable

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due to higher losses. the study has shown that power losses increase with lower power factor and higher switching frequency for all discontinuous PWM strategies. DPWMMAX, DPWM1 and DPWM2 exhibited a more gradual increase in power losses as power factor decreased and switching frequency increased, remaining efficient across varying conditions. In contrast, DPWMMIN, DPWM3 and DPWM4 displayed pronounced peaks in power losses at lower power factors and higher switching frequencies beyond 100kHz, demonstrating higher sensitivity. For these strategies, losses increased substantially with lower power factors and higher frequencies due to more frequent switching events. The gradual characteristics of DPWMMAX, DPWM1 and DPWM2 suggest they maintain reasonable efficiencies over a wide range of operating conditions compared to the other strategies. Therefore, these three DPWM approaches appear most suitable where lower power factors and high switching frequencies may be encountered.

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