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A Switched Capacitor – Inductor High Gain DC-DC Converter for Solar PV Applications

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ABSTRACT- A new switched capacitor-inductor high-voltage gain DC-DC boost converter is presented in this work. A switched-inductor cell is used at input side of the suggested converter to lessen input current source ripples, which is a crucial issue in PV systems for high-reliability applications. To further increase voltage-gain and reduced voltage stress across the converter's power switches, a switched-capacitor cell is employed at the output side of the converter. This is a critical component in applications like to extended lifespan of the PV panel and other suggested converter parts, especially semiconductor devices. To validate the efficacy of the presented DC-DC converter, extensive simulations are conducted by using PSIM simulation tools. The results obtained from these simulations serve as a robust confirmation of the converter's capabilities, showcasing its ability to obtain high voltage gain with reduced power components at various duty cycles.

Keywords: DC-DC converter; photovoltaic; high gain; switched capacitor; harmonic distortion.

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1. INTRODUCTION

In modern times, there is a global shift towards renewable energy sources for power generation, with photovoltaic (PV) energy taking centre stage. Despite its promise, PV systems typically generate lower output compared to conventional energy sources, posing challenges for various applications. To overcome this, DC-DC Boost converters are used to elevate the lower DC voltage to higher levels suitable for practical use. The voltage boosting capacity depends on the specific DC-DC converter topology, which has seen significant advancements with the development of diverse designs to meet different application requirements. These converters, also known as step-up DC-DC converters, are critical in improving the efficiency and viability of renewable energy systems [1][2].

PV systems offer a sustainable alternative to fossil fuel-based power generation by utilizing solar energy, reducing environmental impact, and decreasing reliance on finite resources. However, their efficiency largely hinges on the performance of associated power conversion circuits, particularly DC-DC converters, which optimize power transfer from PV panels to loads or energy storage systems [3]. The output from DC-DC converters is often fed into DC-AC inverters, where various topologies and pulse width modulation (PWM) techniques are employed for efficient control [4]-[10]. Among DC-DC converter topologies, boost converters are widely used in PV systems due to their ability to step up voltage levels efficiently. Traditional boost converters rely on inductive elements, but they are often limited by their size, weight, and cost. Recent innovations have introduced switched capacitor-based converters, which address these issues by offering reduced size, weight, and cost, alongside improved efficiency [11]-[16]. The development of switched capacitor-inductor (SCI-HG) DC-DC boost converters aims to meet the stringent demands of modern PV applications, including maximum power point tracking (MPPT), partial shading, and varying load conditions, making them ideal for enhancing PV system performance.

This paper presents a novel approach towards enhancing the performance of switched capacitor-based boost converters by integrating an inductor into the circuit topology. The proposed switched capacitor-inductor high gain (SCI-HG) DC-DC boost converter aims to combine the benefits of both switched capacitor and inductor-based converters while mitigating their respective limitations. By leveraging the unique characteristics of both components, the SCI-HG boost converter achieves high voltage gain, improved efficiency, reduced component count, and enhanced reliability, making it well-suited for various PV applications.

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2. PROPOSED SWITCHED CAPACITOR INDUCTOR HIGH GAIN DC-DC TOPOLOGY

The illustration above showcases the recommended converter configuration, demonstrating the designed high gain converter is shown in *Fig. 1*. The circuit comprises 02 power switches labelled M_1 and M_2, along with 05 capacitors (C_1 to C_4, and CO), 03 inductors (L_1, L_2, and L_3), and 06 power diodes (D_1 to D_6). The primary power switch is designated as M_2, while M_1 serves as an auxiliary switching element. Both power switches operate concurrently, being activated and deactivated simultaneously at identical intervals.

The auxiliary switch assumes a pivotal role in alleviating the voltage stress imposed on the primary switch. An analysis of the continuous conduction mode (CCM) of the presented converter is conducted with a focus on the load side. Within CCM, this converter operates in two distinct modes, which are explained as follows.

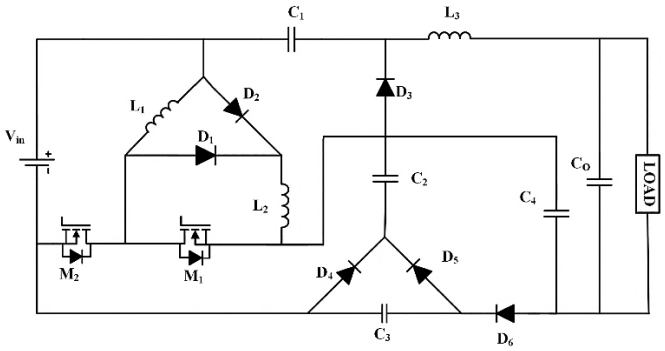

Fig. 1. Proposed Switched capacitor-inductor High Gain DC-DC Converter

2.1. Mode-I operation of proposed converter

When the switches are engaged, diodes D_2, D_3, D_4, and D_6 transition to the off-state, while diodes D_1 and D_5 switch to the on-state. Diodes D_2 and D_3, with their anode pins connected to the ground, remain in the off-state. In this arrangement, input inductors L_1 and L_2 are linked in parallel and gradually charged by the input voltage. In this phase, capacitor C_3's voltage discharges into capacitor C_2 *via* diode D_5, and capacitor C_4 is likewise discharged due to the grounding of their positive terminals. Simultaneously, inductor L_3 initiates charging since its voltage is positive, and the current from capacitor C_1 is redirected into this inductor.

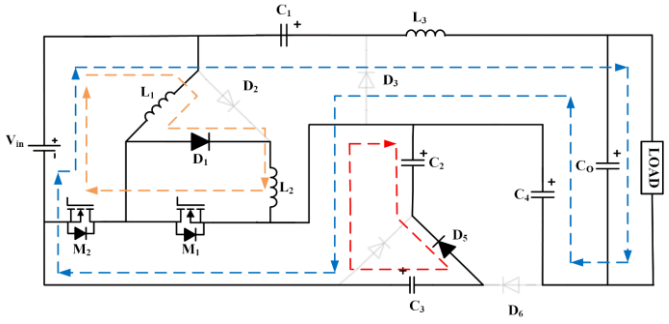

Fig. 2. Mode-1 Operation of proposed converter

By employing Kirchhoff's voltage law (KVL) to analyze this operational state and considering the capacitors' polarities, the following equations can be derived. This dynamic circuit state showcases a sophisticated interplay of components where switches, diodes, capacitors, and inductors interact to manage voltage and current flows effectively. Understanding the intricacies of such configurations is crucial for optimizing circuit performance and ensuring reliable operation in various applications ranging from power electronics to renewable energy systems.

$$V_{in} = V_{L1} = V_{L2} \quad (1)$$

$$V_{in} = V_{L2} + V_{C2} - V_{C3} \quad (2)$$

$$V_{C2} - V_{C3} = 0 \rightarrow V_{C2} = V_{C3} \quad (3)$$

$$-V_{in} - V_{C1} + V_{L3} + V_o - V_{C4} = 0 \quad (4)$$

$$V_{L3} = V_{in} + V_{C1} - V_o + V_{C4} \quad (5)$$

In the given equations, the source and output voltages are symbolized as Vin and V_O, respectively. The voltage across the inductors L_1, L_2, and L_3 is denoted as V_{L1}, V_{L2}, and V_{L3}, while the voltages across the capacitors C_1, C_2, C_3, C_4, and C_O are indicated by V_{C1}, V_{C2}, V_{C3}, V_{C4}, and V_{CO}, respectively.

2.2. Mode-II operation of proposed converter

For this mode of operation, the equivalent circuit depicted in *figure 3*, which illustrates the scenario. Here, the switch is deactivated, and power diodes D_1 and D_5 transition to the off-state, while the other diodes switch to the on-state. With consideration to the serial connection of the input inductors, the voltages across two inductors L_1 and L_2 commence discharging, while the voltages across capacitors C_1, C_2, and C_4 begin to charge, and capacitor C_3 undergoes discharge.

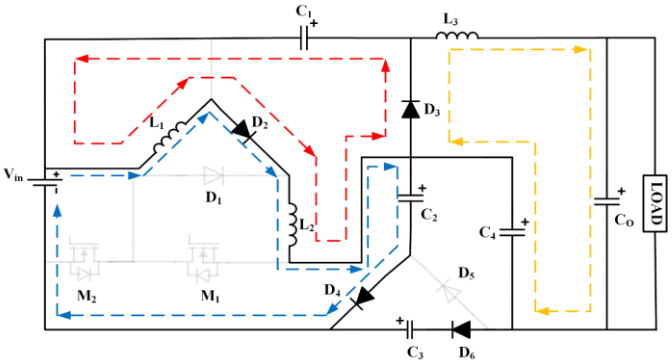

Fig. 3. Mode-2 Operation of proposed DC-DC converter

Additionally, the inductor L_3, which was previously charging in the first operating mode, now enters a discharge phase in this situation because endures a negative voltage base on the charging states of the capacitors C_1 and C_4. The equations of the elements for this state can be obtained as follows:

$$V_{in} = V_{L1} + V_{L2} + V_{C2} \rightarrow V_{L1} = V_{in} - V_{L2} - V_{C2} \quad (6)$$

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$$V_{C4} = V_{C2} + V_{C3} \quad (7)$$

$$V_{C1} = -V_{L1} - V_{L2} \quad (8)$$

$$V_{L3} = V_{C4} - V_o \quad (9)$$

$$V_{L2} = V_{C1} - V_{L1} \quad (10)$$

Figure depicts the current and voltage states for the components of the presented circuit based on the given equations and simulation results. The above illustration shows. That all inductors are charged and discharged at the same time. Capacitors C_1, C_2, C_4, and C_O charge and discharge at the same time intervals, whereas capacitor C_3 charges in the opposite direction as the other capacitors. Also, when diode D_1 is deactivated, diodes D_2, D_3, D_4, D_5, and D_6 are active, and vice versa.

2.3. Mathematical Modelling

The duty cycle for a power component is defined as follows:

$$\delta = \frac{T_{on}}{T} \quad (11)$$

In this equation, T_{on} is equal to DT, and has known is as the time interval that a power switch is activated. The switching time period is shown by T. According to the steady- state voltage equilibrium theorem; the value of the voltage for an inductor with a time period including the on (0 to DT) and off (DT to T) states time intervals is equal to zero.

$$\int_0^{\delta T} (V_{in})dt + \int_{\delta T}^{T} (V_{in} - V_{L2} - V_{C2})dt = 0 \quad (12)$$

By considering this fact that both L_1 and L_2 are charging at the dT time interval with the input voltage and discharging in (1-d) T time interval by the same values of L_1=L_2, one can obtain (VL_1=VL_2), so by *eq. (12)*, the voltage in capacitors C_2 and C_3 can be obtained as follows:

$$V_{in}\delta T = \frac{V_{in} - V_{C2}}{2}(1-\delta)T = 0 \rightarrow V_{C2} = V_{C3} = \frac{V_{in}(1+\delta)}{(1-\delta)} \quad (13)$$

Based on *equation (12)*, the voltage in capacitor C_4 equals:

$$V_{C4} = \frac{2V_{in}(1+\delta)}{(1-\delta)} \quad (14)$$

By considering the *figure 3*, one can write:

$$V_{L1} + V_{L2} + V_{C2} - V_{in} = 0 \quad (15)$$

Then, by replacing eq. (13), the voltage across the capacitor C_1 will obtain as bellow:

$$V_{C1} = \frac{2V_{in}\delta}{(1-\delta)} \quad (16)$$

Based on the laws described that also is known as the second voltage balance rule, one can write for inductor L_3 as

$$\int_0^{\delta T} (V_{in} + V_{C1} - V_0 + V_{C3})dt + \int_{\delta T}^{T} (V_{in} + V_{C1} - V_0 + V_{C3})dt = 0 \quad (17)$$

Therefore, by replacing the values of the parameters V_{C1} and V_{C3} in this equation, the DC voltage gain of the proposed converter for CCM operating mode can be presented as follows:

$$M_{CCM} = \frac{V_0}{V_{in}} = \frac{(2\delta+2)}{(1-\delta)} = 2\frac{(1+\delta)}{(1-\delta)} \quad (18)$$

3. SIMULATION RESULTS AND DISCUSSION

The parameters of the designed DC-DC converter as shown in *fig.1* is simulated in PSIM software at various duty ratios and the respective voltage and current across the capacitors and inductors waveforms are taken. The input and output voltage waveform are taken in consideration for the calculation of the voltage gain.

As shown in *fig. 4*, When the duty ratio of the power switches is at 0.8 in the designed simulated circuit, the waveforms depicts that all the Inductors in the proposed circuit gets discharged and charged at the same time. The capacitors C_1, C_2, C_4, C_O charge and discharge in opposite direction to capacitor C_3. The voltage profile of various capacitors is approximately maintaining flat profile by not exceeding the ripple content more than 2V, which the circuit offering inherent balancing of capacitor voltage profiles. Voltage across S_1 is less than the source voltage and voltage across the Switch S_2 is superior than the input voltage. With a Vin of 40V the V_{Out} is raised to 900V i.e., the voltage is raised by 22.5 times. The voltage gain achieved at duty cycle of 0.8 is 22.5. The output voltage for duty ratio of 0.6 is shown in *fig. 5*, which shows the V_{Out} is raised to 375V i.e., the voltage is raised by 9.4 times. Similarly, the output voltage for duty ratio of 0.4 is shown in *fig. 6*, which shows the VOut is raised to 200V i.e., the voltage is raised by 5 times. Table II represents if the duty ratio of the designed circuit increases the then the output voltage also increases rapidly *i.e.*, higher the duty ratio higher is the voltage gain of the circuit.

Table 1. Simulation Parameters

S. No	Component	Value
1	Output Capacitance C0	470µ
2	Capacitance C_1	100 µ
3	Capacitance C_2	100 µ
4	Capacitance C_3	47 µ
5	Capacitance C_4	47 µ
6	Inductance L_1	200 µ
7	Inductance L_2	200 µ
8	Inductance L_3	200 µ
9	Input Voltage V_{in}	40 µ
10	Output Resistance	161Ω
11	Switching Frequency	20kHz

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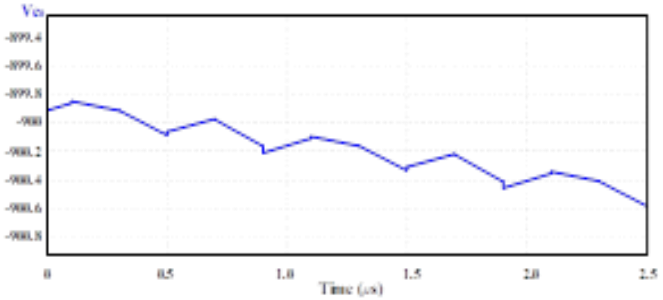
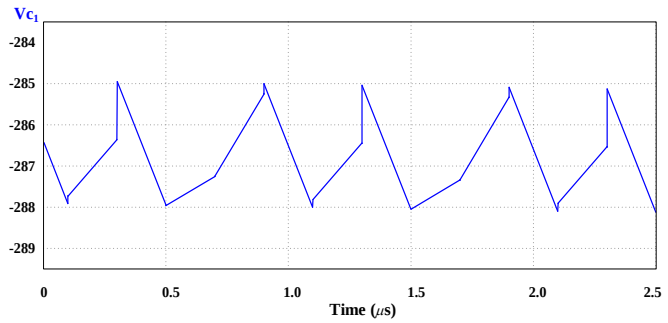
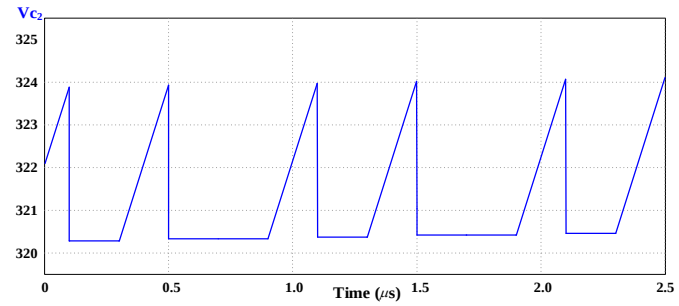


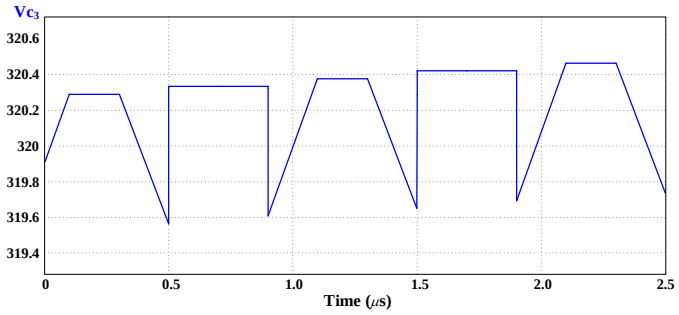
(a) Voltage across Capacitor



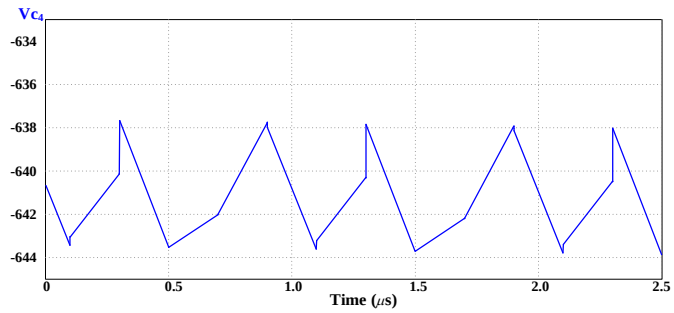
(b) Voltage across Capacitor C1



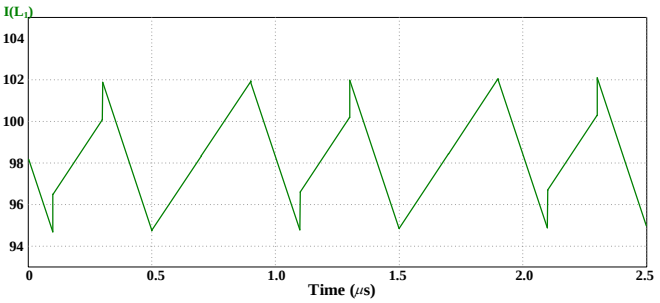
(c) Voltage across Capacitor C_2



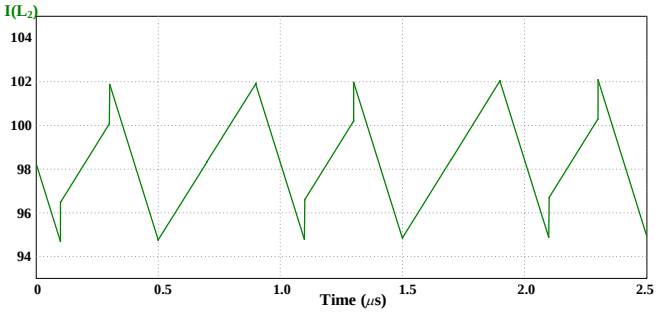
(d) Voltage across Capacitor C_3



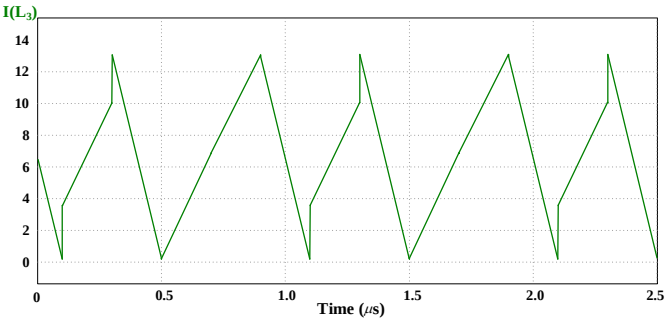
(e) Voltage across Capacitor C_4



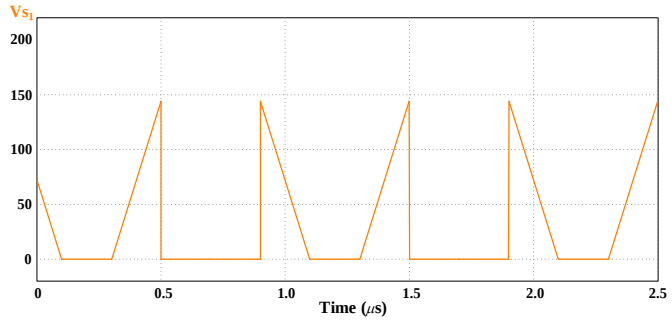
(f) Current through Inductance L_1



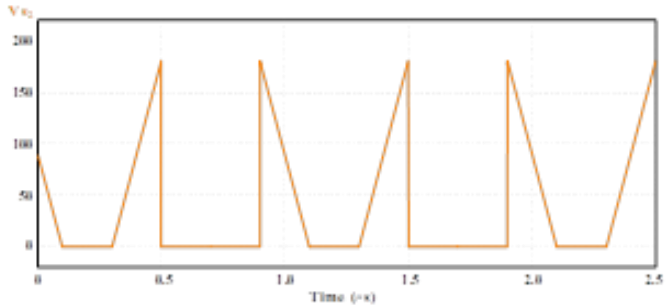
(g) Current through Inductor L_2



(h) Current through Inductor L3



(i) Voltage across Switch S1



(j) Voltage across Switch S2

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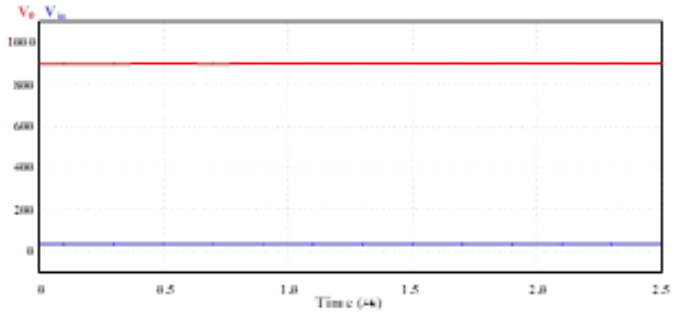

(k) Output and Input Voltage waveform

Fig. 4. Simulated results of proposed DC-DC converter at Duty Cycle of 0.8

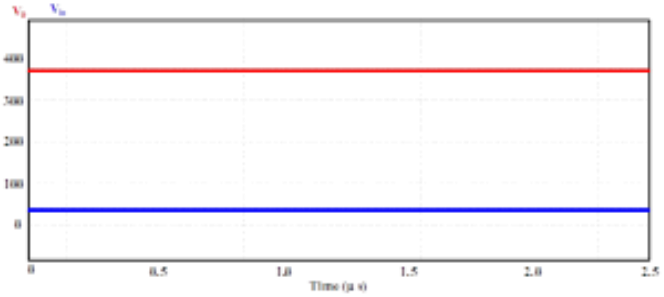

Fig. 5. Simulated results of proposed DC-DC converter input and output voltages at Duty Cycle of 0.6

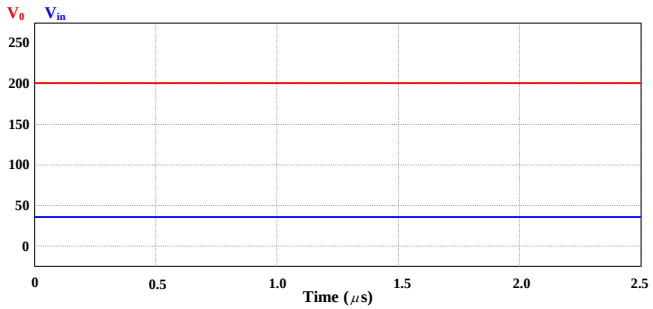

Fig. 6. Simulated results of proposed DC-DC converter input and output voltages at Duty Cycle of 0.4

To validate practicality of the proposed Switched Capacitor Inductor High Gain DC-DC Topology, an experimental result has been presented. *Fig. 7* shows the three-inductor current waveform along with switching pulse for a duty cycle of 0.6. *Figs. 8*, *9* and *10* shows the input and output voltage waveforms along with switching pulse waveform for a duty cycle of 0.4, 0.6 and 0.8 respectively. It is observed that all the hardware results are substantiate with the results obtained in the PSIM simulation. The consistency in the observed waveforms validates the converter's capability to deliver high-gain voltage across varying operational scenarios, thereby proving its adaptability. *Table 2* depicts the assessment of the presented converter with the other DC-DC converter topologies with respect to gain, voltage Stress, current stress, converter efficiency, no of semiconductors and passive components. All of these converters use switched-inductor or switched-capacitor cells, which puts them in the same category for easier comparison.

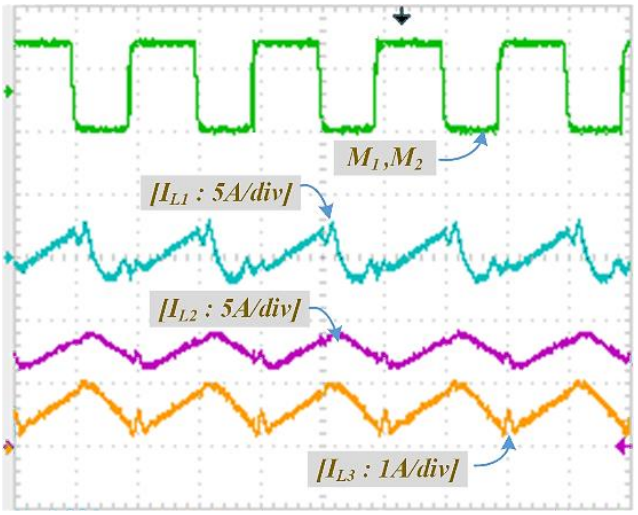

Fig. 7. Experimental results of proposed DC-DC converter various inductor currents at Duty Cycle of 0.4

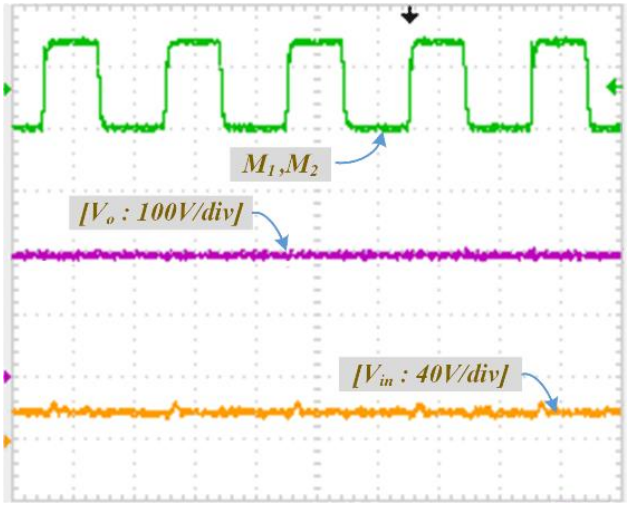

Fig. 8. Experimental results of proposed DC-DC converter input and output voltages at Duty Cycle of 0.4

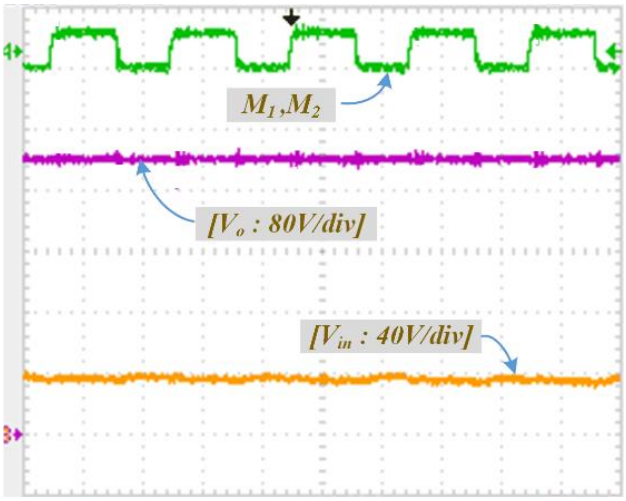

Fig. 9. Experimental results of proposed DC-DC converter input and output voltages at Duty Cycle of 0.6

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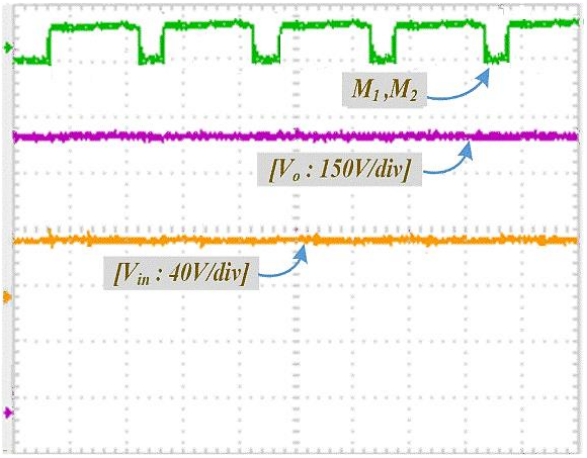

Fig. 10. Experimental results of proposed DC-DC converter input and output voltages at Duty Cycle of 0.8

Table 2. Variations of converter output voltage w. r to duty cycle

S. No	Duty cycle (δ)	Output Voltage for V_{in}=40V
1	0.1	92
2	0.2	118
3	0.3	153
4	0.4	200
5	0.5	270
6	0.6	375
7	0.7	550
8	0.8	900
9	0.9	2030

Table 3. Comparison of various DC-DC converters

DC-DC Topology	Gain (*Vout/Vin*)	Current Stress	Voltage Stress	Efficiency	No. of Semiconductors		No. of Passive Component	
					D	S	C	I
[11]	$\frac{3\delta+1}{1-\delta}$	$\frac{(2+n)\delta I_o}{1-\delta}$	$\frac{V_{out}}{\delta(n+1)+1}$	94.5	3	2	5	4
[12]	$\frac{2n-1}{(1-\delta)(n-1)}$	$\frac{(1+n)\delta I_o}{1-\delta}$	$\frac{(n-1)V_{out}}{2n-1}$	96.2	3	1	4	5
[13]	$\frac{\delta(1+3\delta)}{1-\delta}$	$\frac{2\delta(3+\delta)I_o}{(1-\delta)}$	$\frac{(1+\delta)V_{out}}{\delta(1+3\delta)}$	95.8	5	1	3	3
[14]	$\frac{1+\delta}{1-\delta}$	$\frac{(1+n\delta)I_o}{1-\delta}$	$\frac{\delta V_{out}}{1+\delta}$	95.7	3	2	2	2
[15]	$\frac{3+\delta}{1-\delta}$	$\sqrt{\frac{3+\delta}{1-\delta}}I_o$	$\frac{\delta V_{out}}{2}$	96.8	7	1	4	2
[16]	$\frac{n\delta+1}{1-\delta}$	$\frac{1+n}{1-\delta}I_o$	$\frac{V_{out}}{(n+1)\delta}$	96.4	2	1	3	4
Proposed Converter	$\frac{2(1+\delta)}{1-\delta}$	$\frac{(2+2\delta)I_o}{\sqrt{\delta(1-\delta)}}$	$\frac{V_{out}(1-\delta)}{2(1+\delta)}$	97.1	6	2	5	3

4. CONCLUSIONS

The presented high-voltage boost DC-DC converter stands out for its innovative design, which incorporates lower power components, thereby enhancing efficiency while minimizing current and voltage stress across the main switch. The output voltage varies in a boost converter depending on the duty ratio and input voltage. From the simulation results, with a duty cycle of 0.4 and a Vin of 40V, the output voltage is 200V. Increasing the duty ratio to 0.5 with the same input voltage yields an Vout of 265V. Similarly, a duty ratio of 0.8 with a Vin of 20V results in an Vout of 900V. These findings underscore the relationship between duty cycle, input voltage, and output voltage in boost converter circuits. As the duty cycle increases with input and output voltages tends to increase. For the designed circuit for the duty ratio of 0.8 the voltage gain is 22.5. The suggested converter streamlines complexity by incorporating only two power switches that operate simultaneously, simplifying the control mechanism of the drive circuit. With its versatility, the suggested converter finds applications in portable lighting systems and solar PV-based applications.

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