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Precise Models for Power Loss Analysis in a 15-level Asymmetric Reduced Switch Inverter

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ABSTRACT- In the examination of power converters, power losses are the most important metrics, and since they are approximated well enough, they have a considerable influence on both economic and technical evaluations. In comparison to high-switching frequency modulation, the purpose of this article is to demonstrate that switching and conduction losses, which are both types of power losses, are much lower in low-frequency switching modulation. Phase Disposition (PD), a pulse width modulation (PWM) method that is based on high-frequency multi-carriers, and Selective Harmonic Elimination Pulse Width Modulation (SHEPWM), which operates at a fundamental switching frequency, are the two switching modulation techniques that will be utilized in this investigation. The objective of this study is to evaluate the power losses that occur in an asymmetric multi-level energy converter that has fifteen levels of reduced switches. To determine the switching losses that occur in multi-level inverters, a MATLAB Simulink model has been constructed. The PLECS software was used to construct the thermal model of the recommended inverter, which would further facilitate in-depth research. A comparison of the switching losses and conduction losses of the proposed inverter system is carried out by this study via the use of the PLECS thermal model and MATLAB simulation.

Keywords: Power Loss, Conduction Loss, Reduced switch inverter, Switching Loss, Precise models.

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1. INTRODUCTION

Multilevel inverters, also known as MLIs, play a crucial role in contemporary power electronics. They provide solutions for high-power and medium-voltage applications by improving power quality and lowering losses [1]. One of the most notable innovations in this field is the 15-level asymmetric reduced-switch inverter, which strikes an effective compromise between complexity, cost, and performance. These inverters, in contrast to standard topologies, make use of a smaller number of switches to attain greater voltage levels, hence reducing the amount of both power losses and component prices [2]. In applications using renewable energy, where efficiency and compactness are of the utmost importance, this design is very advantageous. The efficiency of MLIs is significantly impacted by several important parameters, including switching and conduction losses. The transitions between the on and off states in power devices are the source of switching losses, while conduction losses are caused by the resistance of semiconductor materials when they are in operation [3]. Several sophisticated modulation methods, such as Phase Disposition Pulse Width Modulation (PD) and Selective Harmonic Elimination Pulse Width Modulation (SHEPWM), have been extensively used to reduce the impact of these losses. By operating at low switching frequencies and focusing on the removal of certain harmonics, SHEPWM can enhance efficiency while simultaneously reducing electromagnetic interference. On the other hand, pulse width modulation (PD PWM) makes use of numerous high-frequency carriers, which helps to ensure that switching losses are distributed uniformly across all devices and improves the thermal stability of the system [4].

Simulation tools such as MATLAB SIMULINK and PLECS are essential for assessing and optimizing power losses in multilevel inverters (MLIs). MATLAB facilitates accurate simulation of switching dynamics and harmonic behavior, while PLECS emphasizes thermal analysis, aiding in the modeling of heat dissipation and device junction temperatures under actual working circumstances. These techniques have been widely used to construct and evaluate models for 15-level asymmetric inverters, providing a thorough comprehension of their performance under diverse operating situations [5].

One of the primary benefits of reduced-switch topologies is their capacity to provide nearly sinusoidal output voltage with little harmonic distortion while using fewer components. This not only lowers the dimensions and mass of the system but also decreases total production expenses. The asymmetric design allows enhanced control over the output waveform,

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rendering it appropriate for applications where power quality is paramount, such as industrial drives and renewable energy integration [6]. Nonetheless, there are obstacles to attaining maximum performance with these systems. The asymmetric architecture necessitates precise control algorithms to regulate voltage levels and minimize harmonic distortion properly. Moreover, thermal management is a significant issue, since reduced-switch layouts may result in localized heat accumulation in some components, affecting dependability [7]. Future research aims to create sophisticated thermal management systems, including enhanced heat sink designs and dynamic control techniques, to resolve these challenges. Furthermore, the incorporation of machine learning and artificial intelligence for the real-time monitoring and regulation of switching and thermal performance is a burgeoning field of study [8-9].

In renewable energy systems, especially photovoltaic (PV) applications, 15-level asymmetric inverters are increasingly used for their efficiency in managing high input voltages while preserving compact designs. With the increasing demand for sustainable energy, these inverters are set to assume a pivotal role in both grid-tied and freestanding systems. Their capacity to enhance power quality, reduce losses, and function effectively under fluctuating load situations makes them essential for attaining sustainable energy objectives [10]. Numerous research has proposed using Sinusoidal Pulse Width Modulation (SPWM) to mitigate harmonic distortion and evaluate overall power loss in multilayer inverters [11]. Although SPWM is good at reducing harmonics, it uses very high switching frequencies and wastes a lot of power because of it. To minimize power losses and total harmonic distortion (THD), it is essential to optimize the switching frequency. To further reduce power losses, additional methods have been explored, such as modifying the switching angles to generate gating pulses for different inverter switches. The goal of these solutions is to drastically reduce power losses, which may reach as high as four percent of the power that reaches the load, especially when switching frequencies are reduced. [12-13].

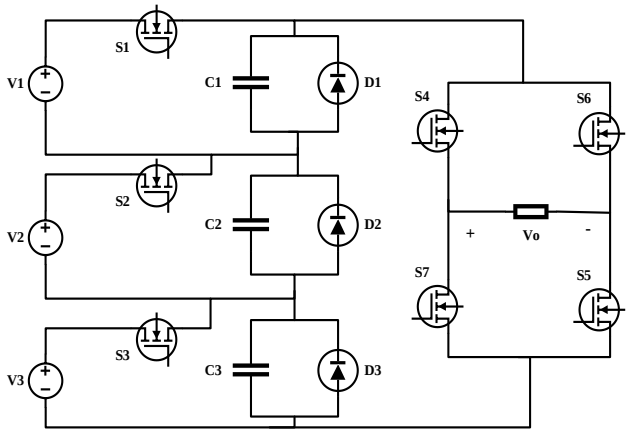

Figure 1. Proposed Fifteen-Level Asymmetric Inverter

The thermal analysis of MOSFETs in the proposed inverter integrates PDPWM and SHEPWM techniques using PLECS software to calculate switching and conduction losses [14]. Subsequently, SIMULINK is used to streamline each switch in the suggested inverter. The suggested simplified models use SHEPWM and a curve-fitting method derived from the MOSFET data sheet to evaluate switching and conduction losses [15]. This study compares PLECS thermal analysis with SIMULINK simplified model power losses.

2. PRECISE POWER LOSS MODELS

When designing power converters, power semiconductor devices experience four main types of losses:

- **Switching Losses**: These occur when the device is turning on or off. During these transitions, energy is dissipated as heat, especially due to the voltage and current overlap.
- **Conduction Losses**: These occur when the device is fully on and conducting current. The device typically has a non-zero resistance, which leads to power losses as current flows through it.
- **Gate Driver Losses**: These are due to the control circuit that drives the gate of the semiconductor. While these losses can be significant in some designs, they are usually small compared to switching and conduction losses.
- **OFF-State Losses**: These losses happen when the device is in the OFF state, where it ideally should not conduct any current. However, small leakage currents or other factors can cause some losses.

In most cases, the losses introduced by the gate driver and the OFF-state are negligible enough to be disregarded. Because of their disproportionate contribution to total power dissipation, switching and conduction losses are often the main targets of loss estimation in inverter and converter designs.

2.1. Power losses in MOSFET

While ideal switches have almost no power losses at all, real switches have both static (conducting) and dynamic (switching) losses that have been measured during the switching cycle (Figure 4). When operating with non-zero voltages and currents, the semiconductor switch consumes power throughout its on-and-off operations, which take many microseconds. Power loss due to conduction occurs when the switch is in its on state, which causes a voltage drop on MOSFETs.

The inverter's efficiency is affected by the power loss in the MOSFET, which restricts its usage and becomes an essential challenge that designers of power inverters cannot ignore. Heat is produced by power losses inside the semiconductor switch, which leads to an increase in junction temperature and the device's overall temperature profile. The effect of self-heating is particularly noticeable in devices that are packed closely together.

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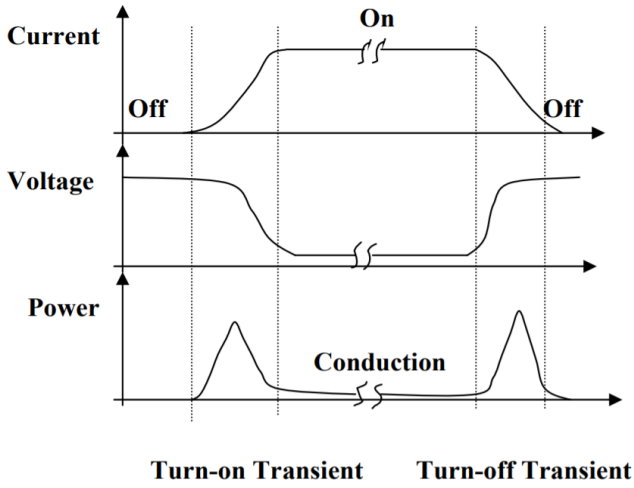

Figure 2. Representation of an MOSFET switching cycle spanning a cycle

Keep the T_j junction temperature below the manufacturer-specified healthy operating range to avoid catastrophic failure of the system. An improved setup is possible if the device's internal temperature gradient can be accurately anticipated under real-world working circumstances. To get the best possible stability, performance, and package design in power converters, thermal analysis is an essential design challenge.

2.2. Details about MOSFETs' datasheets and their thermal properties

The proposed 15-level inverter uses Infineon MOSFETs; Table 1 details the model and specs of these devices.

Table 1. Details of MOSFET specifications from the datasheet

MOSFET Model	MFA60N40H5
Make	**Infineon**
Drain Source Voltage VDSO Max	**500V**
Drain Current at 25^0 C	**20A**
Ic Max	**12A**
P_d	**35W**
T_j	**25^0 to 175^0 C**
I_{ON}	**110A at 175^0 C**

Furthermore, specific temperatures for the conduction energy losses, turn-on losses, and turn-off losses of the MOSFET device need to be given at 25°C and 175°C, respectively. *figure 3* shows that the on-state voltage (Von) and the base-level conduction ion current are directly proportional to these losses.

2.3. Switching and Conduction Losses in Thermal Simulation

Due to rising demands for smaller packages and greater power densities, the thermal performance of electronic power systems is of the utmost importance. To provide an effective cooling solution tailored to each specific application, PLECS requires the thermal system to be integrated with the electrical architecture early in the design process. Additionally, estimates of switching and conduction losses are calculated within a few seconds. The simulation of losses does not impact the overall speed of the process, as optimal switching is maintained throughout the simulation. Throughout the operation, the device's current and temperature are the key factors influencing the amount of power loss. When compared to thorough device modeling, our synthesis of optimum switching models with exact loss data offers an alternative that is both cost-effective and accurate. To get access to the relevant datasets, the integrated visual editor inside PLECS is used.

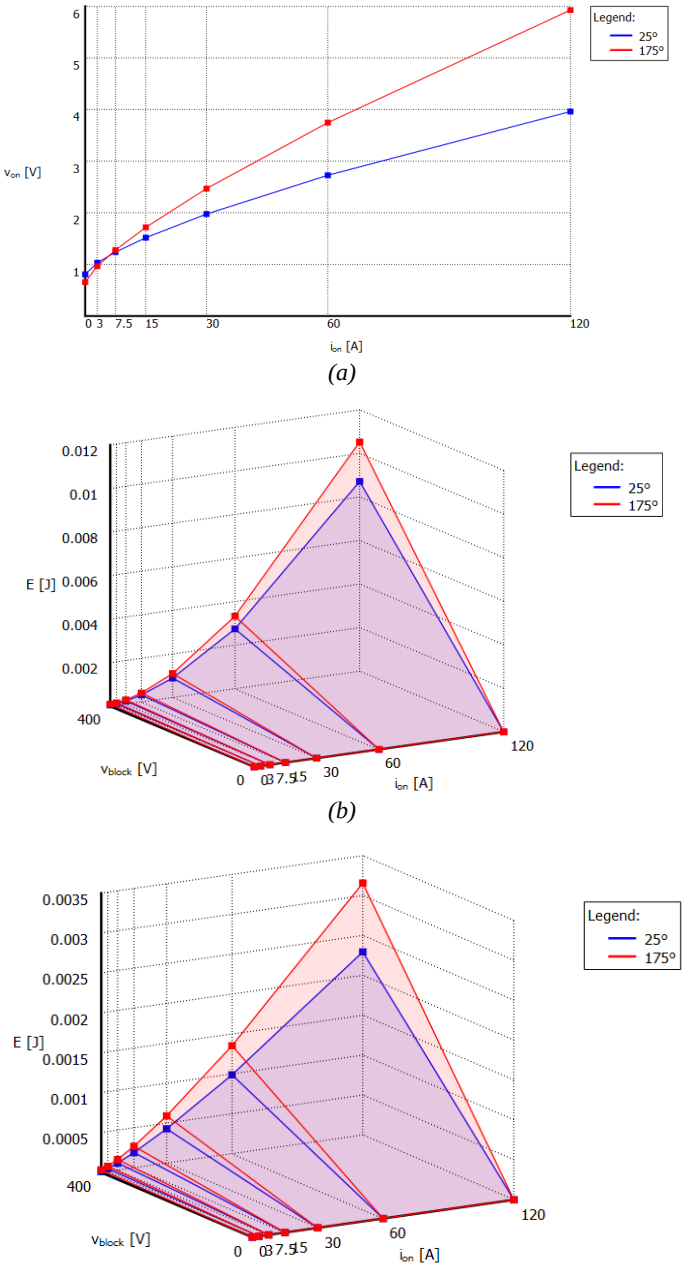

Figure 3. MOSFET Thermal Characteristics

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2.4. MOSFET thermal modeling using PLECS as the modeling tool

Plexim has created a software tool called PLECS, which is designed to do system-level simulations of electric circuits. Although it was built specifically for power electronics, it may be used for any kind of power system. Controls and a variety of physical domains, including thermal, magnetic, and mechanical systems, are among the things that may be modelled using PLECS [16]. These go beyond the electrical system. The only DC feature of the MOSFET employed in PLECS is the high-level output of a control signal that is linearly interpolated from user input. [17]. Simulating the effects of variables such as junction temperature (T_j), drain current (I_D), gate resistance (R_G), and overvoltage on the total switching energy (Ets) is critical due to the MOSFET's dynamic characteristics. This is especially significant because this MOSFET is also dynamic. In PLECS, these connections may be used, and much like the DC characteristics, they are often interpolated linearly. In addition to this, the system is dependent on the value that the user enters to switch energy that is lost.

2.5. Concept of heat sink

The power losses of all devices that are inside the heatsink's border are absorbed by the heatsink. At the same time as it describes an isothermal atmosphere, a heat sink is responsible for distributing the temperature of the atmosphere to the components that are near it. There will be no difference in temperature between the semiconductors that are installed on the heat sink. Direct-type pulses on PLECS are used to mimic the witching energy losses.

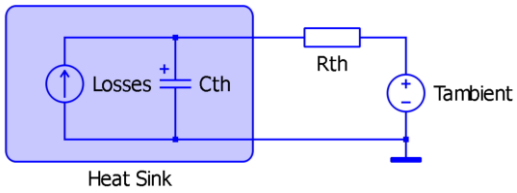

Figure 4. Heat sink-based electrical equivalent of thermal circuit

These pulses are characterized by having zero duration and infinite amplitude. To avoid the unrealistic scenario of infinite thermal resistance associated with these switching energy pulses, it is essential to either define the thermal capacitance of the heat sink or incorporate a thermal network with capacitance. Both of these approaches are necessary to ensure a more accurate and feasible thermal model. To accurately represent heat dissipation, the electrical version of a thermal circuit with a heat sink is shown in *figure 4*. Additionally, it shows how the thermal dynamics are modelled using circuits.

2.6. The computation of the overall cycle-average losses

However, another element that is of significance is the overall power dissipation that each semiconductor produces. One way to determine the average losses a device goes through is to add up the losses that happen during the next switching time to the average power pulse. The representation of the average cycle technique of loss computation may be seen in Figure 8. To do integrated loop summation on energy loss processes, the C-Script PLECS Block is used [17].

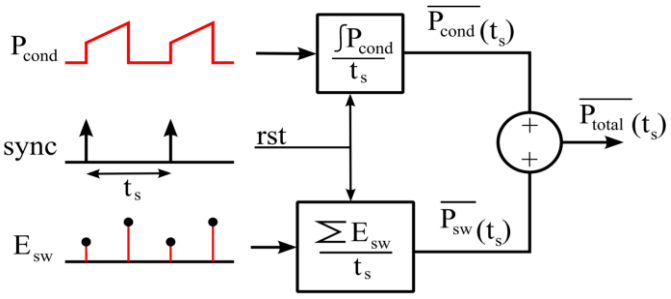

Figure 5. Computational model for average losses

3. POWER LOSS CURVE FITTING MODELS

Multilevel inverters, in comparison to two-level inverters, provide a more difficult challenge when it comes to the computation of inverter losses. Traditional methods for calculating losses in two-level inverters do not work well enough when used in multilayer inverters. Because each semiconductor switch in multilevel inverters has a different current in comparison to the other switches, the loss behavior of each switch is different. This is the primary explanation for this phenomenon. The estimation of losses, on the other hand, becomes more challenging when the switching frequency of each device is not the same at higher levels.

The purpose of this study is to offer a simpler model for the calculation of power losses on 15-level MLI. A few minor adjustments have been made to the methodology described in [9] to create the model that is being proposed. 150^0 is considered to be the highest temperature that may be reached while operating. MATLAB-SIMULINK, a modeling tool, is being used to do an online evaluation of the prototype. When conducting the investigation, the researchers took into consideration the total load of R = 25Ω and L = 15mH. Unlike the previous state where the load was changeable, this one causes a complete shift from a resistive to an inductive load. We plan to conduct an in-depth analysis of the behavior of inverter losses under different load circumstances.

3.1. Calculation of Conduction Losses

Power semiconductor devices can have conduction losses while the device is in the on-state and conducting current. It is predicted that the conduction losses in the inverter that is being suggested would rise in a manner that is proportional to the number of levels that are present. By multiplying the saturation voltage by the conduction current while the device is in the on-state, it is possible to determine the conduction losses for any device that is in the on-state [10]. The equation that follows is an expression of this connection.

$$P_{Conduction} = |I_C| V_{on}$$

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For this reason, the absolute value is taken into consideration. It is of the utmost importance that the present value maintains constant positive values. Two crucial components are commonly included in the majority of theoretical models of on-state voltage. A V_o voltage, often called the threshold voltage, and a R_{on} resistor, which shows the current dependence in series with the ideal device, are the parts that make up this system. Several parts are necessary to reproduce the device's operation in its state to a precise degree.

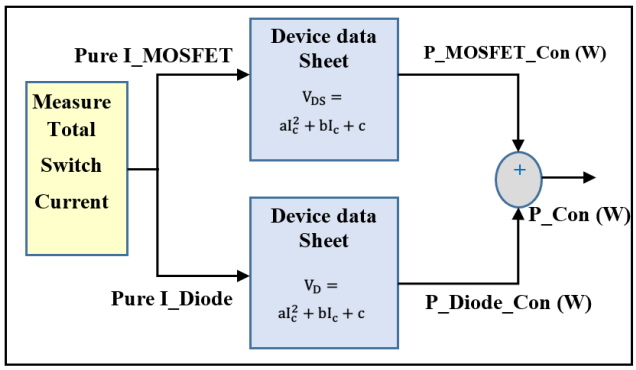

Figure 6. Determination of the conduction loss with the use of the curve-fitting SIMULINK model

The approach in *figure 6* simplifies and efficiently calculates conduction losses. This technique uses a second-order conduction current formulation to represent the device's threshold voltage. Based on datasheet curves, curve fitting generates a quadratic equation. The control system uses switch and diode quadratic equations. The MATLAB SIMULINK model must measure pure switch and diode current independently. Pure switch current is the positive component of the on-state device current, whereas pure diode current is the negative component. Measure the device's total current. The diode and MOSFET switch conduction losses may be simply manufactured by adding the relevant blocks.

3.2.Calculation of Switching Losses

Most power semiconductors lose power when turned off. Parallel switches and diodes lose switching power. Due to switching frequency, SPWM switching losses increase inverter loss. Power switches introduce e_{on} and e_{off} losses. Antiparallel diodes are so fast to respond to forward bias that they only ever suffer from E_{rec} loss or turn-off loss.

Diode turn-on losses are usually less than 1% of turn-off times. Junction temperature, gate resistance, wire inductance, blocking voltage, and switching current affect switching loss. High-cost multi-level inverters with switching losses perform badly in HVDC. We estimate losses online using the device's datasheet switching energy curves. After current segmentation, curve fitting generates energy factor (K) second-order polynomial equations. Energy loss is the result of plugging the switching current into the energy factor curve calculation.

Figure 7 shows the block diagram for switching losses.

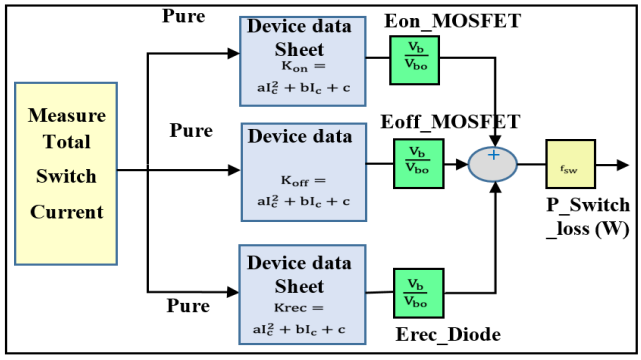

Figure 7. Process curve fitting for the switching loss computation using the SIMULINK graphical modeling tool

It is usually possible to calculate the switching losses at any point in time when the device is in operation, including during the on and off states.

Energy loss during MOSFET on time is

$$E_{on\_SW\_loss} = V_{CE} * I_C * \frac{T_{on}}{2}$$

Energy loss during MOSFET off time is

$$E_{off\_SW\_loss} = V_{CE} * I_C * \frac{T_{off}}{2}$$

The total energy loss during the switching operation

$$E_{SW\_loss} = E_{on\_SW\_loss} + E_{off\_SW\_loss}$$

The power loss in the operation switch $= (E_{SW\_loss})/T$

Total switching losses $= (E_{SW\_loss}) * f_{SW}$

Where,

f_{SW} is Switching frequency

E_{SW_loss} is the Total energy loss during switching operation.

3.3. Computation of Total Losses

The model shown in the figure is used to analyse the overall power losses that result from the combination of *figures 6* and *7 and 8*.

MOSFET datasheet curve fitting equations

$$v_{DS} = -2 * 10^{-7} I_D^2 + 0.0018 I_D + 0.9661$$

$$v_D = -1 * 10^{-7} I_D^2 + 0.0012 I_D + 0.7796$$

$$K_{MOSFET-on} = 8 * 10^{-7} I_D^2 - 0.0023 I_D + 4.016$$

$$K_{MOSFET-off} = 3 * 10^{-7} I_D^2 - 0.0011 I_D + 3.1584$$

$$K_{Diode-rec} = 7 * 10^{-7} I_D^2 - 0.0039 I_D + 6.6546$$

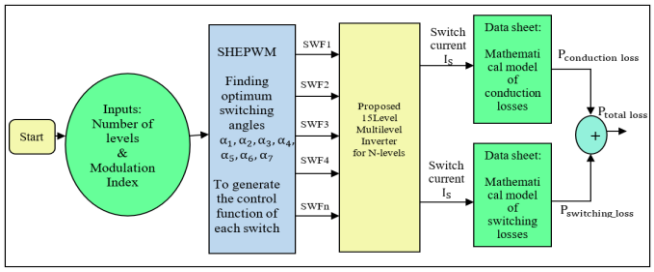

Figure 8. Simulations of the SHEPWM switching curve using the SIMULINK model for calculating total power loss

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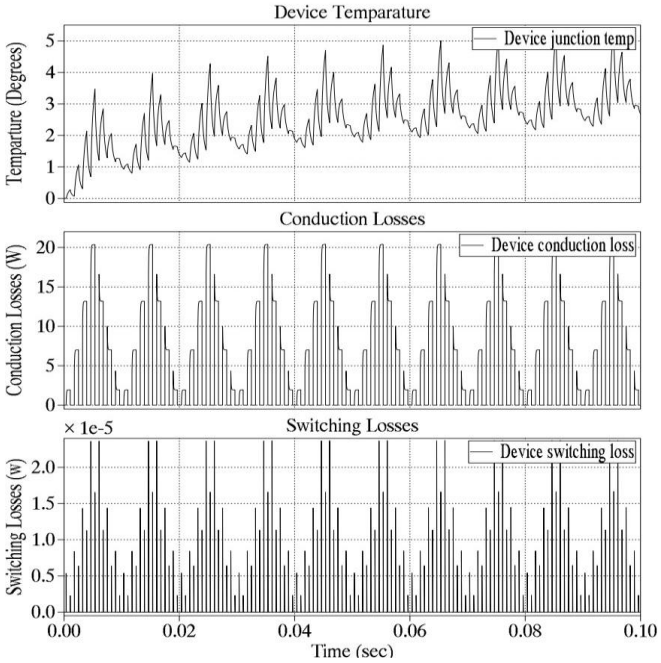
4. RESULTS & DISCUSSIONS

4.1. Using PLECS Thermal Models for Power Loss Calculations

For both low and high switching frequencies, PLECS simulation was used to study conduction losses as well as switching losses. For each switch, *figure 9* displays the switching losses, conduction losses, and PDPWM switching losses as a function of device temperature. Increased switching losses and numerous on-and-off cycles are caused by the high-frequency IGBT switches 'S1', 'S2', and 'S3' in the proposed inverter. Switches 'S4', 'S5', 'S6', and 'S7' operate at lower frequencies, which results in reduced power losses.



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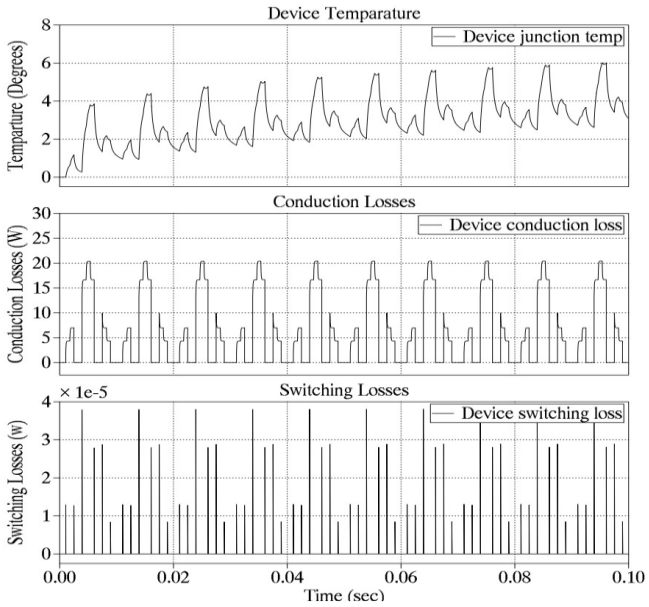

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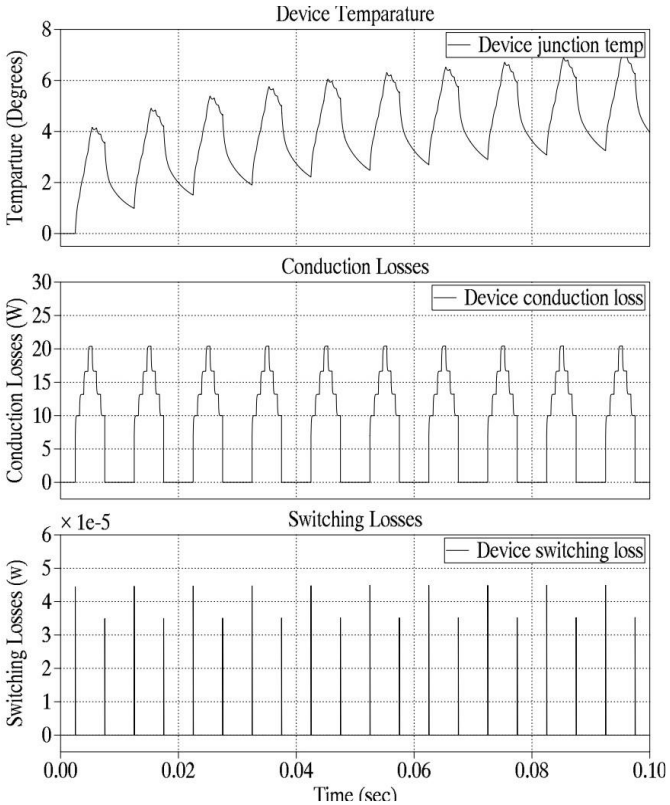

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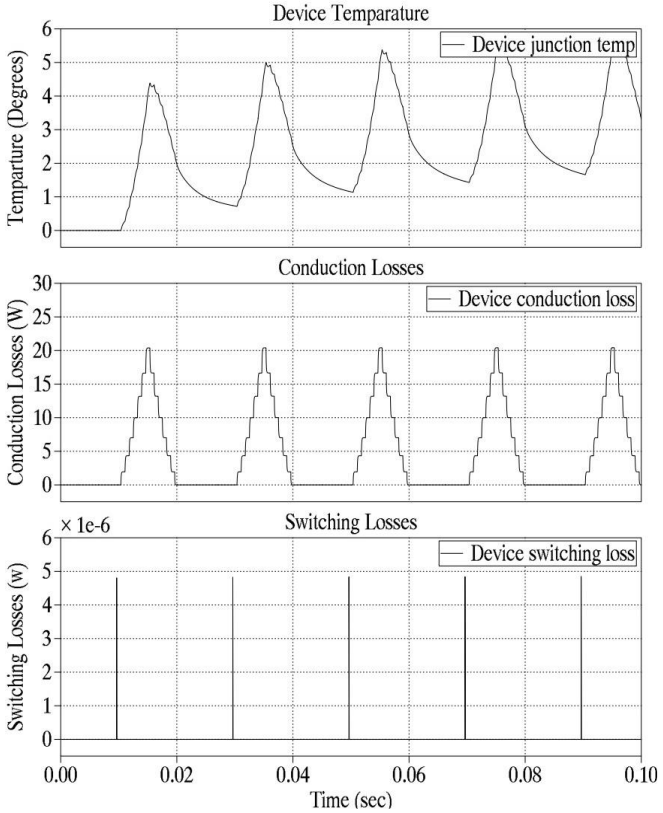

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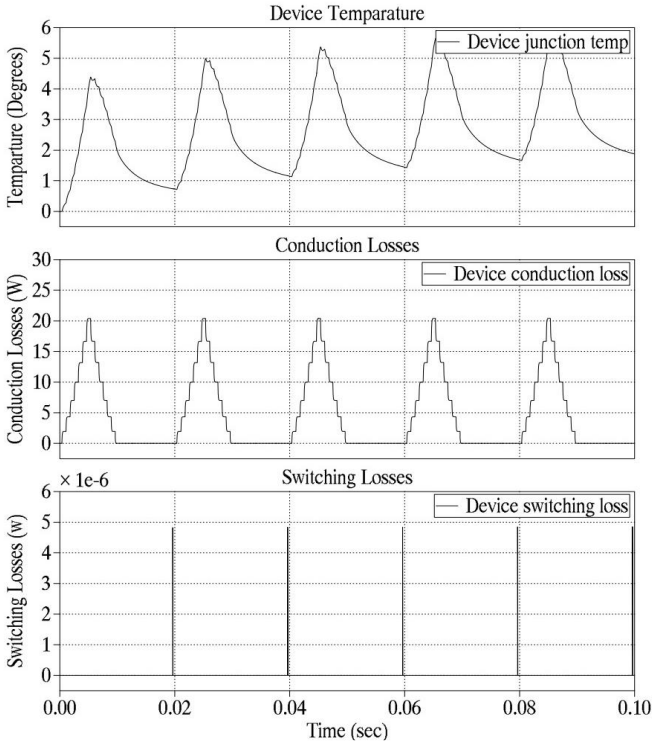
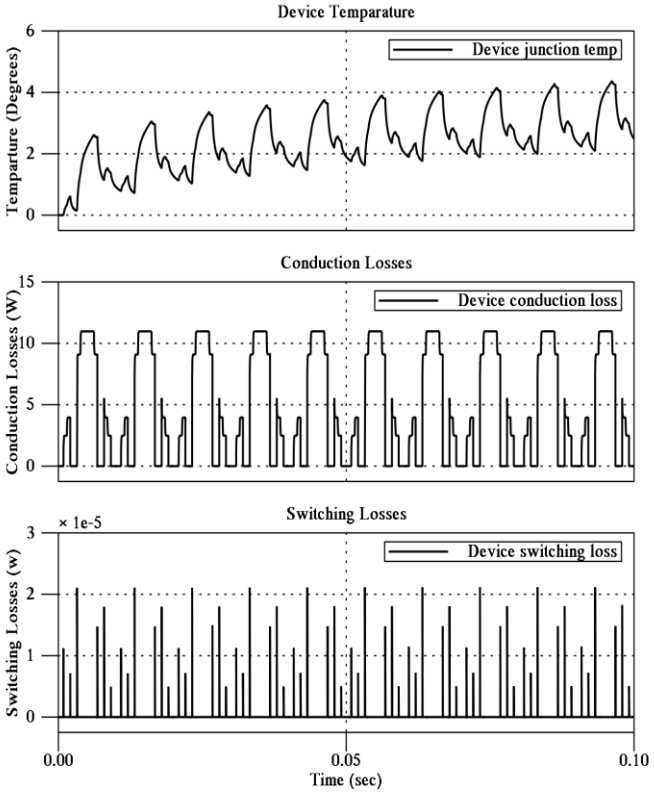


(e)

Figure 9. Power losses in the inverter switches S1 to S5 with PDPWM



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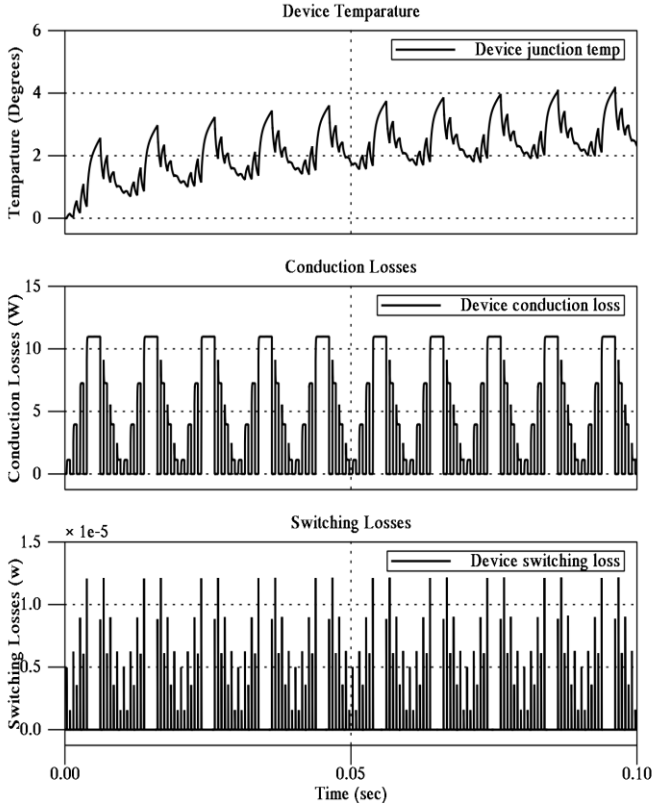

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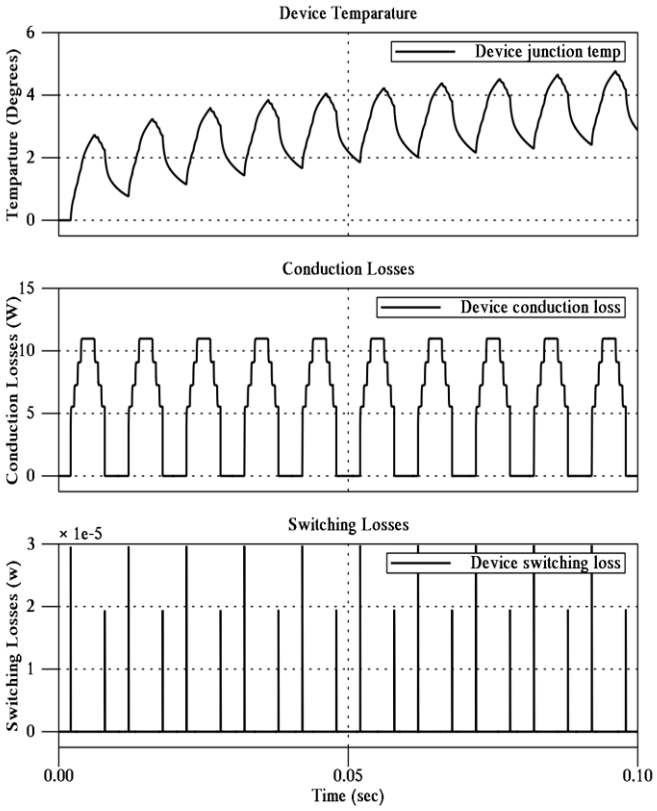

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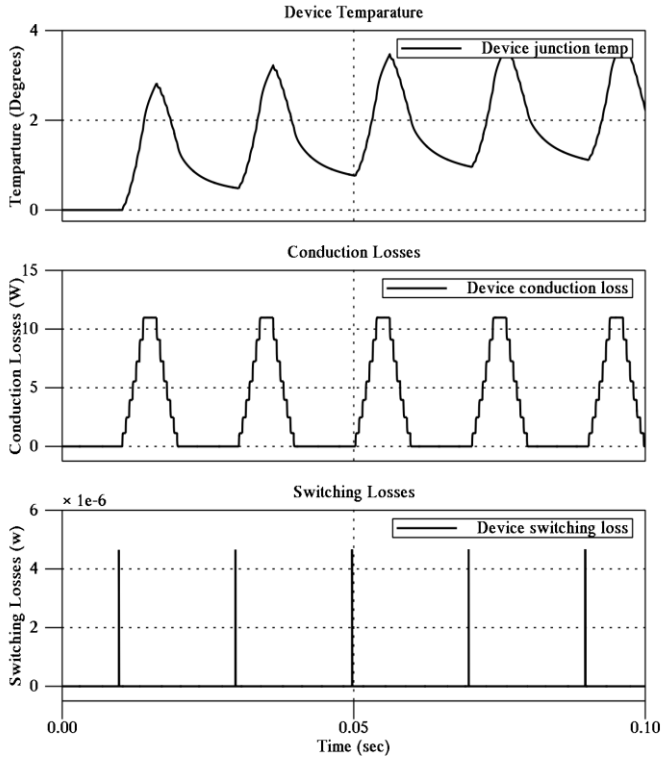

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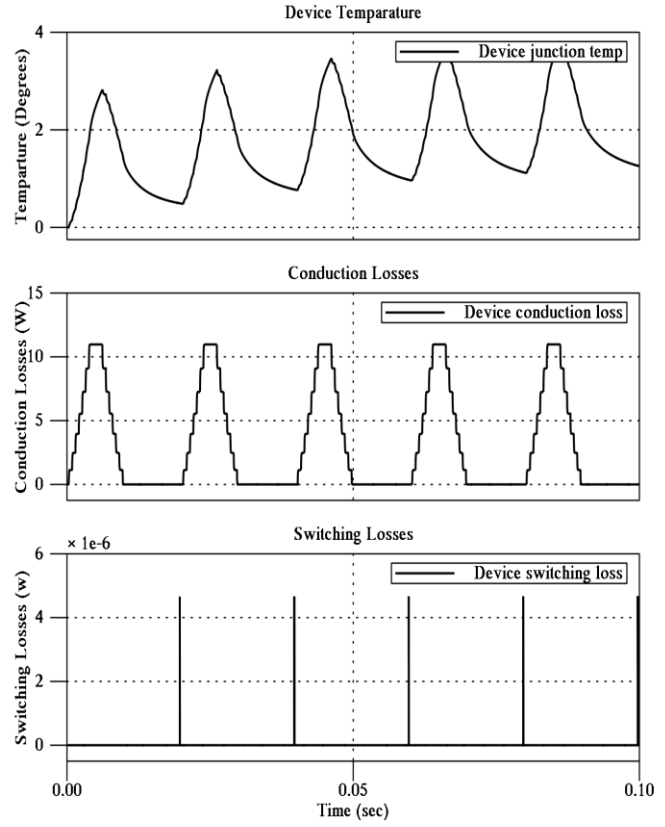

(e)

Figure 10. Power losses in the inverter switches S1 to S5 with SHEPWM

Table 2. Power losses with PDPWM and SHEPWM

Switches	PDPWM			SHEPWM		
	P_{L}-Cond (W)	P_{L}_Switch (W)	P_{L}_Total (W)	P_{L}-Cond (W)	P_{L}_Switch (W)	P_{L}_Total (W)
S1	3.980	0.015	3.995	3.952	0.0085	3.9605
S2	4.962	0.013	4.975	4.753	0.0075	4.7605
S3	6.850	0.009	6.859	5.650	0.005	5.655
S4	3.905	0.003	3.908	2.985	0.0003	2.9853
S5	3.902	0.003	3.905	2.984	0.0003	2.9843
S6	3.903	0.003	3.906	2.985	0.0003	2.9853
S7	3.904	0.003	3.907	2.984	0.0003	2.9843

All of the SHEPWM switches' temperatures, conduction losses, and switching losses are shown in Figure 10. Comparing *figures 9* and *10*, PDPWM switching has larger switching and conduction losses than SHEPWM switching. PLECS simulation indicated power losses from PDPWM and SHEPWM for each 15-level inverter MOSFET switch in *table 2.*

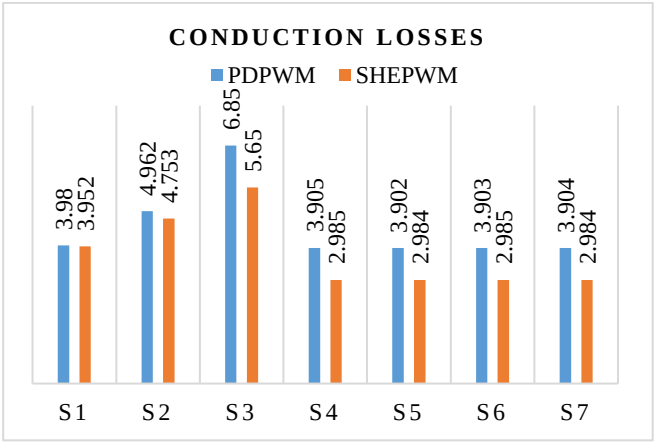

Figure 11. Conduction Losses Comparison with PDPWM and SHEPWM Switching using PLECS

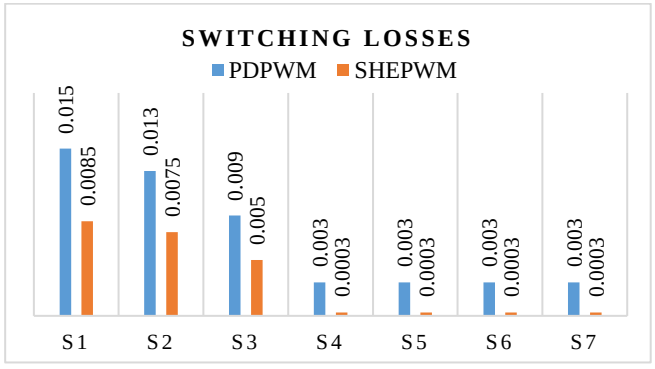

Figure 12. Switching Losses Comparison with PDPWM and SHEPWM Switching using PLECS

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A comparison of the conduction losses that are caused by high-switching frequency control techniques and low-switching frequency control methods is shown in *figure 11*. The findings show that SHEPWM switching results in lower conduction losses than PDPWM switching. Additionally, *figure 12* shows a comparison of switching losses, indicating that the SHEPWM technique yields lower switching losses in comparison to the PDPWM method.

4.2.Using SIMULINK Models for Power Loss Computation

The curve fitting techniques from the device data sheet are used to create the exact models that are displayed in *figures (6), (7),* and *(8)*. These models are implemented in the MATLAB SIMULINK platform respectively. The genetic Algorithm is used to implement the SHEPWM (low-frequency switching) control mechanism, and the GA toolbox is used to implement it. *Table 3* shows the power losses that happen across all of the switches in the 15-level inverter.

Table 3. Accurately predicting power losses with precise models

Switches	P_L-Cond (W)	P_L_Switch (W)	P_L_Total (W)
S1	3.9024	0.00857	3.91097
S2	4.2312	0.00743	4.23863
S3	5.0341	0.0051	5.0392
S4	2.8622	0.0002	2.8624
S5	2.8622	0.0002	2.8624
S6	2.8622	0.0002	2.8624
S7	2.8622	0.0002	2.8624

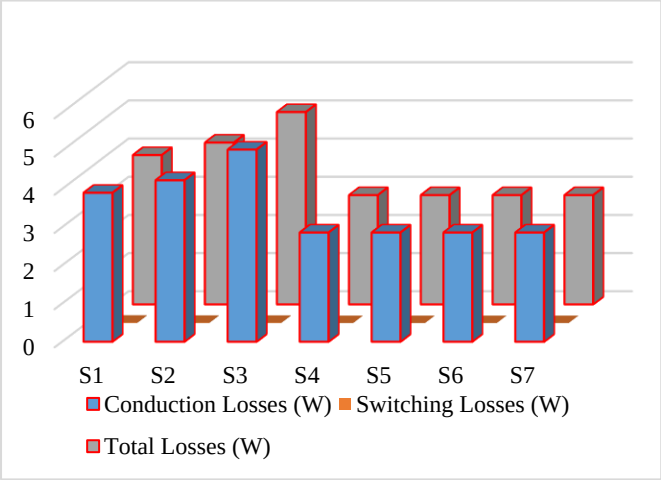

Figure 13. Comparison of Power losses with SHEPWM using precise models

Table 4 summarizes the total harmonic distortion (THD) and power losses that occurred as a consequence of running the SIMULINK model simulation for different modulation indices (*figure 8*). *Figure 15* shows the fluctuation of total harmonic distortion (THD) with modulation index, whereas *figure 14* shows the output voltage waveform. Power losses amount to 26.04W and total harmonic distortion (THD) hits a low of 5.75% at a modulation index of 0.9. Power losses may be seen in *figure 16* varying with the modulation index. *Figure 16* displays the power losses of the modulation index.

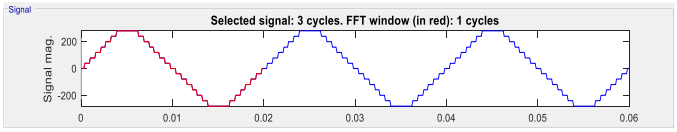

Figure 14. Output voltage waveform of 15-level inverter

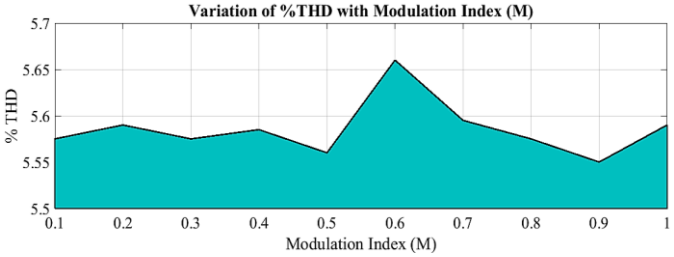

Figure 15. Variation of THD with Modulation index

Table 4. Variation in power loss and total harmonic distortion (THD) with modulation index using SHEPWM control

Modulation Index	P_L-Cond (W)	P_L_Switch (W)	P_L_Total (W)	THD %
0.4	19.562	0.022	19.584	6.65
0.5	19.923	0.022	19.945	6.36
0.6	20.882	0.021	20.903	6.09
0.7	22.061	0.021	22.082	5.76
0.8	22.757	0.02	22.777	5.63
0.9	23.516	0.02	23.536	5.52
1.0	24.484	0.019	24.503	5.55
1.1	24.625	0.018	24.643	5.38
1.2	24.959	0.019	24.978	5.5

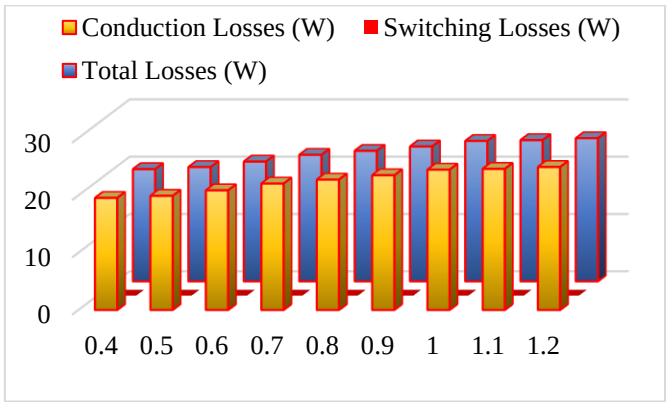

Figure 16. Total power loss variation with modulation index

5. CONCLUSIONS

Power converter circuit performance is affected by semiconductor transient losses. A 15-level PV-compatible

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asymmetric inverter with fewer switches is designed and built. This asymmetric inverter's harmonic distortion and power losses should be assessed. Evaluation of multi-level inverter losses is crucial. Many multi-level inverters waste conduction and switching power. A study on power losses using accurate models Utilizing PLECS thermal modeling and SIMULINK's simple and precise curve fitting methods, this study examines the power loss of a 15-level asymmetric inverter. We assess switching and conduction losses independently at a junction temperature of 150^0 C and a thermal impedance of 1.25 Ω. Switching and conduction losses are evaluated separately at 150^0 C junction temperature and 1.25Ω thermal impedance. For PDPWM and SHEPWM, PLECS presented the 15-level inverter foster thermal model. PDPWM inverter efficiency at 0.9 modulation index is 97.53% and SHEPWM 98.25%. The system datasheet states that SIMULINK creates precise curve-fitting models with exact voltage and energy curves. At low switching control and 98.56% efficiency, inverter losses were 1.006% of power. PLECS modeling yields 98.78% efficiency while SIMULINK curve fitting models 98.82% at low switching frequency control for the recommended inverter.

ABBREVIATIONS

SHEPWM:	Selective Harmonic Pulse Width Modulation
PDPWM:	Phase Disposition Pulse Width Modulation
THD:	Total Harmonic Distortion
P_L-Cond:	Conduction Losses
P_L_Switch:	Switching Losses
P_L_Total:	Total Power Losses
GA:	Genetic Algorithm
E_{on}_sw_Loss:	Energy Loss in Switches during ON time
E_{off}_sw_Loss:	Energy Loss in Switches during OFF time
E_sw_Loss:	Total Energy Loss in Switches
Ic Max:	Maximum Collector Current
P_d:	Maximum Power Dissipation
T_j:	Junction Temperature
I_{ON}:	ON-time current of the switch

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