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Implementation of Pass Transistor Logic and C²MOS Linear Feedback Shift Register (LFSR) Circuit using FPGA and PSpice

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ABSTRACT- In this paper, a 4-bit Linear Feedback Shift Register (LFSR) is implemented based on a well-designed architecture combining using Pass-Transistor (PT) and Clock Complementary Metal Oxide Semiconductor (C²MOS) logic techniques. The D-flip flop registers and the XOR gates are the main parts of the propose LFSR. Number of transistors along with the speed of LFSR were positively enhanced since the exploited logic design techniques tends to blend the flavor of NMOS and PMOS devices. The PSpice and Field Programmable Gate Array (FPGA) based on Hardware Description Language (HDL) are the two different LFSR implementation environments. It has been observed that LFSR performance was effectively improved in terms of size and speed. Therefore, paper's main aim refers to decreasing in number of transistors as well as speeding up LFSR circuit. A minimum clock time of 5ns was recorded under clearly correct LFSR output patterns. The LFSR circuit Based CMOS techniques can reduce the exploited transistors up to 43% of the conventional C²MOS logic. Besides, the number of transistors being reduced reflects the achieved circuit's size reduction. It was concluded that paying attention to the design of the main LFSR circuit parts contributes mainly in the enhancement of the whole circuit performance.

Keywords: LFSR, Pass-transistor, C²MOS, Transmission Gate, FPGA.

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1. INTRODUCTION

A Linear Feedback Shift Register (LFSR) is a shift register device in which the exclusive-or (XOR) of its previous states (taps) leads to form the LFSR input state. In other word, it is known as a chain of flip-flops connected so that the input of each present flip-flop state is the output of the previous one. The feedback polynomial controls the feedback itself. They are defined as the connecting points at which the outputs of one or more than one XOR is fed back to LFSR registers' input [1]. Random numbers are often used in various systems such as decryption and encryption keys, digital communications and other modellings and simulating of complex data sets [1-4]. In digital communication systems, generating random sequences is of importance in order to achieve data and noise simulation. For instance, the Linear Congruential Generator (LCG) is used to produce pseudorandom sequence with a Gaussian distribution for additive noise simulations [5]. However, arbitrary number creator is a special device that generates number of sequences and which may be hardware or software-based system [6-8]. LFSR is one of the shift-register devices used to generate pseudo-random numbers, pseudo-noise sequences, fast digital counters, and whitening sequences [9]. Hence, paying attention to LFSR design is regarded as an important circuit design.

Many techniques have been applied to design the LFSR circuit in order to enhance the circuit performance as well as to reduce the power consumption along with minimizing the area. Some of those techniques focus on the power consumption and some of them focus on area-size. Complementary Metal Oxide Semiconductor (CMOS) Field Effect Transistor (FET) is known as a low power dissipation architecture, so that, it is opted to implement the LFSR circuit as in [10,11]. In [10], a modified low power LFSR is prepared for Test Pattern Generation (TPG) technique in order to achieve low power consumption. However, the design of the LFSR does not focus on the internal parts of the whole circuit such as the XOR or even the D-flip flop registers. In [11], the author aims to implement the LFSR in 3-different architectures to achieve its low power implementation in CMOS VLSI but it solely focuses on the design of the D flip-flop. A Gate Diffusion Input (GDI) technique is used to architect the LFSR circuit in [12,13] to reduce the area size and to obtain low power dissipation. The Conditional Discharge Flip Flop (CDFF) and GDI techniques were exploited to design the flip-flops and XORs respectively in order to build a low-power consuming LFSR circuit as in [12]. In [13], the pulsed latches were applied as a substitute to D- flip flops applied in the circuit of the LFSR. The aim behind

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using pulsed latches was to minimize the consumed power of the whole LFSR circuit. However, the author in [13] did not take into account the XOR design. In addition, and based on the GDI, the author in [14] implemented LFSR in order to obtain low power dissipation along with decreased area size but the design did not take into account mixing between CMOS families. The architecture of 2 Phase Clocked Adiabatic Static CMOS Logic (2-PASCL) along with the Reversible Logic Gates (RLG) architecture was proposed in [15] but LFSR design was not performed by enhancing the work of its main parts (XOR and D-flip flop). Another approach was presented in [16] where optimization of the LFSR circuit was achieved using Built in Self-Test (BIST) architecture. However, paying attention to the gist of the XOR or D flip flop design was not taken in consideration in [16]. In [17], the low power LFSR was used to design and implement of the low power Test Pattern Generator (TPG). The LFSR used in [17] comes from utilizing Three ring oscillators and fuzzy logic concept. The drawback of [17] is that it does not take into account the inner design for XOR and D flip flops. In [18], multibit LFSR circuit based Pseudorandom number generators is presented and implemented using FPGA. Using the multibit comes to add more security over the conventional LFSR designing. In [19], LFSR design is presented through applying the Positive Feedback Source Coupled Logic (PFSCL) style through applying 4 different connections by combining two PFSCL styles in order to pick the best one with respect to delay and power consumption. Again, [20] exploits the FPGA to design 4 bits LFSR design. The XNOR is replacing the standard LFSR feedback which eventually enhanced the power dissipation saving. Using altera Quartus 16, [21] presented an LFSR implementation based on using of the transition controller design which proved better power consuming enhancement over standard LFSR circuit.

The focus of this paper is on building LFSR in two different environments through applying well-combined logic design architectures represented by C2MOS and Pass Transistor Logic (PTL) techniques. FPGA and PSpice are the simulation environment of the proposed LFSR design. Generally, the paper aim is to reduce the number of transistors in the whole LFSR circuit design in order to level up the speed along with keeping the area quality acceptable in terms of decreasing its size.

2. LINEAR FEEDBACK SHIFT REGISTER (LFSR)

In general, LFSR is a state machine which is used to generate random number sequences. It is built by a series of nth flip-flop shift register devices whom their n is set based on the data size and from which the specified taps are XOR-ed and fed to the LFSR input as feedback [9]. The seed is the name given to the very beginning input code set to feed the LFSR. A nonzero value seeded LFSR is periodic due to the property of having specific number of states for any register type [1]. However, a well-determined feedback function is prone to produce long and good random sequences. Since there are n flip-flops (X0 to Xn-1), then this LFSR s known as an n stage LFSR. It can cover a 2n-1 different states which is also called a maximal length LFSR. *Figure 1* illustrates the standard form of the assembled LFSR throughout this paper.

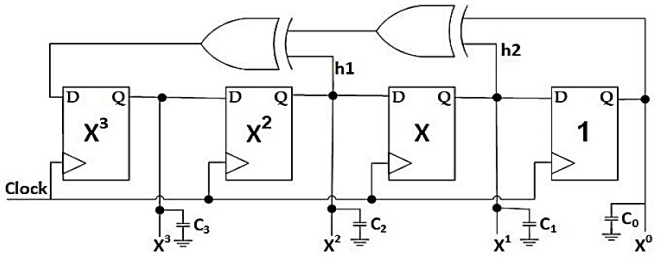

Figure 1. Standard linear feedback shift register

Mathematically, the behavior of the LFSR can be described by *equation 1* shown below:

$$f(x) = 1 + h_1 x + h_2 x^2 + \dots\dots\dots + h_{n-1} x^{n-1} + x^n \quad (1)$$

Where f(x) is the LFSR polynomial algebra and h_i indicates whether the feedback is present or absent from a specific particular flip-flop position into flip-flop position x^(n-1). The presence of feedback path is indicated by setting h_i into 1, and its absence is indicated by setting h_i into 0 which means there is no feedback in that particular position.

2.1. Pass-transistor and C²MOS logic

Of the powerful architecture techniques, pass-transistor logic is regarded as a popular and wide spread substitution to CMOS specially when the target is the reduction of used transistor in a particular design. The property of the pass-transistor logic is represented by its allowing for the primary inputs to drive the gate, the source and the drain terminals of MOSFET [22]. Since PTL suffers from static power dissipation, it was found that using Transmission Gates (TG) can provide an effective way to solve this problem. Therefore, the TG was opted to design the XOR gate applied in the LFSR circuit design. The TG is of the most widely exploited design techniques to solve the power degradation. It depends on combining the best flavor of the NMOS and PMOS devices through connecting them in parallel. For the register part of the LFSR circuit, the C²MOS positive edge-triggered register D-flip flop is exploited. The C²MOS architecture was chosen because it is insensitive to clock overlap device that depends on master-slave design concept [23].

2.2. Theory of Operation

From the given LFSR design in *figure 1*, h1, h2, and h3 are set to be equal to 1. Therefore, the polynomial algebra can be written as in *equation 2* depending on *equation 1* as follows:

$$f(x) = 1 + x + x^2 + x^3 \quad (2)$$

The feedback taps arrangement in an LFSR is expressed so that the polynomial coefficients must be 1s or 0s (a polynomial mod 2). *Equation 2* indicates the feedback polynomials where taps are chosen at the 4th, 3rd, and 2nd bits. According to *figure 1*, it is clearly shown that the taps are XORed and fed back to the first bit. Initializing the LFSR with a seed value is necessary

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since it will continue to shift 0s unless a starting seed is chosen to wake it up. In this paper, the seed value was chosen to be 0001 while simulating LFSR output results.

3. LFSR Implementation Design Circuit

3.1LFSR implementation Design Based on PSpice

In VLSI PSpice model, TG is used to implement the XOR function between LFSR taps. It is then called TG XOR. It has the property of being fast and simple [24]. *Figure 2* illustrates the TG XOR schematic design. The design of TG XOR is shown in *Figure 2*.

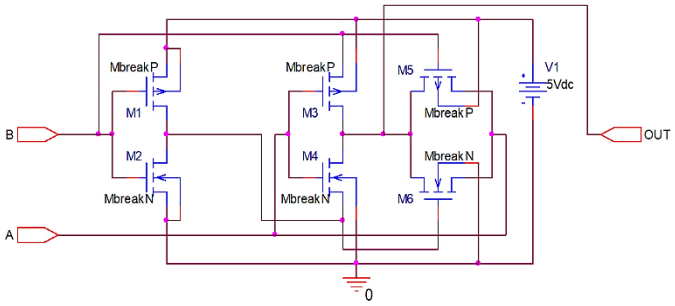

Figure 2. PSpice Transmission Gate XOR design

Figure 3 and *figure 4* show the schematic hierarchical block and its simulation results respectively.

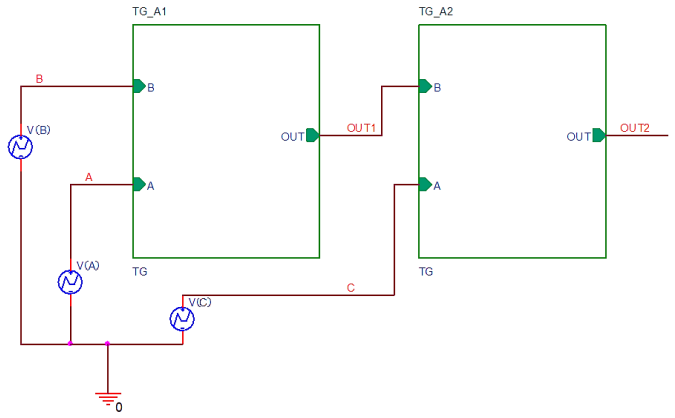

Figure 3. PSPICE Hierarchical Block of TG XORs

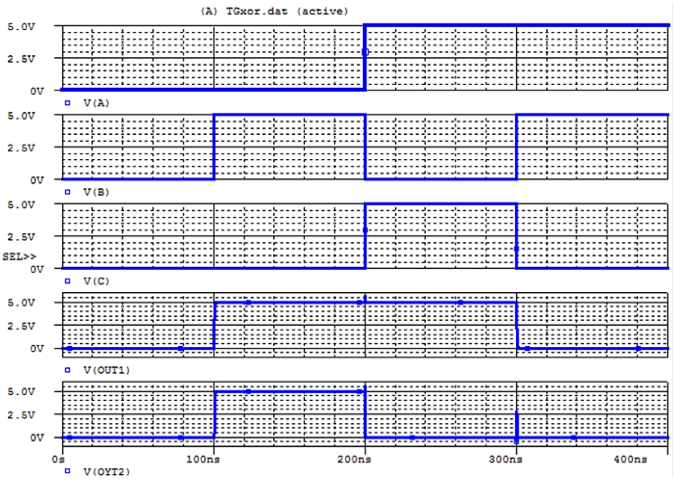

Figure 4. PSPICE Simulation of Hierarchical Block TG XORs

C²MOS logic architecture was opted to perform D flip-flop design of the LFSR circuit [24]. PSpice software was used to simulate the behavior of the suggested C²MOS D flip-flop (positive edge-triggered register). The single D flip-flop architecture is illustrated in *figure 5* as shown below.

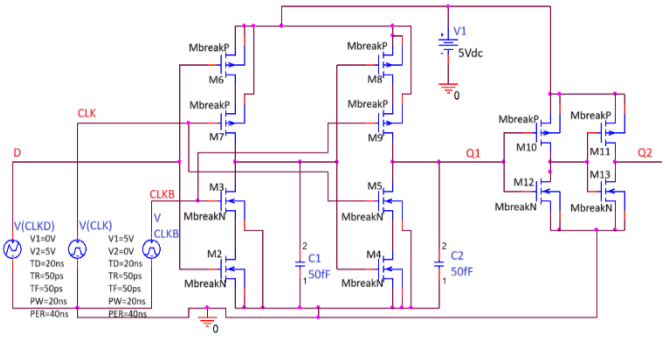

Figure 5. PSPICE C²MOS (Positive ET flip flop) Schematic design

By defining the D flip-flop as a block in hierarchy level, the whole circuit of the LFSR was built in hierarchy level after including the TG XOR block design. *Figure 6* shows the PSpice schematic of LFSR. In this circuit, we defined a primary clock signal with a period of T=40ns and rise/fall time of (tr=tf= 50psec.) and a duty cycle of 50%. In order to set the initial pattern of the flip-flops in the PSpice so as to be X0X1X2X3=0001, we need to set the initial condition for capacitances C_4, C_3, and C_2 as 0 V dc, and the initial condition for capacitance C_1 as 5 Vdc. It worth to mention that VDD value of 5V were opted since using high VDD level ensures a quick charging up to gate-source capacitor which significantly increases the switching speed of the device. Moreover, noise immunity is enhanced in the case of high VDD levels since the grounded side and the 5V VDD provide a symmetric amount of noise level form both directions which take part in minimizing any effect that could be occur from unexpected signal spikes. Besides, circuit stability is maintained. Consequently, a successful setting for the LFSR seed was achieved as (0001) from which the LFSR will starts generating the random sequences.

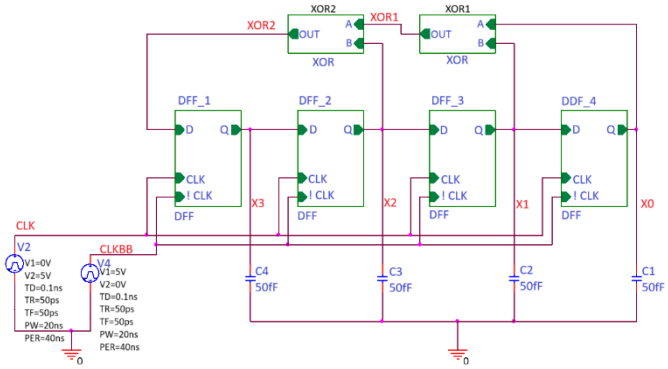

Figure 6. PSpice Schematic design of the LFSR

4. RESULTS AND DISCUSSION

In this paper, both of PSpice and FPGA design circuit of LFSR were tested through applying an initial seed condition starting from a primary clock signal of 40ns period. The aim is to

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observe the minimum clock period at which the arranged LFSR circuit will keep valid output results.

4.1 Synthesis and Simulation

To simulate the LFSR circuit, minimum clock period (higher speed) factor is figured out. Starting from 40 ns period clock, it was noticed that the obtained waveforms of the LFSR output are correct when compared to previously predicted waveform patterns. A16-clocking period has been used to simulate the proposed LFSR circuit. The Predicted number is chosen to be :(1, 8, 4, 10, 13, 6, 3, 1, 8, 4, 10, 13, 6, 3, 1, 8). Predicted and simulated patterns with perfect matching was noticed during LFSR circuit testing. Simulation of LFSR was also performed to calculate the minimum clock period (T_(CLK-min)) at which valid waveforms are obtained. In this part, we started reducing the clock period and test LFSR performance at each new clock signal while observing the results. It was found that T_(CLK-min) is equal to 5ns since correct LFSR patterns are still shown. The reason is that the wrong Patterns start to emerge when the clock width is no longer overcoming the LFSR register's speed. Therefore, the clock value of 1.5 ns could be regarded as an example for the value of the clock at which the LFSR patterns reveal wrong records. PSpice simulations for the different clock periods taken and *figure 7*, *figure 8*, and *figure 9* show the results at 15ns (as test clock start up until reaching to minimum clock), 5ns and 1.5ns respectively.

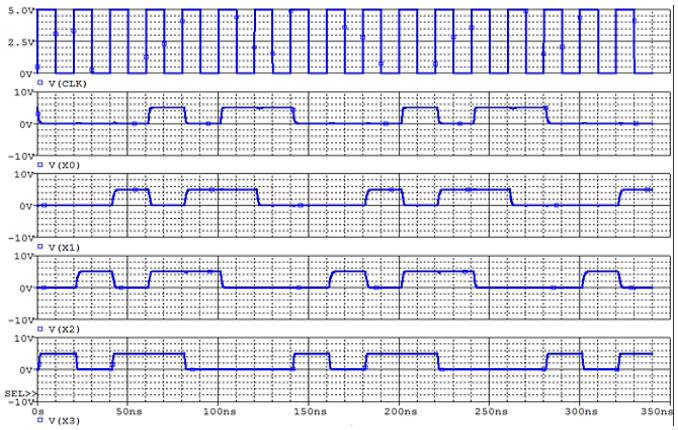

Figure 7. PSPICE Simulation of LFSR circuit at (T_CLK= 5ns)

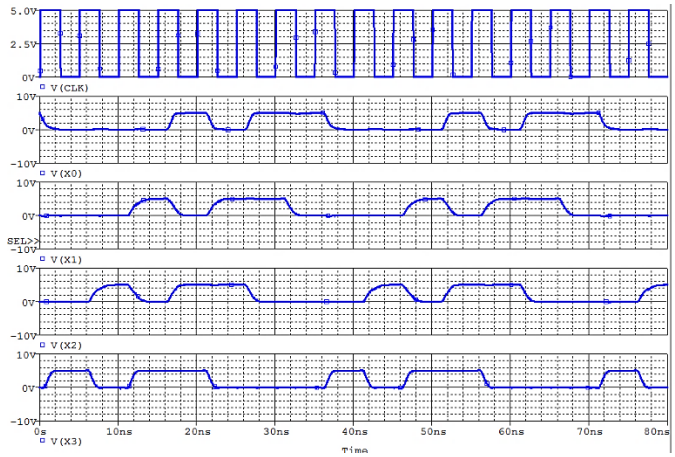

Figure 8. PSPICE Simulation of LFSR circuit at (T_CLK= 5ns)

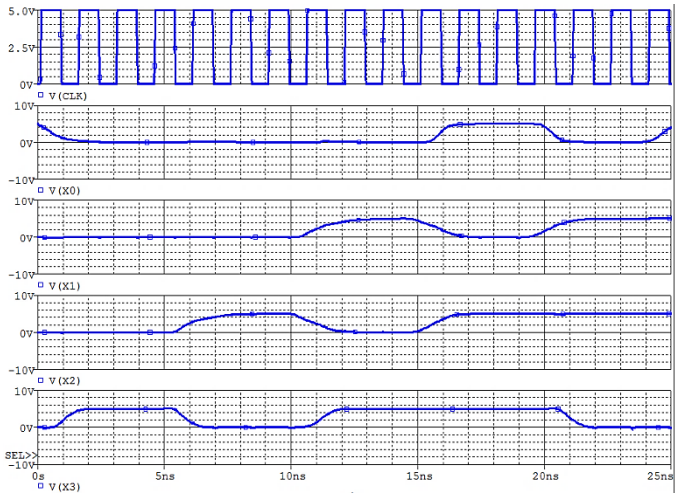

Figure 9. PSPICE Simulation of LFSR circuit at (T_CLK= 1.5ns)

4.2. FPGA Gate Level Simulation

To implement the LFSR circuit based on FPGA kit platform, the proposed design circuit has been codded by Verilog HDL code using Quartus-II software in order to be verified and simulated. The register transfer level (RTL) viewer of the programmed LSFR circuit illustrated in *figure 10* declares the DFF blocks of the designed circuit. To verify the achieved mathematical results of the design circuit with gate level simulation result, a Verilog test bench code is utilized to the LFSR project codded file. Quartus-II software applied on Cyclone-IV FPGA kit platform is used to gate level simulate the designed LFSR design. As shown in *figure 11*, the proposed design operates with the processing speed of 928.51 MHz. In the other word, it only requires 2,947ŋSec delay times to get the output results. The gate level simulation results of Figure 11 declare that the programmable LFSR circuit is using a clocked period of 25ŋSec. On the other hand, the *Q* output line shows that the presented values (1, 9, 13,7, 10, 12, 15, 14, 6, 2, 8, 5, 3, 0) are repeatedly generated for every 16 timing periods. Moreover, the LFSR design consumes power dissipation as follows: Core Static, I/O and the total Thermal Power Dissipation are 46.11 mW, 9.44 mW and 55.55 mW respectively.

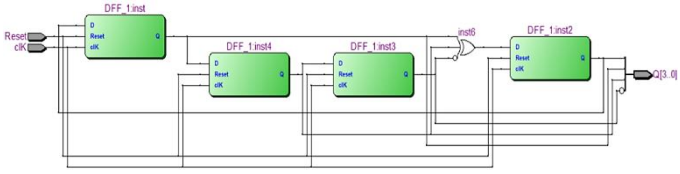

Figure 10. RTL Viewer of LFSR Circuit

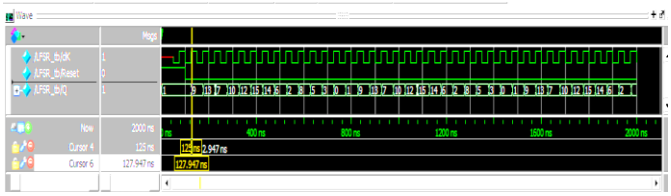

Figure 11. The gate level simulation results of LFSR Circuit

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A comparison between the proposed LFSR circuit and other previous works is done in *table 1* in the terms of the FPGA types, number of bit samples, operating speeds and delay times.

Table 1. A Comparison Between the Proposed LFSR Circuit and the Previous Works

LFSR	No. of Bits	FPGA Type	Freq. Operation (MHz)	Delay (ηsec)
[15]	4	Kintex-7	62.94	5.3
[16]	4	Spartan-6	678.77	3.597
[17]	4	Virtex5	379.23	2.637
Proposed	4	Cyclone IV	724.64	3.28

The comparison table shows the improvement of proposed LFSR circuit in the term of delay time and frequency operating speed over the other works taking into account the variety of the FPGA types, number of the bits, and the frequency operating speed.

The dissipated power of the proposed circuit was compared to other previous works taking in a count the FPGA kit platforms and families, the most popular FPGA types are the following: Altera Quartus-II, and Xilling for ISE software respectively. *Table 2* shows the proposed design project compared to the other previous works.

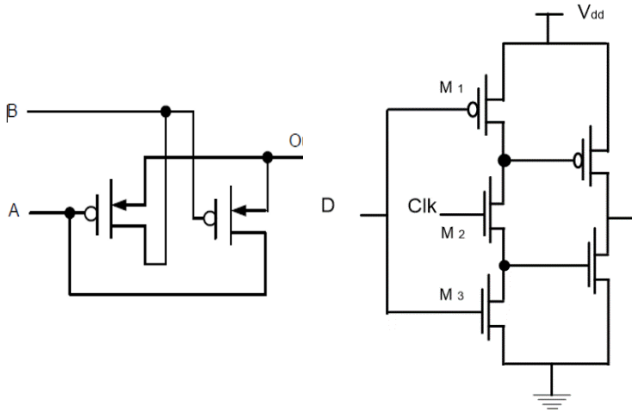
Table 2. A Comparison of The Power Dissipation Between the Proposed LFSR Circuit and the Previous Works

	[25]	[16]	[17]	Proposed
FPGA Type	Spartan 6	Spartan-6	Virtex5	Cyclone III
Power (mW)	59.84	36	147.72	55.55

All the presented FPGA kit (Spartan-6, Virtex5 and Cyclone III) in *table 2* known as a medium efficiency type. It was found that the implemented design has the less dissipated power than in other works. The power dissipation of the work in [16] has the lowest power in *table 2*, but this is at the expense of performance of the circuit during the term of the frequency operating speed 678.77 MHz and the timing delay 3.57nS regarding to the proposed design that has a higher operating speed (928.51 MHz) and 2.947nS delay time as shown in *table 1*.

4.3. Future work for Configuration of Improved LFSR Circuit based on CMOS Techniques

The LFSR circuit that employed 5-Tr. DFF Register and 2-Tr. XOR CMOS techniques are illustrated in *figure 8*. This will probably enhance the efficiency of the LFSR circuit by decreasing power consumption and minimizing the required space area. This could be achieved in the future work by utilizing the cadence software. In this part, the LFSR circuit suggested for the future work of this study can be configured in CMOS techniques with the aim of using a smaller number of transistors. Hence, the key element is the DFF blocks as well as XOR gates used in the LFSR design circuit. Based on C2MOS techniques, number of transistors was decreased in order to reduce the area size and power consumption. However, it could be lesser as in LFSR design model which exploits 2-transistor based XOR gate design chosen to be applied in the future proposed LFSR circuit [26]. Some designs of XOR gate may be done through using 8-transistors as in [27]. Also, XOR based 6- and 4-transistors can be implemented according to [28, 29] and [30, 31] respectively. Hence, designers target is to build the XOR gate with a minimum number of transistors. The given 2-transistor XOR gate of *figure 13 (a)* is a good choice [23]. The CMOS technique for D flip flop (DFF) design proposed in [32] was chosen to implement the proposed LFSR circuit since it only takes 5-transistors as in *figure 13 (b)*.



(a) (b)

Figure 13. (a) 2-Transistors XOR gate [30]; (b) 5-Transistors DFF CMOS Techniques [31]

The presented 2-Transistors XOR gate as well as the 5-Transistors DFF blocks were used to architect the LFSR circuit as in *figure 14*.

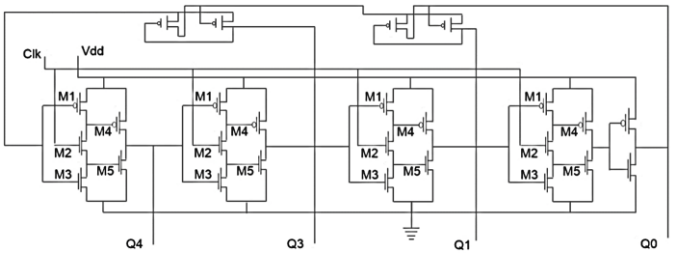


Figure 14. Improved LFSR circuit based on CMOS techniques

The LFSR circuit Based on five transistors (5-Tr). DFF Register and two transistors (2-Tr). XOR CMOS techniques shows that LFSR can be architected with 26 transistors. Hence, it can reduce the used transistors up to 43% of the conventional C2MOS logic (contains 60 transistors (12 for each of DFF and 6 for each XOR logic).

5. CONCLUSION

The analysis of the hybrid energy storage system, incorporating a battery and supercapacitor, reveals an effective approach to managing power demands in electric vehicles. The battery

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primarily addresses the initial power surge, delivering rapid response to immediate load demands, while the supercapacitor gradually steps in to support ongoing energy needs. This power-sharing arrangement helps maintain stability and prolong battery life by reducing excessive discharge cycles.

The coordinated control strategy, as demonstrated in the graphs, allows for a balanced power flow between the battery and supercapacitor, optimizing energy efficiency and ensuring that peak loads are effectively managed. The gradual engagement of the supercapacitor not only mitigates the stress on the battery but also leverages the high-power density of the supercapacitor to handle transient demands, enhancing overall system performance.

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