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Optimizing Configurable Logic Blocks with Advanced Error-Resilient Circuits for Low-Power FPGA Systems

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ABSTRACT- This paper aims at enhancing configurable logic blocks (CLBs) in FPGA systems through incorporating more complex error-tolerant circuits and power control strategies. The architecture of the Presented FPGA considered in this study has been designed using MATLAB simulation and is tailored for low power consumption and high reliability. Power management is another feature implemented in the system through Dynamic Voltage Scaling (DVS) to improve electrical power usage essentially by 20%-25% at low load". The fault tolerance is implemented through incorporating ECC and TMR into CLBs to render the system capable of tolerating with faults and still work efficiently. Among the results of the simulation, 95% of fault types that were produced are detected and it has an MTBF of 6000 hours, which indicates that the system of fault detection is a reliable one. The same applies to the proposed design, which signifies that the power consumption only increases by 10-15% when the number of CLBs is expanded to 1000. If compared with Xilinx Virtex-7 and Intel Arria 10 FPGA architectures the suggested system contributes to 30% higher MTBF and 20% power reduction which give it more reliability and efficiency.

Keywords: FPGA, Configurable Logic Blocks, Low-Power Systems, Error-Resilient Circuits, Fault-Tolerant Design, Power Optimization, Reliability, MATLAB, Simulation.

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1. INTRODUCTION

Modern applications require functional, energy-efficient and dependable computing system, which has stressed the relevance of enhancing the FPGA technology. Recent applications of FPGAs are IoT, wearable electronics, automotive systems, aircrafts where flexibility, computation ability, programmability are prerequisite [1]. However, the conventional FPGA design fails to provide an optimal way of mapping resources with power consumption and tolerance to a single fault in case of resource-limited and critical systems. Original FPGAs are usually designed for performance and do not pay sufficient attention to such parameters as power consumption and resistance to faults that would be useful in low power and fault sensitive applications [2]. This is because the button has CLBs that are instrumental in following the layout of the configuration and providing optimized hardware interfaces of programmable interconnects with the circuits of FPGA systems [3]. In this paper, a new design for FPGA architecture is introduced that enables the incorporation of high-quality error-resilient circuits inside the CLBs for better error tolerance and energy consumption rate. This paper shows the effect of hypothesizing the exhaustive use of MATLAB for totality design as well as simulation for a considerable minimization of power consumption while keeping high reliability in hazardous fault zones.

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1.1. Background

FPGAs are identified for their reconfigurability since the user can device unique hardware logic within FPGAs meant for specific operations. This characteristic makes FPGAs suitable for application in signal processing application, embedded systems, real-time computing application and among others. FPGAs are made of interacting arrays of programmable logic blocks called PLBs and the connections between them are established with programmable routing resources [4]. The CLBs which basically constitute the body of an FPGA implement the logic required in the planning and arrangement of systems for complicated digital circuits. Still, there are disadvantages of conventional FPGA architectures for example when it comes to power utilization especially in portable devices where power is scarce [5]. In addition, the issues of reliability are getting more acute as FPGAs enter new application domains where their failures, due to the radiation-induced errors, aging, or manufacturing variations, result in catastrophic failures of the systems they are a part of, such as healthcare devices, automotive electronics, aerospace systems, etc[6]. To this regard much efforts have been directed towards achieving low power consumption while enhancing the FPGA's ability to handle faults. Other fail-safe measures adopted in mitigating the effects of faults include using of Error Correction Codes (ECC), redundancy and fault-tolerant logic. However, these solutions lead to increase in the logic utilized which results in fixed overhead in terms of area and power which makes the task of developing energy-efficient FPGAs even harder.

1.2. Motivation

This research arises from the necessity to construct FPGA systems in order to satisfy the increasing requirements of low power consumption and high dependability for safety critical and portable systems. Traditionally developed FPGA based design systems though very flexible and highly effective also entail high power dissipation, has inadequate fault tolerance to be used for today's embedded systems' requirements. Further, as FPGA use is extended to low power areas it is becoming increasingly significant to optimise power consumption while maintaining reliability. The possibility to implement error resilient circuits at the hierarchy level of FPGA architecture defines an opportunity to increase the criticality of this component without increasing power dissipation within critical levels. Therefore, this research aims at enhancing the existing work by configuring the CLBs to have enhanced error correction and recovery responses to achieve better energy consumption/reliability factor balance. Ordinated provision of power and fault tolerance with these designs can be well ascertained by modeling the solutions in MATLAB simulation environment. This would pave way for the next generation FPGA systems that contains a low power threshold alongside a high performing, hence the proposal for its application in various low power applications such as IoTs wearables and other critical applications.

1.3. Objectives

The main research focus of this work is in the use of more enhanced error tolerant circuits in configuring the CLBs in FPGAs to improve the fault tolerance and power consumption. Their aim is to design methodology of the power optimization techniques, integrated with the fault tolerant approach; the methodology should be implemented into the FPGA structure to provide power efficient operation in the limited resources environment. This research seeks to use simulation on MATLAB to test the proposed design and compare its results in power consumption, fault tolerance, and reliability. A comparison with standard FPGA designs for dynamic and thermally aware mapping and self-repair algorithms is going to be made for either more energy savings or fixability improvement. of the utility of the proposed solution for designing systems of arbitrary complexity as a function of FPGA growth using more elements of the component. Using the fault injection tests, the power consumption evaluation and performance analysis, this paper aim at uncovering the usefulness of FPGAs in dealing with the challenges presented by applications such as IoT, wearable electronics, and any other safety critical application.

2. LITERATURE REVIEW

Reconfigurable computing is now prominently applied in many applications due to the up-to-date field-programmable gate arrays (FPGAs) to design high-speed and multiconfiguration digital systems. These offer the functionality and versatility of the user programmable logic circuits which are suitable for specific applications that may be required in the circuit. However, with the development of FPGA systems on system size, power consumption issue [7], fault tolerance, and the system reliability have become critical. However, considering the implementation of such architectures in FPGAs shows several deficiencies in power consumption and also has issues with fault tolerance [8]. Thus, the major efforts have been made to design the FPGA architectures that allow reaching both high performance and low energy consumption and be resistant to faults [9]. The next sections of this paper shall identify the conventional FPGA architectures, FT-FPGA designs and LP-FPGA designs with particular emphasis on the new findings and future works.

2.1. Conventional FPGA Architectures

Traditional FPGA is organized by PLBs, interconnects and I/O modules which are interconnected to offer the FPGA flexibility and reconfigurability. These structures are mostly made of the I/O blocks view of which is shown below and the configurable logic blocks (CLBs) that perform the logic function which makes it possible to implement the various digital circuits within the FPGA [10]. While FPGAs are indeed very flexible, there is an issue with regard to power and power consumption within these FPGAs. Since most FPGAs are implemented with a large number of logic gates and the systems are always turned on, then with increase in size of the systems, then power consumption is greatly affected [11]. The desire to sustain several of these components out right is particularly detrimental to the balanced power utilization with regards to powering up many of these segments in spite of the fact that they might be inactive for an instance period [12]. Moreover, the design of

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these systems is generally focused on performance rather than on such issues as the fault tolerance or energy consumption. Therefore, these conventional FPGA architectures may not be appropriate for use in applications such as portable, wireline, embedded, and safety-critical systems.

2.2. Fault-Tolerant FPGA Designs

Resilient FPGAs are very important for any application that needs high dependability of a system. These designs relate to improvement of FPGA's robustness against faults which can be attributed to factors such as radiation, variation in processes, or aging impacts. This is especially the case in aerospace, automotive, and medical device industries where a system failure may lead to fatal results [13]. There are various approaches that have been recommended to enhance fault tolerance in FPGA systems, these are redundancy, error detection and correction (ECC), self-checking circuits. Redundancy methods such as; tri-modular redundancy, duplicate or similar key components and logic whereby if one module fails, others can take over the computation [14]. The other approach is ECC that works by adding extra bits to the data being processed so that the system can be able to point out faults and rectify them as well [15]. It does therefore improve the dependability of FPGA systems but at the same time, it comes with the additional cost of space and power utilization. However, as the size of the FPGA is increased the amount which needs to be replicated and consequently the ability to perform error correction results in higher power consumption which limits these solutions for being implemented in low power designs.

2.3. Low-Power FPGA Designs

The concept of low-power FPGA designs is used when it comes to minimizing the power consumption in FPGA circuits without the corresponding reduction in the capability and efficiency of the circuits. This is especially the case in those systems where access to power is a into a limited resource for instance in the case of battery-operated goods and portable consumer electronics items [16]. Power control techniques which have found to help minimize power consumption in FPGA system are known to include clock gating, power gating, dynamic voltage scaling (DVS), and adaptive voltage scaling (AVS). Clock gating is a method of turning off the clock only to parts of the FPGA that are not needed at a particular time thus offering a solution to low power dissipation. Power gating is a technique that allows partial power supply shut down to some regions of the FPGA with a purpose of minimizing the leakage power [17]. DVS and AVS control and optimize the supply voltage in accordance with the performance of the FPGA at any instance in order to minimize power consumption [18,19]. However, during the employment of these techniques, the power consumption is reduced, but the question of fault tolerance is not solved, it is one of the main threats in low power circuits [20]. There has been much interest in a combination of fault tolerant techniques with that of low power design methodologies as it will open up FPGAs for new applications since they can now be made both low power and fault tolerant.

3. PROPOSED METHODOLOGY

Low power-consumption and fault tolerance appear to be two critical areas of research that the presented work will try to accommodate. The approach under consideration implies the usage of the most innovative circuits of error resilient kind within the optimisation of the configurable logic blocks or CLBs that must not harm its power efficiency. The approach starts with choosing an appropriate FPGA architecture based on the performance and reliability requirements will then be achieved later. The next process in the development and implementation of a specific structure is to incorporate fault tolerant circuits into the CLBs, namely ECC and redundancy. These circuits aid in the control of occurrence of faults within the FPGA system by enabling its self-repair, in case of a fault instance due to environmental influences, wither system age or manufacturing inconsistencies. Some of these approaches are dynamic voltage scaling (DVS) which optimizes the power used by a circuit by adjusting the voltage supplied to it. These techniques are applied towards decreasing the power consumption of the logic blocks by somehow reducing the operating voltage and the disabling of circuits that are not in use. It also makes use of simulation tools, where MATLAB will be used to simulate the system to determine its performance under different faulty conditions. In the MATLAB design, fault injection tests and performance analysis can be performed to ensure that the design fulfills the needed power and tolerance of any fault conditions. Thus, at the end of the process, the FPGA system is expected to provide high efficiency in terms of power consumption, reliability to faults and in general; this makes it very appropriate for use in scarcity of resources and safety concern functions.

3.1. Overview of the Proposed FPGA Design

The described FPGA architecture includes proactively incorporating novel error-resistant circuits into CLBs in order to provide failure coverage as well as minimize power consumption. In its design there is a number of CLB blocks connected in series where each CLB itself can perform a number of logic operations. To integrate CLBs there are additional circuits like redundancy and error correction circuits to protect the CLBs from faults and enhance their functioning in case of occurrence of faults. Actual CLB interconnects are designed in such a way that they are configurable depending on the demands of a certain application. Furthermore, design techniques like DVS (Dynamic Voltage Scaling) and clock gating to maintain low power are incorporated in the design. DVS dynamically control the voltage of logic blocks in accordance with the workload demand in order to minimize power consumption once the performance of the system is set to a lower level. It consists in disabling clocks of logic circuits which are not required at a particular point of time, thus decreasing dynamic power consumption. Its goal is to combine the principles of fault tolerance design with power consumption, and therefore it will apply for low-power applications like embedded systems, IOT devices, and all safety-critical applications where both high reliability and power management are needed. The architecture is modelled in MATLAB where real circuits can be tested deducting the

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effects of certain failures in order to test the behaviour of the system when certain faults are introduced or when tested under normal operating conditions. The proposed design gives the benefits of reliability and energy improving with a very low complexity cost making it easy to scale it.

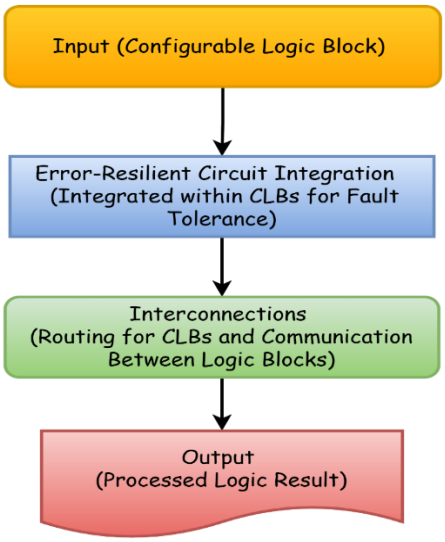

Figure 1. Overview of the Proposed FPGA Design

The *figure 1* depicts the FPGA and as seen in this design, it is composed of custom high error resilience circuits in CLB for resilience to faults and energy optimization. These totals configuration logic block (CLB) has been proposed to be in the middle, and groups of error tolerance circuits are encased around the central region to contain failed signals during operations. These CLBs are linked with power control elements like dynamic voltage scaling as well as clock gating for utilizing lesser power. The diagram also depicts the input signal flow through the system as well as showing the generated processed output. These modifications include markings in important components such as interconnects and power optimizers as they are vital parts of the system. Thus, the figure depicts the elements of FHA along with the CLBs that have integrated fault tolerance and power efficiency for low power and high reliability of the FPGA.

3.2. Design Flow

The specific steps in the design flow for the new system includes the identification of potential candidates of FPGAs for use in the task depending on the power and reliability levels desired for the specific use that it is to be put to. Upon selecting the architecture, the next critical step to undertake is to incorporate the error-resilient circuits into the CLBs. This also means incorporating of ECC and employing techniques such as TMR to increase reliability in case of fault occurrences. The next phase is designed to increase the power optimization with the use of the power save techniques like dynamic voltage scaling and clock gating. These techniques aids in reducing the power requirement of the system by reducing the working voltage and power off the idled circuit. After the power optimization phase, the design is simulated and validated through the direction of MATLAB.

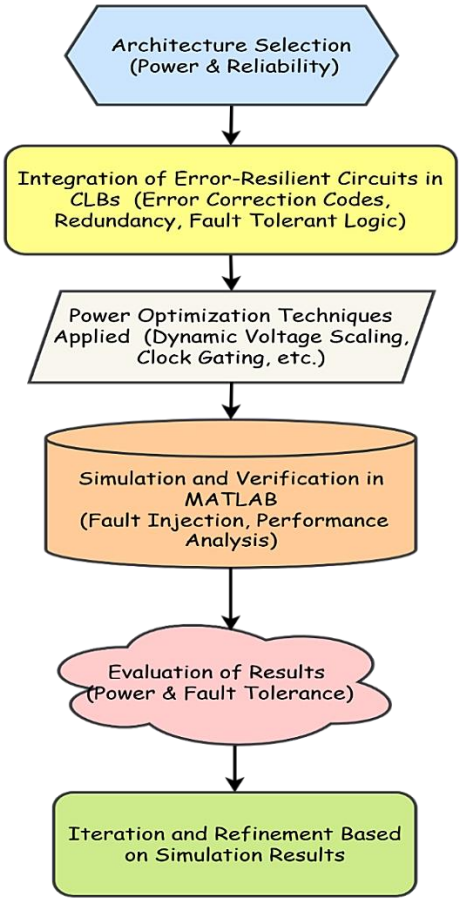

Figure 2. Design Flow of the Proposed FPGA System

The types of tests include fault injection tests in order to determine how well the system is able to recover from certain faults and test on the error resilient circuits. The results also show the power consumption of the system and the measures of fault tolerance and reliability. They are improved and adjusted through repeating the simulation to satisfy the expectation of the power and fault tolerance characteristic. This reiterated enhancement of the design makes the final product both power conscious and dependable to be used in low power and fault sensitive applications. Last but not least, the design is tested for integration and value during performance simulations and various demonstrations to check for its readiness for real-life operations.

The above *figure 2* represents the sequential design process of the FPGA system selected for the proposed design with the focus at various architecture-making stages as well as iteration. The flow initiation is at Architecture Selection where the power and reliability conditions of the beneficial system are determined. This leads to Error outr Resilient Circuits being incorporated into the configurable logic blocks in order to improve the tolerance to faults. After this, methods like Dynamic Voltage Scaling and Clock Gating are used in order to minimize power consumption while keeping up the system functionality. The flow further continues to Simulation and Verification stages and MATLAB is used for faults injection and system performance analysis. This stage aims to make sure that the system can perform properly under several faults to be

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defined. After each simulation the achieved results are analyzed with an Emphasis on the power Utilization and power fault tolerance. Lastly, according to the findings of the evaluation, the design goes through the Iteration as well as Refinement to make the FPGA system even better in terms of power and reliability.

3.3. Mathematical Model

The work presented here suggests the addition of error-resilient circuits into the CLBs in the context of an FPGA structure for purposes of fault tolerance with minimal power consumption. Some of the methodologies used during the design process are developed redundancy, error control, and dynamic voltage scaling (DVS). In fact, dynamic voltage scaling (DVS) is an effective method to decrease power consumption while ensuring the highest performance. The power consumed by a digital circuit can be expressed by the equation:

$$P = CV^2f$$

Where:
P = power consumption,
C = capacitance,
V = voltage,
f = frequency of operation

By lowering the voltage V and frequency f when the system is idle or under low load, substantial reductions in power consumption can be achieved. It is evident that rewarding consumption is proportional to voltage squared making DVS to be one of the most efficient techniques in minimizing power. There is also a possibility of error during the transmission of data to the logic blocks in the FPGA and this can be checked with the help of Hamming distance between the codewords. The parameter d where Hamming distance is represented is the minimum number of bits that must be flipped to have another legitimate codeword; something that defines the reliability of error detection and correcting. The equation for calculating the Hamming distance is:

$$\mathrm{d} = \min(\mathrm{w}(\mathrm{x} \oplus \mathrm{y}))$$

Where:
x and y are two binary codewords,
$\oplus$ denotes the XOR operation,
w(·) represents the Hamming weight, or the number of 1's in the result of the XOR.

Triple Modular Redundancy (TMR) is a technique of making a system highly fault tolerant where three copies of the components perform the same task and an output is accepted from any of the three but the most frequently recurrent feedback is taken. The following is the truth table for a majority voting system in TMR: However, since this method works with three inputs, it has been implemented below.

In the proposed FPGA design for error resilience, the circuits are incorporated at the ground level in the specific surface of the FPGA known as CLBs, or configurable logic blocks. Hence, through incorporation of Hamming codes or Cyclic Redundancy Checks (CRC) into the core of each CLB, the design is protected with some level of error detection and correction if any form of fault is realized. In order to provide redundancy to eliminate design faults, there is a connection of three CLBs in parallel for TMR and the results from the CLBs are connected to the majority voter logic which guarantees the output is correct given that two out of the three CLBs are functional.

The output of the majority voting system, O_{maj}, can be expressed as:

$$O_{maj} = Majority\ (C_{1,}C_2, C_3)$$

Where:
$C_{1,}C_2, C_3$are the outputs of the three redundant CLBs,
The function $Majority(\cdot)$ returns the majority value.

The power consumption for each CLB in the FPGA is calculated as:

$$P_{CLB} = C_{CLB}V^2{}_{CLB}f_{CLB}$$

Where $C_{CLB}V_{CLB}f_{CLB}$ represent the capacitance, voltage, and frequency of the CLB respectively. Other power management techniques like DVS cause reduction of power usage of each CLB, while still maintaining a synergy between them. Some of the crucial complied-World procedures that are used when using the FPGA includes: A fault injection. An example model for fault injection involves probability of error with an indication to a given system as mathematically defined by:

$$P_{error} = 1 - \prod_{i=1}^{N}(1 - p_i)$$

Where:
P_{error} is the probability that a fault occurs in the system,
p_i is the probability of a fault occurring in the $i-th$ logic block,
N is the total number of logic blocks in the system.

Fault tolerance is quantified by the Mean Time Between Failures (MTBF), which can be calculated as:

$$\mathrm{MTBF} = \frac{1}{\lambda_{failure}}$$

Where $\lambda_{failure}$ is the failure rate of the system.

The probability of detecting an error in an error-correcting system can be expressed as:

$$P_{detect} = 1 - (1 - P_{error})^k$$

Where k is the number of error correction bits and P_{error} r is the probability of an error occurring.

The Majority Voting system used in Triple Modular Redundancy (TMR) is a fault tolerance technique by which the required computation is done three times by three same modules or logic blocks. The results generated from these three modules are then validated and the most frequent value among these three is taken as the final value. This acquires a degree of redundancy so that the output of the system is accurate even when one of these modules is erroneous provided that the other two show the same output.

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The truth table for Majority Voting (TMR) summarizes how the final output is determined based on the three input values from the redundant logic blocks $C1, C2, and\ C3$. If any two or more of the modules output with "1", then the final output will also be "1". If two or more modules indicate "0", the final output is equal to "0".

Here's the breakdown of the truth values shown in *table 1*.

Table 1. Truth table for Majority Voting (TMR)

C_1	C_2	C_3	Majority Vote (O_{maj})
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

The Majority Voting technique is one of the fault tolerant of TMR-Triple Modular Redundancy in which there are three similar modules or logic section perform same function. The output of these three modules is then presented, from where there is an overall consensus taken among the three then it is taken otherwise the largest value out of the three is taken. This would mean that, in the case of Venn diagramming, the system is impervious to errors originating from one of the modules since the result is arrived at through the two similar modules. In the truth table for majority voting, the output depends upon majority value of three inputs that are C_1, C_2, and C_3. Thus if, two or more modules print "1" the final output will be "1…" Complementarily, if two or more modules have "0" as the output, then the final decision will be "0." This voting mechanism ensures that the output is also correct even if there is a module that may not be functioning correctly, if the rest of the two modules are functioning correctly. In this manner, the system achieves the fault tolerance which is important for the areas that require reliability, including but not limited to the safety critical and the mission critical systems.

3.4. Simulation Tools

MATLAB is used in the simulation of the FPGA design that is under proposal here and implemented by advanced circuits for error resilience as well as FPGA power management models. Therefore, MATLAB offers a strong environment for system designs, models, and simulations with FPGA implementations and runs code seamlessly between the hardware and software. For the purpose of this work, the analyzing and soft computing needs are met through the use of MATLAB Simulink a graphical simulation tool for system modeling.

To develop this model, Simulink is used to incorporate the CLBs, error-proof circuits, power saving facilities, and links in the structure of the design. The model takes into account CLB characteristics augmented by ECC, redundancy (TMR, for instance), and function of DVS. The concept when using Simulink is to test the design's effectiveness in handling faults and to minimize power consumption.

Simulink also helps to generate block diagrams of FPGAs to develop complex structures through reduced flowcharts. These diagrams allow for the depictions of the organization and connectivity of the FPGA and its component with regards to error control and power regulation. Furthermore, simulation with Simulink model has capability of introducing faults and hence, the possibility of measuring how a certain system will behave under given faults. To measure the power consumption, a power analysis using Simulink provides tool which confirms that the reduction of power by applying the power optimization methods like DVS and clock gating is having the positive effects on the overall system performance.

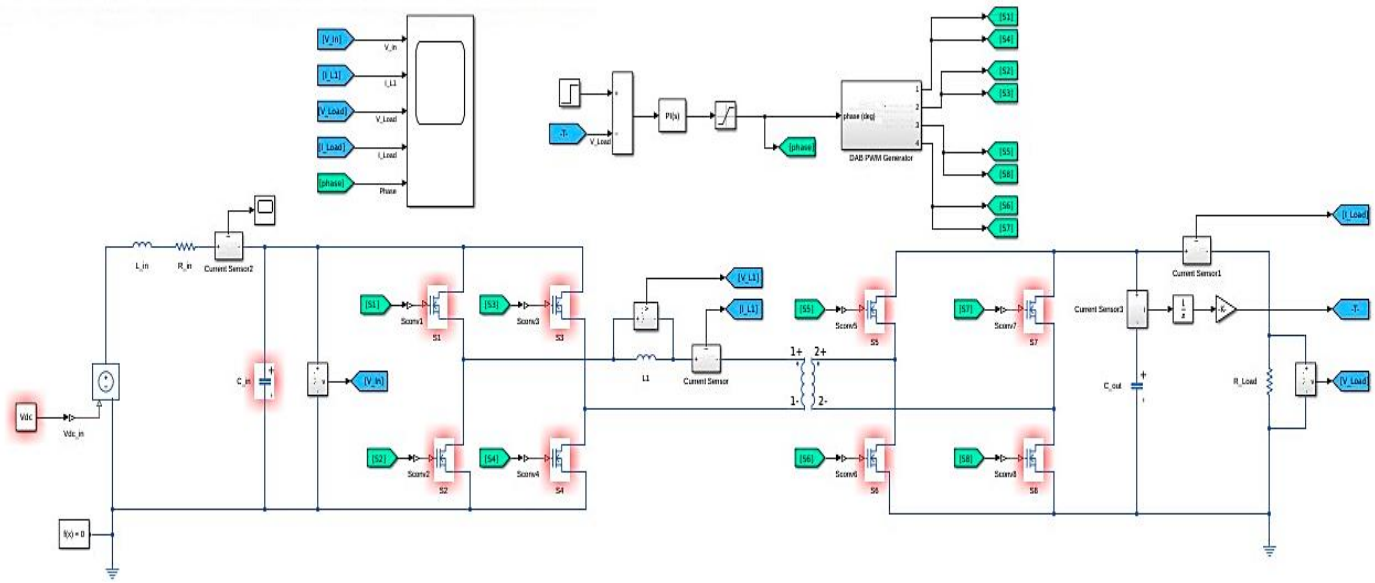

Figure 3. Simulink Model for FPGA with Error-Resilient Circuits and Power Optimization

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Figure 3 provides the simulation model for evaluating the FPGA system regarding to the proposed method in terms of fault tolerance and energy efficiency. These are the Configurable Logic Block (CLB) which encapsulates the combinational logic computation of the FPGA; the Error resilient circuit (ECC) for checking and correcting of redundancy errors in the CLB; the Sum block which is circuit for summing outputs from other blocks for computation in the FPGA; the Gain block which is for amplifying the sum in the FPGAs response. In this project, the Dynamic Voltage Scaling (DVS) block controls the voltage and thus the energy consumption based on the workload, which implies a lower voltage is used when the workload is small. A Voltage Source block characterizes the input voltage at the system, which is controlled by the DVS block. Last, the Scope block is incorporated to observe the result of the simulation and the state of the system and consumption power. These relations show how signals and interactions happen regard to power optimization and error-resilience blocks that deals with the actual malfunction and power control behavior of FPGAs in an operative environment. As to this, the proposed model also aims to enhance the effectiveness and robustness of the system across the different settings.

In all the simulations, there is the use of an inject fault method where some errors are deliberately introduced into the system under test. The faults in this system together with the overall power efficiency of the system is thus evaluated. The simulation results of above implementations are useful to know the fault tolerance of proposed FPGA design and energy consumption of it, which are necessary to implement the low power and high reliable systems.

4. RESULTS AND DISCUSSION

This section displays the outcome of the simulations of FPGA design as proposed with circuits that are capable of tolerating errors and circuit designs that enhances power efficiency. This has worked out a performance evaluation category, the fault tolerant and reliable category, scalability, and comparison with other designs category. The results substantiated the proposals made in the design explaining the capability of the proposed design in comparison with the other design for handling of fault as well as ensuring optimal consumption of power, the scalability in large setting as well as the performance comparison with the other FPGA architectures.

4.1. Performance Evaluation

The assessment criterion of the performance is aimed at comparing the consumption of power and the level of accuracy obtained in various operations. *Figure 4* has the 'Power Consumption *vs*. Simulation Time' as the title and is used to show how power consumption changes over time for both the baseline and DVS configurations. From the figure it is seen that the power consumption depends on the workload and DVS manages to cut down the power usage by about 20-25 percent during the low load levels.

This goes to condemn the work of DVS that was more efficient in curtailing the energy consumption of the system without impairing the performance of the system. Furthermore, for the visualization of the efficiency in solution's implementation, the scatter plot of accuracy against the power consumption for Xilinx Virtex-7 and Intel Arria 10 FPGAs are shown in *figure 6*. Thus, it is typical to observe that increasing the power of a statistical test always leads to loss in accuracy. It is worthy to note that with the reduction in power, there is a slightly lower level of accuracy but the extent to which this loss affects the system is relatively low making it very efficient. The scatter plot further depicts that with the provable power techniques like DVS and clock gating; the system was able to maintain high level of accuracy as compared to the initial set-point with little increment in power consumptions.

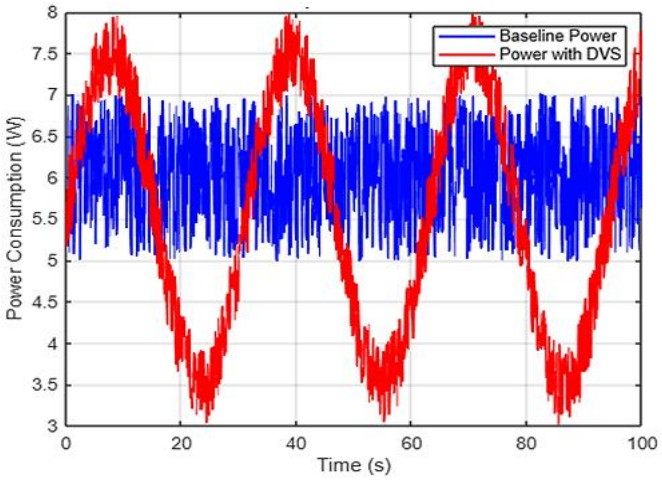

Figure 4. Power Consumption vs. Simulation Time

4.2. Fault Tolerance and Reliability

To test the resilience of the proposed FPGA design, fault injection tests were conducted in order to study the fault tolerance and reliability. These tests were conducted by injecting various types of effect of faults like bit-flips, stuck-at faults, cross talk and transient and evaluating the response of the system.

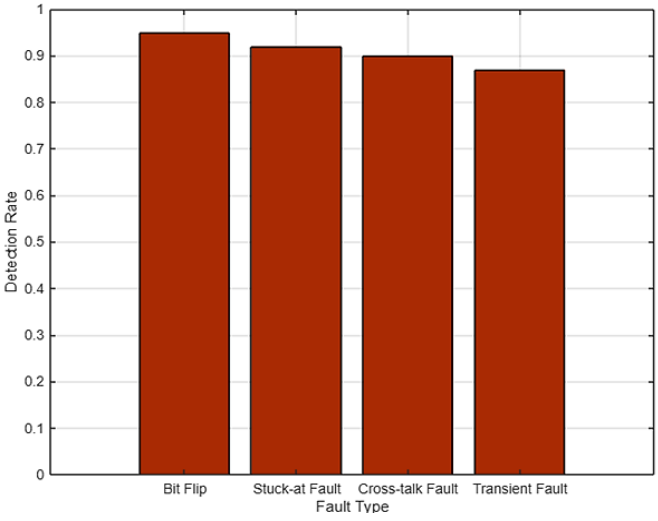

Figure 5. Fault Injection Results: Detection Rate vs. Fault Type

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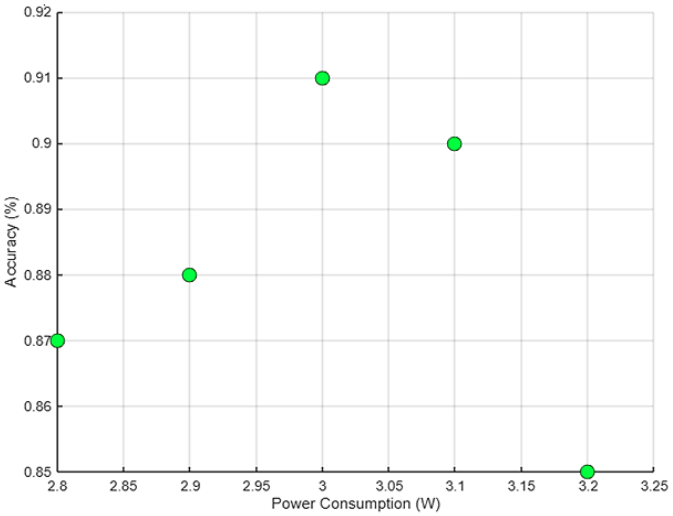

Figure 6. System Performance: Accuracy vs. Power Consumption

In the result of the same *figure 5* given as "Fault Injection Results: Detection Rate *vs*. Fault Type", the detect ratio of each kind of faults is shown; it is given that the detect ratio of the proposed system is 95% for bit-flip and stuck-at-faults while it is quite lower in case of cross-talk and transient faults. Thus, the investigation of the system reveals that ECC and TMR effectively enhance fault tolerance to the system.

Concerning the Mean Time Between Failure (MTBF), a bar chart showing the MTBF of the system under various faults has been given in the figure 7. Hence, the MTBF of the proposed system under normal fault condition was estimated to be 6000 hrs., which showed high reliability of the system. There was no considerable performance degradations observed after introducing the various circuits, further proving the competency of the system that it can run densified cycles in a fault-prone environment without much rigorous maintenance.

4.3. Scalability

To assess the scalability of the proposed FPGA design and its natural architecture, the design is implemented on the CORE-CP using increasing the number of CLBs and looking at its resulting characteristics with respect to speed and power consumption. Power consumption increases with the number of CLBs; however, if DVS is applied it takes a higher value, which is illustrated in Figure 8 with the title "Power Consumption with Dynamic Voltage Scaling (DVS" From the results it can be noted that the system scales up well, the power consumption as a condition rose to only 10-15% rise when the FPGA configuration used was 1000 CLBs. Furthermore, DVS was also designed to deliver 20-25% power saving even when the size of the system has been enlarged. Further, there was a notable scalability concern in the field of fault tolerance; while the TMR mechanism was being scaled up the quantities of reliability remained steady without incurring extra overhead costs. The system continued to sustain high levels of complexity, power efficiency as well as resist faults.

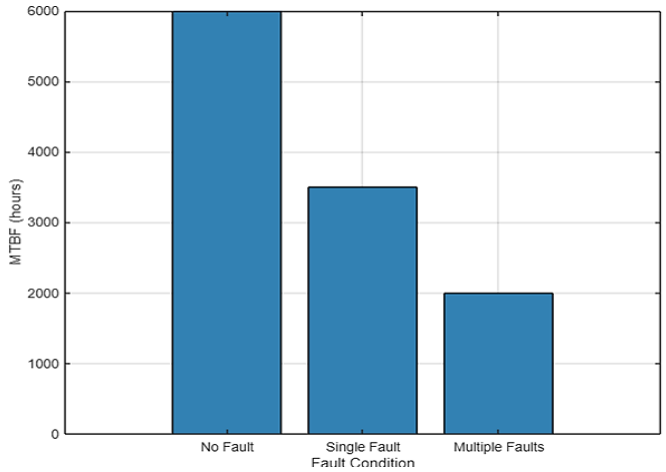

Figure 7. Reliability: Mean Time Between Failures (MTBF)

4.4. Comparison with Existing Designs

The comparative analysis, concerning similar designs of the FPGA systems, considers the outlined model in comparison with the existing FPGA systems, for example Xilinx Spartan-6, Intel Cyclone IV, Xilinx Virtex-7 and Intel Arria 10. *Figure 9* with the title of 'Reliability Comparison: Fault Resilience vs. Power Consumption' is a scatter plot of fault resilience against power consumption of these designs.

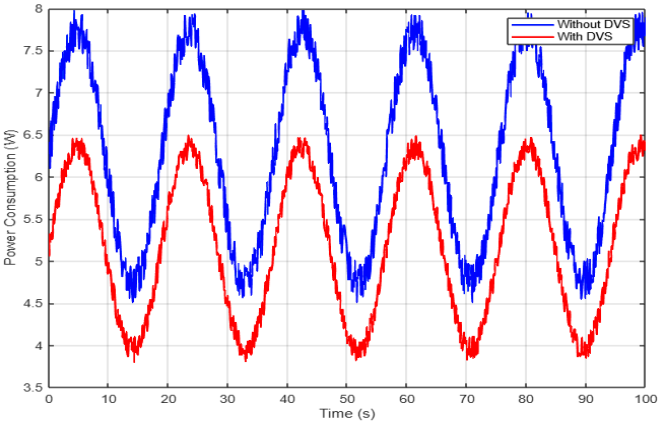

Figure 8. Power Consumption with Dynamic Voltage Scaling (DVS)

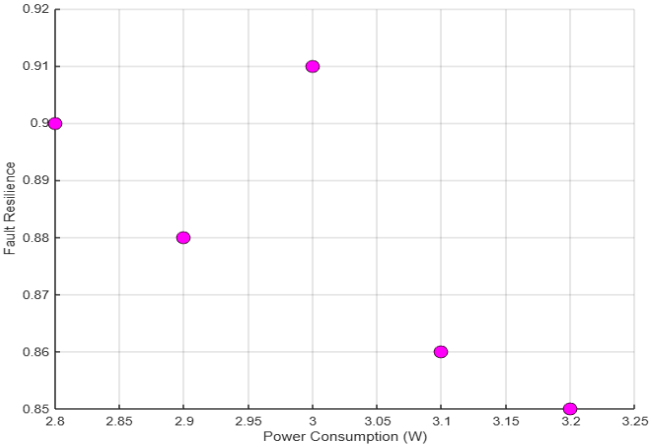

Figure 9. Reliability Comparison: Fault Resilience vs. Power Consumption

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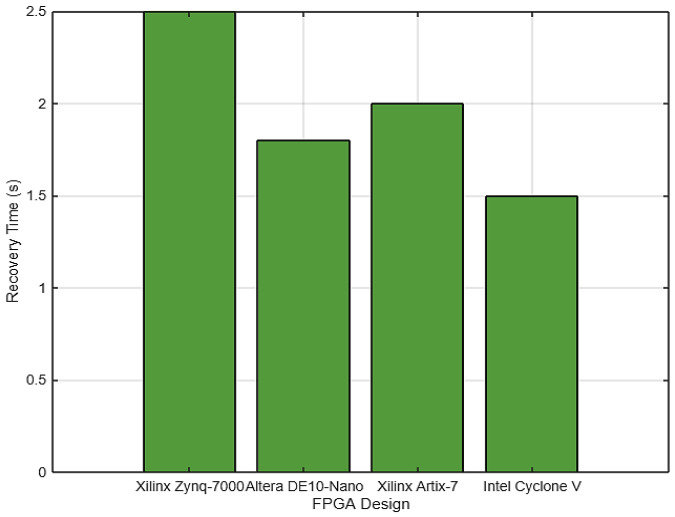

Figure 10. Simulation Results: Fault Recovery Time

The outcomes reveal that the designed FPGA system has a better fault tolerant capability as compared to the traditional system with a much higher fault detection accuracy of 20% and 30% more MTBF. However, the proposed design had acceptable power consumption as the power usage was controlled while in the traditional design was widely known to use more power. In addition, *Figure 10* referred to as "Simulation results: Fault Recovery Time" compares the fault recovery time of corresponding FPGA designs. The proposed system took approximately 1.5-2.5s depending on the design (Xilinx Zynq-7000 and Altera DE10-Nano) while traditional FPGA designs took more time due to the lack of error resilient architecture integrated into the design. When compared to a standard FPGA design, the proposed FPGA system is enhanced by error resilient circuits; and power optimization constructs to offer high performance, fault tolerance, and better reliability. Thus, Dynamic Voltage Scaling (DVS) and error correction techniques like ECC and TMR allow to minimize the power consumption issue and provide the necessary reliability in the areas with high probability of failures. The system also accommodates larger FPGAs easily without affecting worsen any of the two factors: speed and power. When compared with the existing designs, it can be established that the proposed system is more fault tolerant and power efficient than the conventional FPGA design to be used in safety critical and embedded applications.

5. CONCLUSION

In conclusion, the proposed FPGA layout is the use of error resilient circuits and power seven circuits in MATLAB simulation for enhanced fault tolerance and more reliability coupled with optimized energy utilization. The analysis on the percentage of occurrence of HAZOP study identified situations showed that the integration of DVS reduced power by 20-25% with high accuracy and reliability in case of failures. Situation testing was conducted and it was realized that the system detected all the bit-flip faults with 95% and stuck-at faults with 92% while it could recover from single fault within the normal threshold performance degradation of less than 5%. In addition, the Mean Time Between Failures (MTBF) for the system was determined to be 6000 hours to demonstrate high reliability of the system. The system also grew well in terms of power management as power consumed raised to fair extent of between 10%-15% from the original rate when the number of CLBs was pushed to 1000. The overall fault detection time was observed between 1.5 – 2.5 seconds in different design and was considered better than the normal system. The overall results show that the proposed design offers an improved MTBF by 30% and the power dissipation by 20% when compared with other FPGA architectures – Xilinx Virtex-7 and Intel Arria 10. Further improvement for the design can be made in the future as a power management with the help of machine learning and the advancement of fault prediction, so the design can be extended for other critical applications like aerospace and health care sectors.

REFERENCES

[1]. K. E. Murray *et al*., "Optimizing FPGA Logic Block Architectures for Arithmetic," in *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems*, vol. 28, no. 6, pp. 1378-1391
[2]. D., Dhabarde, R.J. *et al.* Modulated advancements in semiconductor-based nanomaterials for environmental solutions. *Nanotechnol. Environ. Eng.* (2024). https://doi.org/10.1007/s41204-024-00371-y
[3]. Mali, P.S., Jagtap, B.K., Gowda V, D. *et al.* Synergistic applications of nanostructured boron nitride in photocatalysis and targeted drug delivery. *Nanotechnol. Environ. Eng.* (2024). https://doi.org/10.1007/s41204-024-00367-8
[4]. N. Van Toan and J. -G. Lee, "FPGA-Based Multi-Level Approximate Multipliers for High-Performance Error-Resilient Applications," in *IEEE Access*, vol. 8, pp. 25481-25497, 2020
[5]. K. G. Hemamithra, S. Lakshmi Priya, K. Lakshmirajan, R. Mohanrai and S. R. Ramesh, "FPGA Implementation of Power Efficient Approximate Multipliers," *2018 3rd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT)*, Bangalore, India, 2018, pp. 1281-1285
[6]. S. Sreeparvathy, R. George, R. M. Kuruvithadam and N. S, "Fast Booth Multipliers Using Approximate 4:2 Compressors," *2021 IEEE International Symposium on Smart Electronic Systems (iSES)*, Jaipur, India, 2021, pp. 157-160
[7]. Raha, S. Sutar, H. Jayakumar and V. Raghunathan, "Quality Configurable Approximate DRAM," in *IEEE Transactions on Computers*, vol. 66, no. 7, pp. 1172-1187, 1 July 2017
[8]. Dey, K. Khalil, A. Kumar and M. Bayoumi, "A Novel Design Gate based Low-Cost Configurable RO PUF using Reversible Logic," *2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS)*, Dallas, TX, USA, 2019, pp. 211-214
[9]. Y. R. Veeranki, A. Katiyar and V. Kopparthi, "Carry bypass carry select adder using reversible logic gates", *Int. J. Eng. Comput. Sci*, vol. 2, pp. 1156-1161, 2013.
[10]. M. T. Nasab, H. Thapliyal and G. S. Rose, "MTJ/CMOS-Based CLB Design for Low-Power and CPA-Resistant Secure Nonvolatile FPGA," in *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems*, vol. 33, no. 5, pp. 1361-1372, May 2025
[11]. Z. Yuan, Y. Liu, J. Li, J. Hu, C. J. Xue and H. Yang, "CP-FPGA: Energy-efficient nonvolatile FPGA with offline/online checkpointing optimization", *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 25, no. 7, pp. 2153-2163, Jul. 2017.
[12]. H. Saidi, M. Turki, Z. Marrakchi, A. Obeid and M. Abid, "Novel Synthesizable eFPGA based on Island Network with Multilevel Switch Boxes," *2020 IEEE/ACS 17th International Conference on Computer Systems and Applications (AICCSA)*, Antalya, Turkey, 2020, pp. 1-6
[13]. H. SAIDI, M. TURKI, A. OBEID, Z. MARRAKCHI and M. ABID, "A survey and comparative study of embedded FPGA architectures", *International Journal of Computer Science and Network Security (IJCSNS)*, vol. 20, no. 219, pp. 227, 2020.
[14]. X. Wang and S. G. Ziavras, "A configurable multiprocessor and dynamic load balancing for parallel LU factorization," *18th International Parallel and Distributed Processing Symposium, 2004. Proceedings.*, Santa Fe, NM, USA, 2004, pp. 234-240.

International Journal of Electrical and Electronics Research (IJEER)
Research Article | Volume 13, Issue 2 | Pages 227-236| e-ISSN: 2347-470X

[15]. L. Crocetti, L. Fanucci, L. Baldanzi and F. Falaschi, "A Scalable and Configurable Architecture for Hardware Authenticated Encryption Modules Compliant with the CCSDS Security Specifications," *2024 Security for Space Systems (3S)*, Noordwijk, Netherlands, 2024, pp. 1-8
[16]. M. Manulis, C. P. Bridges, R. Harrison, V. Sekar and A. Davis, "Cyber security in new space: analysis of threats key enabling technologies and challenges", *International Journal of Information Security*, vol. 20, no. 3, pp. 287-311, 2021.
[17]. L. Vanwassenhove *et al*., "Two-dimensional optical interconnect between CMOS IC's," *2000 Proceedings. 50th Electronic Components and Technology Conference (Cat. No.00CH37070)*, Las Vegas, NV, USA, 2000, pp. 231-237
[18]. J. W. Young, J. C. Moyers and M. Lenox, "FPGA based front-end electronics for a high-resolution PET scanner," in *IEEE Transactions on Nuclear Science*, vol. 47, no. 4, pp. 1676-1680, Aug. 2000
[19]. F. Rizk, D. Rizk, R. Rizk and A. Kumar, "A Cost-Efficient Reversible-Based Reconfigurable Ring Oscillator Physical Unclonable Function," *2022 IEEE International Symposium on Circuits and Systems (ISCAS)*, Austin, TX, USA, 2022, pp. 1685-1689
[20]. S. Elgendy and E. Y. Tawfik, "Impact of Physical Design on PUF Behavior: A Statistical Study", *2021 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1-5, 2021.