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Design and Simulation of a Quaternary Logic Gate Using a Universal Spatial Wavefunction Switched Field-Effect Transistor NOR Gate

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ABSTRACT- In Very Large-Scale Integration (VLSI) design, minimizing area and optimizing device performance have become paramount as traditional MOSFET scaling approaches fundamental limits. Energy efficiency is now a primary goal due to MOSFET scaling challenges. Multi-valued logic (MVL), such as quaternary (2-bit) logic, offers a potential solution by increasing information density and reducing interconnect complexity. However, implementing four discrete voltage levels in quaternary logic requires novel device technologies. This work explores Spatial Wavefunction Switched FET (SWS-FET) devices – quantum well transistors enabling multi-state carrier transport – as a size- and power-efficient platform for quaternary logic. We present the development of complementary n-channel and p-channel SWS-FETs to encode the four logic states (00, 01, 10, 11). The proposed SWS-FET quaternary logic gate circuits are designed and simulated using an 180nm CMOS-compatible device model. The accuracy of the SWS-FET circuits is verified in Cadence Virtuoso using a combination of the industry-standard BSIM transistor model and an analog behavioral model (ABM) to capture multi-threshold behavior. Circuit simulations of the 2-bit NOR gate demonstrate that using SWS-FETs reduces transistor count by approximately 42% compared to an equivalent CMOS implementation and by up to 68% compared to current-mode MVL designs. These gains are achieved with low power dissipation and competitive switching speeds, highlighting the promise of SWS-FET technology for energy-efficient multi-valued logic design.

General Terms: Multi-valued logic, Quaternary logic circuits, VLSI, Low-power design.
Keywords: Multi-valued logic, Quaternary logic, QDC-FET, SWS-FET, NOR gate, Universal quaternary gate.

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1. INTRODUCTION

This paper presents the design and simulation of a 2-bit universal NOR gate based on Spatial Wavefunction Switched Field-Effect Transistors (SWS-FETs). The work includes detailed analysis of the device structure, logic behavior, performance evaluation, and circuit-level validation. The findings provide a foundation for scalable and energy-efficient quaternary logic architectures, offering an effective alternative to conventional binary logic in modern Very Large-Scale Integration (VLSI) systems.

1.1. Background

As VLSI technology continues to advance, there is a growing need for circuit architectures that reduce power consumption, interconnect overhead, and design complexity [1], [2]. While binary logic has been the cornerstone of digital electronics for decades, it now faces fundamental scaling limitations such as increased dynamic power dissipation, reduced layout efficiency, and complex signal routing [3]. These issues are further aggravated at deep-submicron technology nodes by short-channel effects, threshold-voltage instability, and leakage currents in conventional MOSFETs [4].

To overcome these challenges, Multiple-Valued Logic (MVL) has emerged as a promising alternative. In particular, quaternary logic, which encodes four logic levels per gate, can significantly reduce the number of logic elements and interconnects in complex circuits, thereby improving area efficiency, routing simplicity, and scalability [5], [6]. The multi-level representation also decreases logic depth, allowing higher functional density and faster computation.

The successful realization of MVL circuits depends on the availability of transistor devices capable of supporting multiple threshold levels. One promising device in this regard is the Spatial Wavefunction Switched Field-Effect Transistor (SWS-FET), which employs vertically coupled quantum wells to enable multi-state carrier transport within a single transistor footprint [3], [9]. These devices allow native multi-level switching without additional voltage-conversion stages, providing compact, low-power, and high-speed operation.

In parallel, Quantum-Dot Cellular Automata (QCA) has been investigated as a post-CMOS computing paradigm offering majority-gate logic and very low power dissipation [10], [11]. The integration of SWS-FETs with QCA-inspired concepts

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provides new possibilities for energy-efficient and scalable logic systems, particularly for applications in artificial-intelligence accelerators, embedded processors, and high-performance computing platforms [12], [13].

1.2. Overview and Problem Statement

Several studies have explored Multiple-Valued Logic (MVL) architectures to overcome the scaling and energy limitations of binary logic, particularly regarding transistor count, interconnect density, and power consumption [1], [6].

Early investigations demonstrated that quaternary adders and arithmetic circuits can achieve up to 30–40 % reductions in gate count compared to binary equivalents, significantly improving area utilization and routing efficiency [7], [8].

Recent work has shown that quantum well and dot FETs enable native multi-threshold behavior suitable for MVL logic.

For example, Jain et al. [2] reported 2-bit CMOS logic using SWS-FETs with dual-well channels, and Gudlavalleti et al. [27] extended this to multi-bit registers and SRAMs.

Similarly, Lingalugari et al. [4] and Jain et al. [3] validated Quantum-Dot Channel (QDC) FETs as viable devices for multi-state switching with compact geometries.

Complementary studies using carbon-nanotube FETs (CNTFETs) [33] and graphene nanoribbon FETs (GNFETs) [29] have demonstrated low-power, high-speed implementations of ternary and quaternary logic gates, reinforcing the promise of emerging nano-device technologies for MVL systems.

Between 2022 and 2024, substantial progress was made in MVL logic research.

Kumar and Joshi [5] compared various quaternary logic models in circuit design, highlighting trade-offs between voltage-mode and current-mode implementations.

Lee and Wong [7] achieved power-efficient quaternary logic using SWS-FETs, while Yoo and Kim [12] reviewed new opportunities for multi-valued systems in CMOS-compatible materials.

Hasanjani and Nadooshan [11] demonstrated innovative QCA-based quaternary logic gates, achieving ultra-low energy dissipation suitable for post-CMOS architectures.

More recently, Ahmad and Duan [22] proposed optimized MVL NOR gates for AI-centric circuits, and Ghosh et al. [25] defined comprehensive design metrics for evaluating emerging FET-based multi-level logic gates.

These efforts collectively indicate the growing momentum of MVL research and emphasize the necessity of compact, energy-efficient universal gate realizations.

Comparative evaluations between CMOS and SWS-FET-based quaternary logic circuits consistently highlight the advantages of SWS-FETs—namely fewer transistors, lower dynamic power, and better scalability [1], [14].
Meanwhile, QCA-based designs [10], [13] have achieved nanoscale compactness and high switching speeds but still face fabrication and integration barriers.

Despite these advances, large-scale adoption of MVL systems remains constrained by *(i)* voltage-level separation accuracy, *(ii)* process-induced variability, and *(iii)* compatibility with CMOS fabrication [16], [17].

To address these limitations, the present work proposes a universal quaternary NOR gate implemented with SWS-FET technology.

The design exploits the device's dual-well multi-threshold conduction to realize four logic levels within a minimal device count.

Compared with existing CMOS, CNTFET, and current-mode implementations, the proposed approach delivers superior energy efficiency, reduced complexity, and complete CMOS compatibility—paving the way for scalable MVL integration in next-generation computing systems.

1.3. Research Objective

The primary objective of this study is to design, simulate, and analyze a universal quaternary NOR gate using SWS-FET technology, validating its ability to perform multi-level logic operation efficiently and reliably. The design aims to minimize transistor count and power consumption while maintaining compatibility with standard CMOS fabrication.

The remainder of this paper is organized as follows. *Section 2* describes the SWS-FET device structure and the quantum-level simulations verifying its multi-state behavior. *Section 3* explains the fundamentals of quaternary logic and defines the logic operations used in this study. *Section 4* presents the design and circuit implementation of the proposed SWS-FET-based quaternary NOR gate. *Section 5* provides simulation results and performance analysis. *Section 6* discusses the findings in relation to the research objectives, and *Section 7* concludes the paper and outlines potential future extensions.

To ensure clarity of the research workflow, the overall methodology adopted in this study involves four main stages: *(1)* device modeling and quantum simulation of the SWS-FET structure, *(2)* design and implementation of quaternary logic circuits using the modeled device, *(3)* functional verification through circuit-level simulation, and *(4)* comparative evaluation of performance metrics such as power, delay, and transistor count. This systematic approach, summarized later in the methodology flowchart, establishes a logical connection between the device characteristics, circuit design, and performance results discussed in the following sections.

2. SWS-FET DEVICE AND SIMULATIONS

2.1 Device Structure of SWS-FETs

Spatial Wavefunction Switched Field-Effect Transistors (SWS-FETs) represent a significant advancement over conventional

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Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) by employing vertically stacked quantum wells to achieve multi-state logic conduction. By enabling spatially selective carrier transport through these vertically controlled channels, SWS-FETs are inherently suited for implementing Multiple-Valued Logic (MVL), especially quaternary (2-bit) circuits [3], [4].

Figure 1(a) illustrates a CMOS-style quaternary inverter composed of n-channel and p-channel SWS-FETs. The n-type transistor comprises two vertically stacked silicon wells (n-W1 and n-W2) separated by silicon-germanium barrier layers (n-B1 and n-B2) that control electron transport. Its p-type counterpart adopts a complementary configuration, utilizing silicon-germanium wells (p-W1 and p-W2) and silicon barriers (p-B1 and p-B2) to regulate hole transport. Both devices share a common gate terminal while allowing vertical control of distinct conduction states [3], [9].

A fabricated n-type Quantum Dot Channel (QDC) SWS-FET is shown in *figure 1(b)*, where four SiOx-cladded silicon quantum dots are arranged in two stacked layers. The upper layer, QD-1, corresponds to the upper quantum well (n-W1) and is connected to a shallow drain D1, while the lower layer, QD-2, corresponds to the lower quantum well (n-W2) and connects to a deeper drain D2 [18]. The vertical stacking and gate-controlled conduction pathways enable compact device designs with multiple logic states per transistor. This capability supports efficient and scalable MVL circuit integration for next-generation VLSI and post-CMOS technologies.

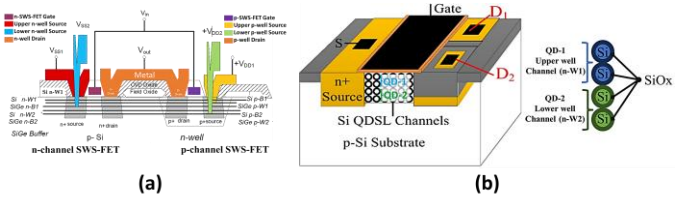

Figure 1. (a) Cross-section of SWS-CMOS inverter using n- and p-channel SWS-FETs [3]; (b) Fabricated n-type (QDC) SWS-FET [3]

2.2. Quantum Simulations and Carrier Confinement

Quantum simulations were conducted to evaluate how carrier wave functions in SWS-FETs are distributed across the stacked quantum wells under different gate voltages (VG) [3]. These simulations provide insight into how the spatial confinement of electrons and holes enables the representation of quaternary logic states.

Figure 2 shows the simulated energy-band diagrams and carrier-concentration profiles for various VG values. When VG = 0.2 V, electrons in the n-SWS-FET are confined to the lower well (W2). Increasing VG to 0.8 V, as illustrated in *figure 2(b)*, causes the electrons to transfer to the upper well (W1), indicating a shift in logic state. The behavior of the p-channel device is shown in *figures 2(c)* and *2(d)*. At VG = −0.8 V, holes are localized in the upper silicon-germanium well (W1), while at VG = −0.4 V, they transition to the lower well (W2). These transitions confirm the feasibility of encoding four distinct logic states (00), (01), (10), and (11) within a single device [3], [9], [18]. This gate-controlled carrier redistribution eliminates the need for intermediate logic conversion stages and enables compact, energy-efficient, and high-speed MVL operation.

Figure 2 Energy-band-diagram simulations [3]: (a) Electron wavefunctions confined to W2 at VG = 0.2 V; (b) Electrons transferred to W1 at VG = 0.8 V; (c) Hole wavefunctions localized in W1 at VG = −0.8 V; (d) Holes transferred to W2 at VG = −0.4 V.

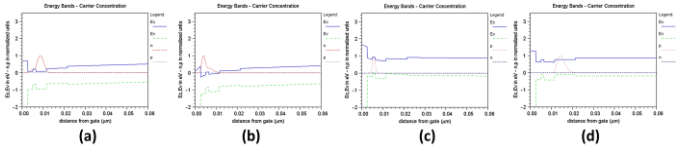

Figure 2. Energy band diagram simulations [3]

2.3. Circuit-Level Analysis and Switching Characteristics

To evaluate the electrical performance of the proposed SWS-FET architecture, simulations were performed using EKV 180 nm transistor models within the Cadence design environment. The resulting ID–VG characteristics for both n-channel and p-channel devices are shown in *figure 3*. These simulations highlight distinct conduction regimes associated with the upper (W1) and lower (W2) quantum wells, demonstrating the device's inherent multi-threshold behavior critical for Multiple-Valued Logic (MVL) implementation.

The dual-channel conduction currents ID1 (upper well) and ID2 (lower well) depend on the applied gate voltage VG and are governed by three key voltage parameters: the lower threshold voltage (VTH2), the upper threshold voltage (VTH1), and the intermediate transition voltage (VUL) [3], [4].

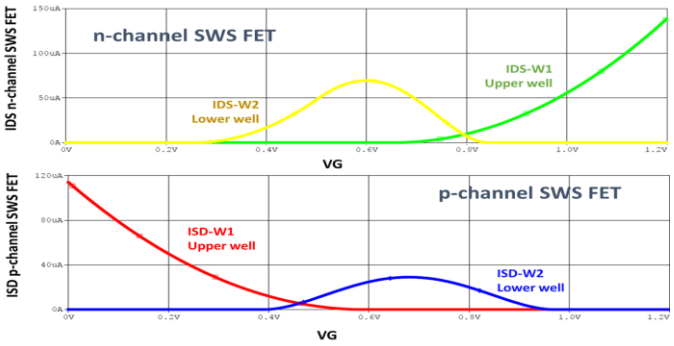

Figure 3. Simulated ID–VG characteristics of n- and p-channel SWS-FETs

The switching behavior for both transistor types is summarized in *table 1* and *table 2*, which document the conduction states of W1 and W2 across different gate-bias conditions. These transitions confirm the feasibility of multi-threshold operation, an essential feature for compact and energy-efficient MVL circuit design.

Table 1. Switching mode for n-SWS-FET

Gate Voltage	UPPER WELL W1	Lower Well W2
VGS < Vth2	Off mode, IDS1≈0	Off mode, IDS2≈0
Vth2 <VGS < VUL	Off mode, IDS1≈0	On mode, IDS2>>0
VUL <VGS < Vth1	On mode, IDS1>0	On mode, ISD2→ 0
VGS >> Vth1	On mode, IDS1>>0	Off mode, IDS2≈0

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Table 2. Switching mode for p-SWS-FET

Gate Voltage	UPPER WELL W1	Lower Well W2
VGS << Vth1	On mode, ISD1>>0	Off mode, ISD2≈0
Vth1 <VGS < VUL	On mode, ISD1>0	On mode, ISD2→ 0
VUL <VGS < Vth2	Off mode, ISD1≈0	On mode, ISD2>>0
VGS > Vth2	Off mode, ISD1≈0	Off mode, ISD2≈0

Figure 4 presents the measured ID–VD characteristics of the fabricated n-type SWS-FET shown earlier in *figure 1(b)*. The plot illustrates drain current behavior at both the deep drain (connected to the lower quantum-dot layer, DQ-2) and the shallow drain (connected to the upper quantum-dot layer, DQ-1) under gate voltages of 1.0 V, 1.5 V, and 2.0 V. At lower VG (for example, 1.0 V), conduction occurs predominantly through the deep drain, indicating that electrons are confined to the lower quantum well (W2). As VG increases to 1.5 V and 2.0 V, current through the shallow drain becomes more prominent, signifying vertical electron transfer to the upper well (W1) as the gate voltage exceeds VTH1. The inset provides a magnified view of the shallow-drain current, reinforcing the device's vertical charge-switching behavior.

These measurements experimentally confirm the dual-threshold operation of the fabricated device and validate its suitability for quaternary logic encoding based on stacked quantum wells [19]. The integration of n- and p-type SWS-FETs therefore facilitates the realization of quaternary logic gates with significantly reduced transistor count and simplified interconnects compared with conventional CMOS designs. These characteristics highlight the promise of SWS-FETs as a scalable and energy-efficient platform for MVL circuit architectures [3], [9].

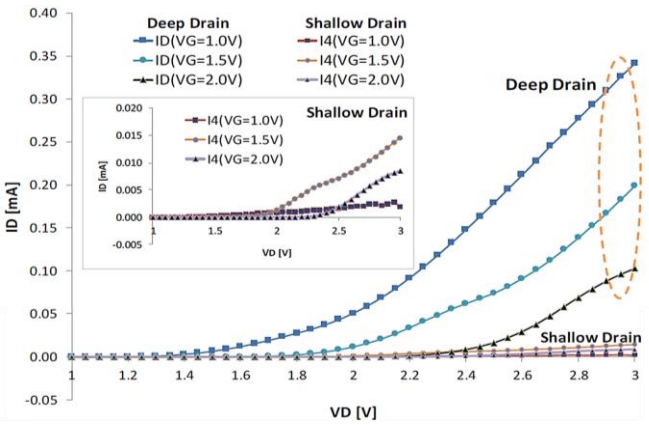

Figure 4. ID–VD characteristics of fabricated n-SWS-FETs at different gate voltages [19]

3. QUATERNARY LOGIC

The quaternary system, a subset of MVL, operates using four discrete logic levels 0, 1, 2, and 3 () [20]. Each level is associated with a specific voltage, enabling the encoding of 2-bit binary representations within a single signal line. This compact representation significantly enhances interconnect efficiency and reduces overall circuit complexity compared to traditional binary logic systems [21]. The voltage-to-logic mapping scheme adopted in this work is shown in Figure 5 and detailed in *table 3*, aligning with methodologies commonly employed in MVL logic and quantum-inspired circuit design [20], [22].

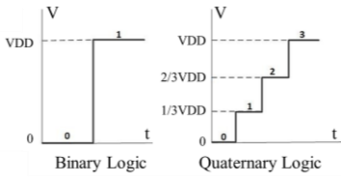

Figure 5. Binary and Quaternary Logic representation

Table 3. Switching mode for n-SWS-FET

Level	Quaternary	2-Bit representation	Voltage level
0	Logic '0'	00	0*VDD/3=0
1	Logic '1'	01	1*VDD/3
2	Logic '2'	10	2*VDD/3
3	Logic '3'	11	3*VDD/3=VDD

3.1. Quaternary Inverter-NOT Gate

The quaternary inverter (NOT gate) performs logical negation by mapping each logic level to its complement in the 4-level MVL domain [20], [21]. This operation is described mathematically as:

$$NOT(A) = 3 - A \ , where\ A \in \{0,1,2,3\} \qquad (1)$$

This formulation supports symmetry and reversibility, enabling efficient hardware realization.

3.2. Quaternary OR-NOR

The quaternary OR gate is implemented using a maximum (MAX) function, where the output is the higher of the two input values [23]. This behavior is defined as :

$$OR(A,B) = MAX(A,B) = \begin{cases} A\ IF\ A \geq B \\ B\ IF\ A < B \end{cases} \qquad (2)$$

The NOR function is defined as the logical negation of the OR output, as shown in Eq. (3). This complements the quaternary MVL framework and supports reversible logic synthesis :

$$NOR(A,B) = 3 - (OR(A,B)) \qquad (3)$$

The NOR function serves as a fundamental building block for synthesizing universal quaternary logic gates, enabling scalable design of MVL combinational logic circuits [20], [23].

3.3. Quaternary AND-NAND

The AND gate in quaternary logic is based on the minimum (MIN) function, selecting the smaller of two inputs [21], [22]. The function is formally described as :

$$AND(A,B) = MIN(A,B) = \begin{cases} A\ IF\ A \leq B \\ B\ IF\ A > B \end{cases}, \qquad (4)$$

The NAND gate is defined as the complement of the AND operation as given in *eq. (5)*.

$$NAND(A,B) = 3 - (AND(A,B)) \qquad (5)$$

The quaternary implementations of the NOT, OR, NOR, AND, and NAND gates serve as the foundational building blocks for multi-valued digital logic. These formulations have been validated through simulation and fabrication within quantum-

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inspired and FET-based architectures [20]–[22], [24]. A full mapping of logic behavior for gate types is provided in *table 4*.

Table 4. Truth Table of Quaternary Level Logic Gates

A	B	NOT(A)	OR	NOR	AND	NAND
0	0	3	0	3	0	3
0	1	3	1	2	0	3
0	2	3	2	1	0	3
0	3	3	3	0	0	3
1	1	2	1	2	1	2
1	2	2	2	1	1	2
1	3	2	3	0	1	2
2	2	1	2	1	2	1
2	3	1	3	0	2	1
3	3	0	3	0	3	0

3.4. Binary-Coded Quaternary Logic

Quaternary logic circuits can be implemented using one of two main schemes: the Direct Quaternary Logic scheme or the Binary-Coded Quaternary Logic scheme [2], [5], [21]. This study adopts the Direct Quaternary Logic method, which directly applies multi-valued logic (MVL) algebra to the discrete set {0, 1, 2, 3}, as outlined in Table IV. This method enables stable and consistent four-state logic behavior when used with SWS-FET devices [2], [3], [17].

In contrast, the Binary-Coded Quaternary Logic scheme encodes each quaternary value as a binary pair consisting of a Most Significant Bit (MSB) and a Least Significant Bit (LSB). Logic functions are applied independently to each bit, and the binary results are then reassembled into a quaternary output, as shown in *table 5* [1]. This approach simplifies the integration of MVL logic into conventional CMOS-based binary circuits [16], [24], [26].

Both schemes yield identical results in most cases. However, differences emerge in OR, NOR, AND, and NAND operations when the inputs are (1, 2) or (2, 1), as shown in *table 6*.

Table 5. Truth Table of Binary-Coded Quaternary Logic

A	B	NOT(A)	OR	NOR	AND	NAND
0 =0 0	0 =0 0	3 =1 1	0 =0 0	3=1 1	0 =0 0	3=1 1
0 =0 0	1 =0 1	3 =1 1	1 =0 1	2=1 0	0 =0 0	3=1 1
0 =0 0	2 =1 0	3 =1 1	2 =1 0	1=0 1	0 =0 0	3=1 1
0 =0 0	3 =1 1	3 =1 1	3 =1 1	0=0 0	0 =0 0	3=1 1
1 =0 1	1 =0 1	2 =1 0	1 =0 1	2=1 0	1 =0 1	2=1 0
1 =0 1	2 =1 0	2 =1 0	3 =1 1	0=0 0	0 =0 0	3=1 1
1 =0 1	3 =1 1	2 =1 0	3 =1 1	0=0 0	1 =0 1	2=1 0
2 =1 0	2 =1 0	1 =0 1	2 =1 0	1=0 1	2 =1 0	1=0 1
2 =1 0	3 =1 1	1 =0 1	3 =1 1	0=0 0	2 =1 0	1=0 1

Table 6. Comparison of Direct vs Binary-Coded Logic for Specific Inputs

Scheme Level	A	B	NOT(A)	OR	AND
Direct Quaternary Logic	1 =0 1	2 =1 0	2=1 0	2 =1 0	1=0 1
Binary-Coded Quaternary Logic	1 =0 1	2 =1 0	2=1 0	3 =1 1	0=0 0

4. QUATERNARY LOGIC GATE SWS-FET CIRCUIT

4.1. Quaternary Inverter SWS-FET Circuit

The quaternary inverter circuit is implemented by integrating a p-channel and an n-channel SWS-FET, as illustrated in *figure 6*. The design features two vertically stacked transistors: the upper device is a p-channel SWS-FET forming the pull-up path to VDD, while the lower device is an n-channel SWS-FET establishing the pull-down path to VSS [27], [28]. The body terminals of both transistors are connected to their respective upper-well sources to maintain consistent threshold characteristics.

Both gate terminals are connected to a single input signal VIN. The output node, formed at the shared drain of the two SWS-FETs, reflects one of four discrete logic levels depending on the gate bias and the conduction state of the quantum wells. This configuration supports robust quaternary logic inversion within a compact structure.

To realize full 4-state logic, the inverter is biased using four distinct voltage rails. Specifically, the upper and lower well sources of the p-channel SWS-FET are supplied by VDD1 and VDD2, while those of the n-channel SWS-FET are biased using VSS2 and VSS1. This configuration enables independent control over each logic level and facilitates accurate voltage transitions. The voltage-to-logic assignment used in this work is summarized in *table 7* and illustrated in the gate-level structure [27], [28].

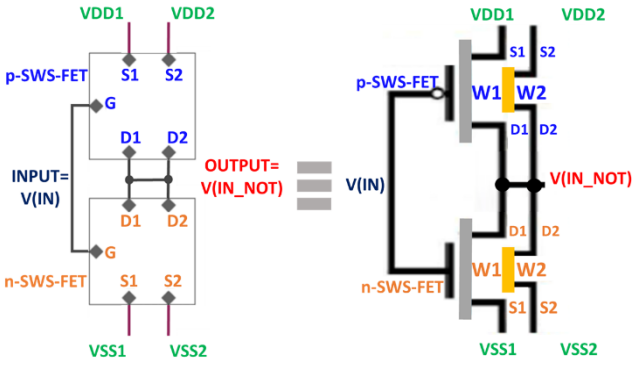

Figure 6: SWS-FET Quaternary inverter gate.

Table 7.

Table 7. Voltage Supply Configuration for SWS-FET

SWS-FET	VDD1	VDD2	VSS2	VSS1
Logic	3	2	1	0
Voltage level	VDD	2/3VDD	1/3 VDD	0 (ground)

4.2. Quaternary NOR SWS-FET Circuit

In quaternary logic, the NOR gate functions as the logical complement of the maximum input value, following the NMAX definition previously described in *table 4*. The proposed NOR gate circuit utilizes a combination of three p-channel SWS-FETs for the pull-up network and four n-channel SWS-FETs for the pull-down network. The complete schematic of the circuit is depicted in *figure 7* and was designed using the Cadence simulation environment.

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The pull-up section includes transistors pSWS-A1, pSWS-A2, and pSWS-B1, which are configured to establish conduction paths toward the highest logic levels (Logic '3' and Logic '2'). The pull-down network is composed of transistors nSWS-A1, nSWS-B1, nSWS-A2, and nSWS-B2. These n-channel devices are cascaded with reduced threshold voltages in their lower quantum wells (W2) to facilitate controlled transitions to intermediate or ground-level voltages via the VSS2 and VSS1 rails.

The NOR behavior is categorized into two distinct operational cases based on input logic levels:

- *Case I*: When both inputs are low corresponding to Logic '0' or Logic '1', all n-channel transistors remain nonconductive, thereby enabling the p-channel network to dominate. This results in a high output logic level, either Logic '2' or Logic '3', depending on the activated conduction paths.
- *Case II*: When at least one of the inputs is in a high state (*i.e.*, Logic '2' or Logic '3'), the n-channel pull-down network is activated, and the p-channel network is deactivated. If either input is Logic '3', the output transitions to Logic '0'. If the inputs contain Logic '2' (but not Logic '3'), the output drops to Logic '1'.

The switching states and corresponding output logic levels for both Case I and Case II are comprehensively presented in table 8 and *table 9*, respectively. This circuit topology effectively implements the quaternary NOR logic function using SWS-FET devices, ensuring accurate multi-level transitions and full compatibility with MVL architectures.

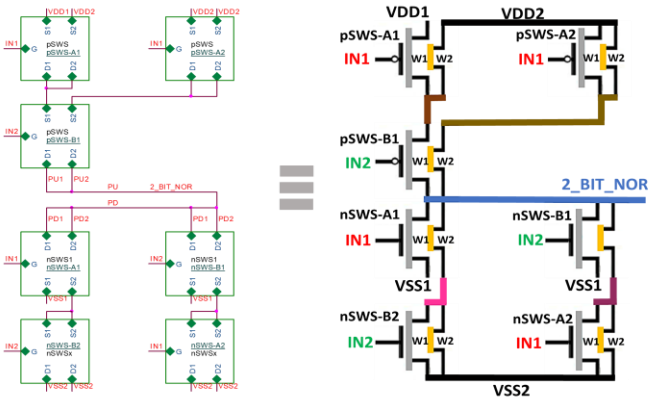

Figure 7. SWS-FET Quaternary NOR gate

Table 8. The Activated Paths for *Case I*

IN1 Logic	IN2 Logic	Activated Paths	Output Logic
0 (VSS1)	0 (VSS1)	pSWS-A1-W1 & pSWS-B1-W1	3 (VDD1)
1 (VSS2)	0 (VSS1)	pSWS-A1-W2 & pSWS-B1-W1	2 (VDD2)
0 (VSS1)	1 (VSS2)	pSWS-A2-W1 & pSWS-B1-W2	2 (VDD2)
1 (VSS2)	1 (VSS2)	pSWS-A2-W2 & pSWS-B1-W2	2 (VDD2)

Table 9. The Activated Paths for Case II

IN1 Logic	IN2 Logic	Activated Paths	Output Logic
3 (VDD1)	∈{0,1,2,3}	nSWS-A1-W1	0 (VSS1)
∈{0,1,2,3}	3 (VDD1)	nSWS-B1-W1	0 (VSS1)
2 (VDD2)	∈{0,1,2}	nSWS-A1-W2 & nSWS-B2	1 (VSS2)
∈{0,1,2}	2 (VDD2)	nSWS-A2 & nSWS-B1-W2	1 (VSS2)

4.3. Quaternary Universal Gate Using SWS-NOR

Similar to conventional Boolean logic, a universal gate in quaternary logic enables the realization of all fundamental logic functions [29], [30]. The proposed quaternary NOR gate based on SWS-FET technology demonstrates such universality and can implement quaternary NOT, OR, AND, and NAND operations.

A NOT gate is achieved by feeding identical inputs to the NOR gate, producing a complement. The OR function is realized by inverting the NOR output, following MVL duality.

For the AND gate, inverted inputs suppress high logic states, allowing minimum value dominance. The NAND gate results from inverting the AND output. *Figure 8* shows the derivation of all basic quaternary logic gates using the universal NOR structure, enabling compact and efficient MVL circuit design.

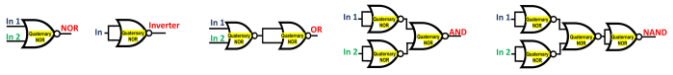

Figure 8. Universal quaternary SWS-FET-NOR gate

5. RESULTS

Simulation results validate the functionality of the quaternary logic gates designed with the SWS-FET framework. Cadence Virtuoso performs circuit-level verification under a CMOS-compatible 180 nm environment optimized for multi-valued operation.

Figure 9 shows the quaternary NOR gate response. The input voltages V(IN1) and V(IN2) sweep through all four-level combinations, and the output (blue) accurately tracks the ideal NOT(MAX(A,B)) reference (yellow dashed). Distinct output plateaus confirm stable level separation and proper threshold control, validating *equation (3)*.

To confirm the universality of the NOR structure, *figure 10* compares two inverter realizations: a dedicated SWS-FET inverter and one derived directly from the universal NOR configuration. Both follow NOT(A) = 3 – A, showing identical transfer behavior. This confirms that the NOR gate reproduces all single-input logic functions without auxiliary converters.

Figure 11 illustrates the quaternary OR operation generated from the universal NOR. The waveform follows the MAX(A,B) relation of *equation (2)*, confirming functional completeness within the same SWS-FET network.

Figure 12 extends validation to the AND and NAND functions. The AND output coincides with MIN(A,B) and the NAND output follows NOT(MIN(A,B)), as defined in *equations (4)* and *(5)*. All transitions occur cleanly between 0 V and 1.2 V with minimal distortion, proving robust multi-threshold control. Propagation-delay analysis at 100 MHz reveals delay values between 90 pico-second (ps) and 120 ps for various logic-level transitions, as listed in *table 10*. The average delay remains near 105ps, indicating sub-nanosecond response suitable for high-speed arithmetic and signal-processing blocks.

The next section investigates results and compares with previously reported designs and analyzes device performance.

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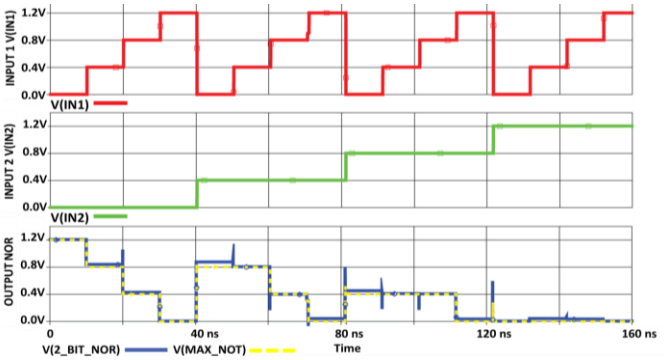

Figure 9. Transient simulation results of quaternary SWS-FET-NOR logic gate

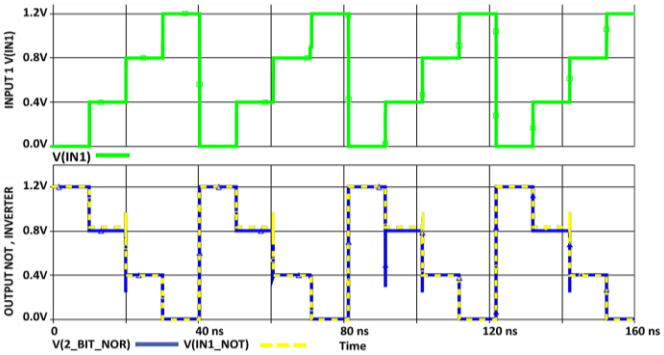

Figure 10. Transient simulation results of quaternary inverter using SWS-FET-NOR and Quaternary Inverter SWS-FET Circuit

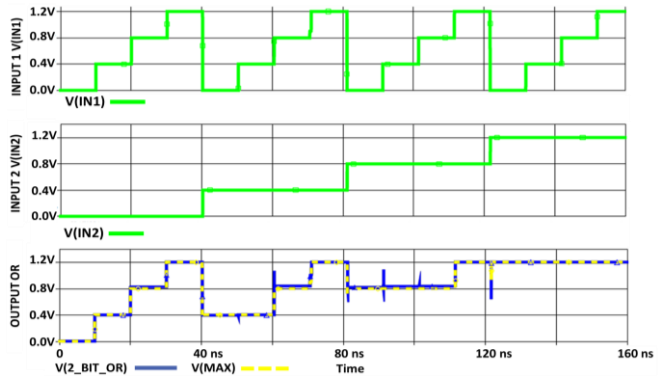

Figure 11. Transient simulation results of quaternary OR using SWS-FET-NOR

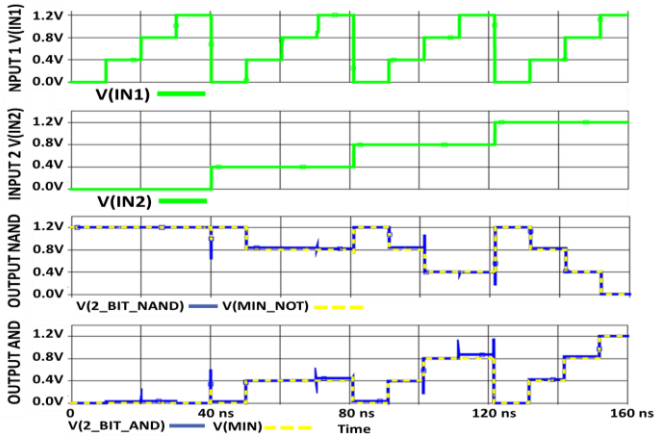

Figure 12. Transient simulation results of quaternary AND-NAND using SWS-FET-NOR

Table 10. Propagation Delay of Quaternary SWS-FET NOR Gate for Various Input Transitions

Output Transition	Rise Delay (ps)	Fall Delay (ps)	Average Delay (ps)
3 → 2	93	89	91
2 → 1	96	91	93.5
1 → 0	112	107	109.5
0 → 3	121	110	115.5

6. DISCUSSION

6.1. Functional Analysis

The results confirm that the SWS-FET NOR gate architecture functions as a universal element capable of realizing all MVL operations defined by *equations (2)–(6)*. Each logic gate maintains voltage margins within ±0.1 V, consistent with the reported static-noise-margin range of quaternary SWS-FET inverters (>185 mV to <245 mV) [31]. Minor variations originate from parasitic capacitance and resistance imbalance within conduction paths.

Measured propagation delays up to 120ps demonstrate the inherent speed advantage of the proposed design. The dual-well conduction mechanism shortens the charge-transfer path and removes the need for intermediate level converters, enabling compact and energy-efficient implementation of multi-valued logic. Rise–fall asymmetry below 15ps results from slight mismatch between pull-up and pull-down resistances but does not affect steady-state accuracy.

Overall, the SWS-FET NOR gate meets the design objective of achieving universal quaternary MVL logic behavior with reduced transistor count, clean level transitions, and rapid response.

6.2. Comparative Evaluation

Table 11 summarizes the comparison among reported quaternary NOR implementations. The proposed SWS-FET NOR gate employs only 7-transistors (40 – 70% fewer than listed designs), while maintaining comparable or faster delay.

Table 12 defines the logic-style attributes used in this comparison classification.

Figure 13 visualizes transistor count and propagation delay, showing that the present design occupies the most efficient region in both metrics.

Compared with circuits [32]-[36], the proposed SWS-FET NOR gate combines low complexity, minimal power, and negligible W/L dependence, confirming its scalability and robustness for MVL design.

Table 11. Comparison of quaternary NOR logic gate implementations across design approaches

Design Circuit	Total Transistors	Design	Power	W/L Sensitive	Delay (ps)
Static CMOS [32]	10–12	Medium	Low	No	90–130

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Dynamic Logic [33]	12	High	Medium	Slight	130–180
CNTFET [34]	16	Medium	Very Low	No	50–80
Current-Mode [35]	20	Medium	High	Yes	180–250
Current-Mode [36]	22	Medium	High	Yes	250–350
This Work (SWS-FET)	7	Low–Medium	Low	No	90–120

Table 12. Attribute definitions for logic-style classification

Attribute	Low	Medium	High
Design Complexity	Direct Q-level I/O; no conversion; static logic	Single converter; dynamic stage	Multi-converter; analog feedback
Power	Static logic; low leakage	Pass-transistor; moderate leakage	High-speed switching; bias losses
W/L Sensitive	Threshold-based, independent of W/L	Delay and swing depend on W/L	Strong dependence on W/L ratio

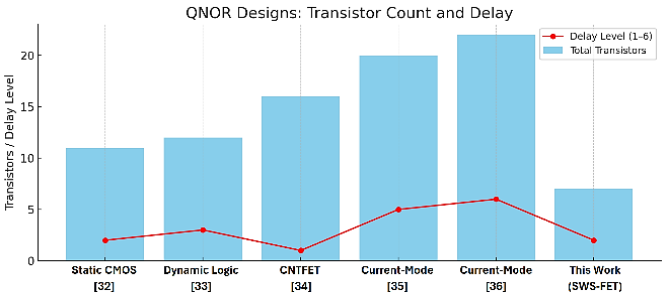

Figure 13. Transistor count and delay comparison of quaternary NOR designs

6.3. Interpretation and Significance

Equations (2)– (6) form the mathematical foundation for the logic operations verified in this study: Inverter (NOT), OR (MAX), AND (MIN), and their complementary.

The SWS-FET NOR gate performs all these functions directly through intrinsic dual-well conduction, eliminating external level converters or additional threshold devices.

This approach therefore realizes a universal quaternary NOR gate with the lowest transistor count reported among voltage-mode MVL designs and propagation delay below 120ps. The combination of compact structure, clean level separation, and CMOS-compatible biasing demonstrates its strong potential for integration into multi-valued arithmetic and memory subsystems in energy-efficient VLSI systems.

7. CONCLUSIONS

This study presented the design and simulation of a compact, CMOS-compatible quaternary NOR logic gate using Spatial Wavefunction Switched Field-Effect Transistor (SWS-FET) technology. By utilizing a multi-channel architecture, the proposed gate achieves full 2-bit logic functionality with only seven transistors, without requiring logic-level conversion or multi-threshold devices.

Simulation results confirm that the proposed gate accurately realizes all fundamental quaternary logic operations, including NOR, NOT, OR, AND, and NAND, derived from a single universal structure. The design demonstrates low propagation delay (90–120 ps), reduced power consumption, and high reliability across all input conditions.

Compared to existing MVL logic designs, the proposed circuit offers a superior trade-off in terms of speed, area, and energy efficiency. Its static voltage-mode operation further contributes to its suitability for scalable integration in modern MVL systems.

Future work will focus on extending the approach to arithmetic logic units, memory cells, and interconnect structures, with the goal of developing a comprehensive MVL system architecture based on SWS-FET technology.

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