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Design, Stage-Wise Power Loss Evaluation and Real-Time Validation of Totem-Pole Bridgeless Boost Converter Against DBR–Boost PFC Topology

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ABSTRACT- Conventional AC–DC power factor correction (PFC) systems typically employ a diode bridge rectifier (DBR) followed by a boost converter, resulting in significant conduction losses due to multiple semiconductor paths. This paper presents a comprehensive design, modeling, and comparative loss analysis of a Totem-Pole Bridgeless Boost Converter (TPBBC) as an efficient alternative to the DBR–Boost configuration. The proposed topology eliminates the front-end diode bridge, reducing conduction and switching losses while improving efficiency and power quality. Detailed MATLAB/Simulink simulations and real-time validation using OPAL-RT demonstrate the superior performance of the Totem-Pole converter, achieving higher efficiency, lower total harmonic distortion (THD), and near-unity power factor. A stage-wise power loss evaluation further confirms reduced device stress and ripple-free DC-link voltage. The results validate the Totem-Pole topology as a high-performance solution for next-generation AC–DC conversion applications requiring enhanced efficiency and power quality.

Keywords: Bridgeless PFC Topology, Stage-wise Loss Breakdown, Voltage Stress Mitigation, Interleaved Totem-Pole Converter, Real-Time HIL Validation.

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1. INTRODUCTION

The rapid growth of power electronics in renewable energy systems, electric vehicles, data centers, and industrial drives has significantly increased the demand for efficient AC–DC conversion systems[1], [2]. These converters serve as the essential front-end interface between the utility grid and DC loads, with stringent requirements for high efficiency, power quality, and near-unity power factor [3]. Traditionally, AC–DC power conversion is achieved through a diode bridge rectifier (DBR) followed by a boost converter operating in continuous conduction mode to enforce power factor correction (PFC) [4], [5], [6]. While this configuration is simple and widely adopted, it suffers from notable efficiency limitations. Nearly 48% of total conduction losses originate from the combination of the DBR and boost diode, resulting in reduced overall efficiency and increased thermal stress [7].

To overcome these challenges, bridgeless topologies have been introduced, eliminating the DBR stage to reduce conduction paths and switching losses [8], [9]. Among them, the totem-pole bridgeless boost converter has emerged as a promising candidate due to its ability to combine high efficiency, reduced component stress, and compact design. Several studies [2], [8], [9], [10], [11], [12], [13], [14] have reported the use of totem-pole converters for applications in data center power supplies, EV onboard chargers, and renewable energy interfaces, highlighting their potential for next-generation AC–DC front ends. Unlike existing works that focus on control optimization or hardware prototyping, this paper performs a component-level, stage-wise loss analysis and validates the Totem-Pole converter using real-time (RT) OPAL-RT simulation, bridging the gap between theoretical and experimental efficiency evaluation. The results obtained are presented quantitatively and graphically for better clarity. A summary of existing works and their limitations is presented in *table 1*, followed by a quantitative performance comparison of the proposed converter.

Table 1. Comparison of Reference Topologies, Their Limitations, and the Contributions of the Proposed Converter.

Ref	Topology / Method	Key Limitation	This Work Contribution
[8]	Totem-Pole Bridgeless PFC with phase-angle control	Grid polarity current spikes; limited stage-wise loss data	Adds loss breakdown and presented smooth frequency-based close loop control

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[12]	GaN-based Totem-Pole, improved light load efficiency	Light load only; less about full load or open-loop soft-switching; focused on load efficiency only	real time soft-switching verification of design and wide load range
[13]	Totem-Pole with various devices	Doesn't show real-time system behavior; output control via switching frequency not studied	real-time HIL, and demonstration of output DC voltage regulation by frequency
[14]	Totem-Pole BL PFC with auxiliary ZVT	Adds component complexity; limited to high frequency; no wide load or frequency variation	frequency-based control over wide range, soft-switching at lower kHz, simpler topology
[9]	Interlaced Totem-Pole PFC prototype	Limited power ratings and fewer comparative data vs DBR-Boost	Compares DBR-Boost vs Totem-Pole; wider frequency variation
[11]	Triangular current mode + interleaving	Lower power; sampling & circuit complexity	Larger scale, higher power, full-range ZVS verification in RT
[10]	Bidirectional interleaved PFC for EV chargers	Limited soft-switching across full frequency range; parasitic losses prominent	Incorporates soft-switching, stage-wise loss, frequency control etc.

2. DBR AND BOOST CONVERTER

Figure 1 shows the conventional boost [12] converter configurations used after a diode bridge rectifier for power factor correction (PFC). This topology is highly used in PFC circuits, however in many articles it is claimed that this topology has a disadvantage of less efficiency due to conduction losses of the diode bridge rectifier and the boost diode, against it the use of advanced bridgeless topologies such as the totem-pole converter shown in *figure 1(b)* has widely become popular. Ahead in this paper the design and control of Totem pole converter for PFC operation is done in MATLAB Simulink and the design is validated with the real time hardware in loop OPAL RT 4510. Also, efficiency, power factor calculation at wide input voltage range, total harmonic distortion (THD) of the proposed developed design *i.e.* Totem pole design against conventional converter is done.

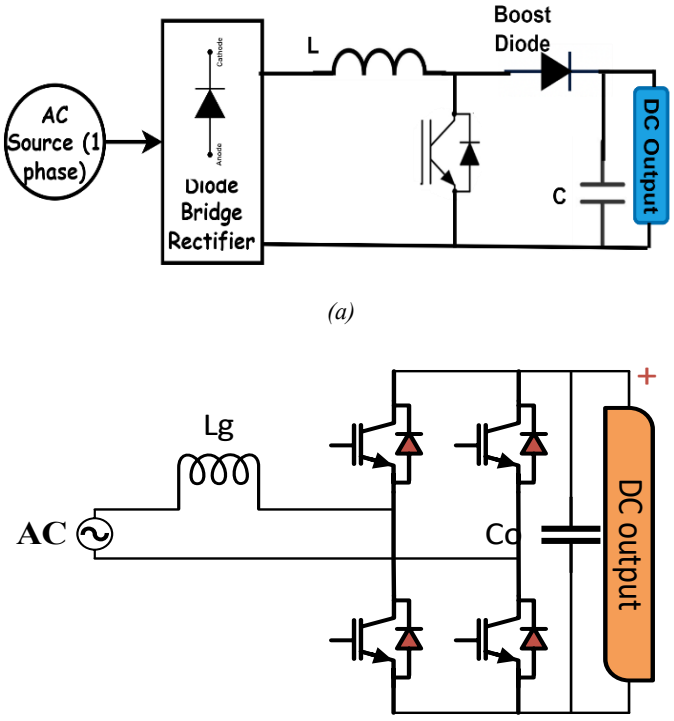

Figure 1. (a) DBR and Boost converter (b) DBR and Interleaved boost converter

3. TOTEM POLE STRUCTURE AND DESIGN

Totem-pole bridgeless boost converter (TpBBC) shown in *figure 1(b)* eliminates the diode bridge stage and conduct current through 4 active switches. Studies discussed in Table 1 have claimed their highly efficient operations and discussed control strategies, however still stage wise power loss analysis, voltage stress on used components is not much explored. At very high frequencies, switching losses dominate and efficiency degrades, while at lower frequencies, the passive components become bulky[4]. In this work, totem pole topology is examined for a 2.5 kW, 400 V application with switching frequency of 40 kHz to provide a practical balance between efficiency, component size, and thermal performance. Considering 20 % and 2 % ripple in current and voltage respectively, the inductor L_g and capacitor C_o is obtained through standard *equations (1-2)* [3].

$$L_g = \frac{V_{out}}{4 \times f_{sw} \times I_{ripple}} \quad (1)$$

$$C_o = \frac{P_{out}/V_{out}}{4\pi \times f_{line} \times V_{ripple}} \quad (2)$$

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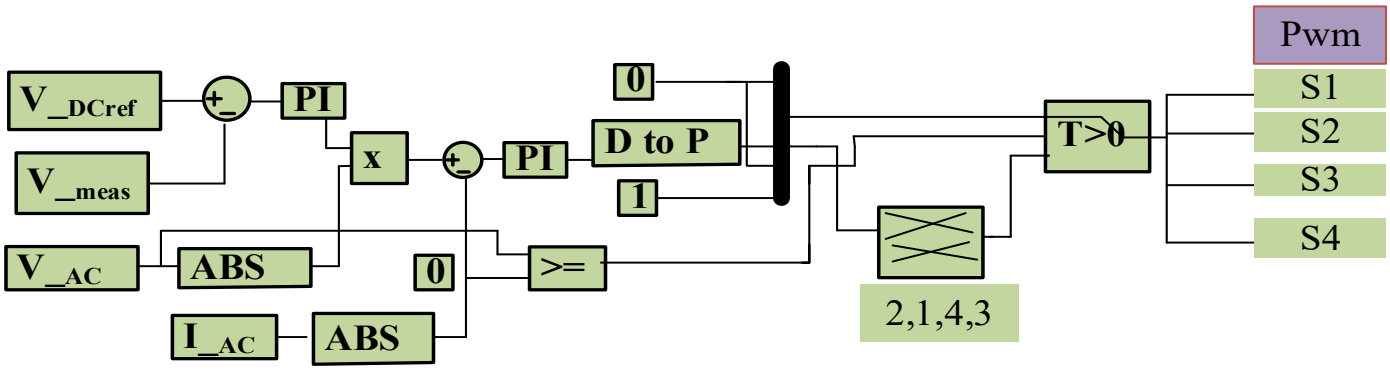


Figure 3. Control structure

The control strategy shown in *fig. 3* employs a dual-loop architecture comprising an outer voltage loop and an inner current loop. In the outer loop, the DC-link voltage is regulated by comparing the measured voltage V_{mens} with the reference voltage V_{DCref} resulting in voltage error $e_V(t)$ expressed in *equation (3).*

$$e_V(t) = V_{DCref} - V_{mens} \qquad (3)$$

This error signal is processed by a proportional–integral (PI) controller to generate the reference input current amplitude I_{ACref}, given in equation (4), The PI controller in this loop maintains the DC bus voltage constant under varying load conditions through proportional–integral gains K_{p1} and K_{i1}. The inner current control loop ensures that the actual input current I_{AC} follows the reference current I_{ACref} and a current error $e_I(t)$ is generated shown *in equation (5).*

$$I_{ACref} = K_{p1}\, e_V(t) + K_{i1} \int e_V(t)\, dt \qquad (4)$$

$$e_I(t) = I_{ACref} - I_{AC} \qquad (5)$$

This error is applied to another PI controller, characterized by proportional gain K_{p2} and integral gain K_{i2}, which generates the control voltage $v_{control}(t)$ given in *equation (6).*

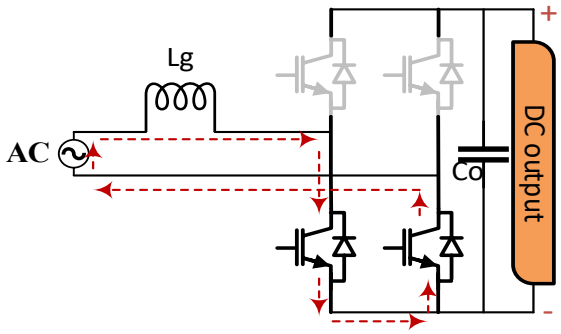
$$v_{control}(t) = K_{p2}\, e_I(t) + K_{i2} \int e_I(t)\, dt \qquad (6)$$

The control voltage is compared with a high-frequency triangular carrier signal $v_{carrier}(t)$ to produce the PWM gating signals for the IGBTs. Depending on the polarity of the input AC voltage V_{AC}, the Totem-Pole operates in one of two conduction modes. During the positive half-cycle, switches S_1 and S_4 are active, while during the negative half-cycle, switches S_2 and S_3 conduct, mathematically shown in *equations (7-8).*

$$\text{If } V_{AC} \geq 0 \Rightarrow \text{Mode A: (S1, S4 active)} \qquad (7)$$

$$\text{If } V_{AC} < 0 \Rightarrow \text{Mode B: (S2, S3 active)} \qquad (8)$$

Under the proposed control strategy, the Totem-Pole PFC converter operates in four distinct modes during each AC cycle, as illustrated in *fig. 4*. The active switch pair is determined by the input voltage polarity, ensuring bidirectional current flow with minimal conduction loss. During the positive half-cycle, switches S2 and S4 are activated, that charges the inductor for the on time, while in the left time of the positive half inductor discharges through S2 and S4. In the negative half-cycle, S1 and S3 are engaged to charge the inductor again bit the direction of current in the inductor reverses. And finally, the energy is discharged to the load from S2 and S3 to have intact direction of DC output. In the control scheme the absolute value of inductor current is considered owing to the fact that the current in the inductor reverses in each positive and negative half cycles, that cannot be supported with the PI controller for providing optimal control. The gate pulses generated from the control scheme to switches S1, S2, S3 and S4 charges the inductor and discharges inductor energy to the load in such a way that input current shapes in phase with AC voltage providing unity power factor at input side. The obtained value inductor is responsible for its continuous conduction mode in phase. The capacitor draws out ripples from the output voltage providing ripple free DC output.



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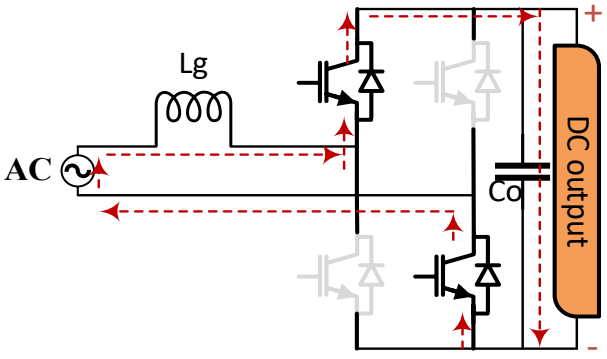

(b)

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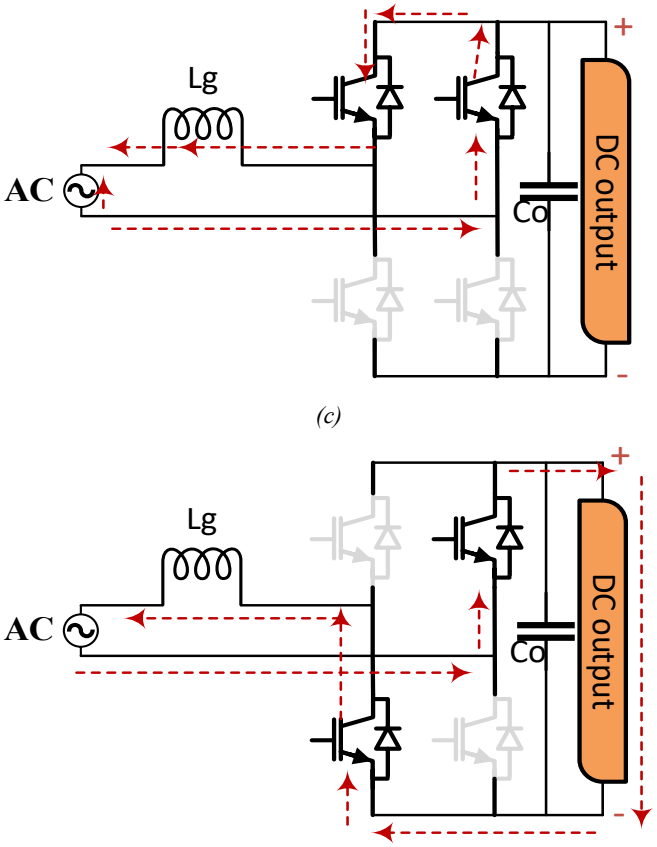

Figure 4. 4-Modes of operation (a) Inductor charging in Positive half cycle (b) output to load and inductor discharging (c) inductor charging in negative half cycle (direction reversed) (d) inductor discharging to load from same side of output as previous

4. SIMULATION AND HIL RESULTS

The topology shown in *figure 1(b)* is developed in MATLAB Simulink, to analyses its performance on three main criteria's, *(i)* attainment of Unity power factor for wide AC input voltage range *(ii)* DC output with less than 5% ripple *(iii)* performance of control for wide DC output voltage variation. *Figure 5(a)* shows the obtained simulation results for lowest input voltage first. The Figure has to displays; the first display shows the Input AC voltage (with 120-volt peak) in blue color and input AC current in orange color. Both sinusoidal voltage and current are in phase with each other which resembles of attainment to unity power factor. The second display in the same *figure 5(a)* shows 400 volts DC output with ripples less than 5%.

The topology is then tested at rated voltage of 325-volt peak in the second stage, the result obtained are presented in *figure 5(b)*. This Figure also consist of 2 displays similar to *figure 5(a)*. The alignment of sinusoidal input AC voltage and current in phase with each other confirms the attainment of unity power factor for the applied voltage. in this case also the output load voltage has ripple less than 5% in the DC output.

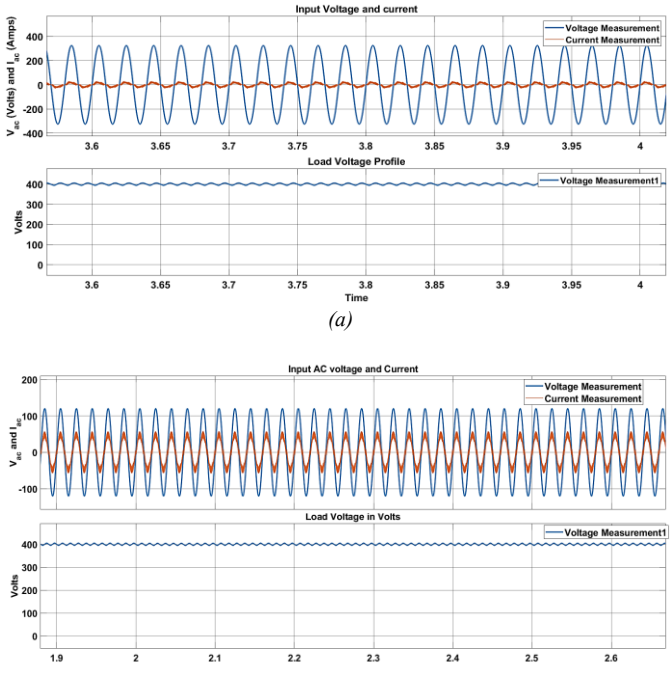

Figure 5. (a) Input Voltage (@120-volt peak), current and Load Voltage (b) Input Voltage (@325-volt peak), current and Load Voltage

In the third test the topology is then tested for over voltage of 400-volt peak. The result obtained are presented in *figure 6(a)*, in this case voltage and current have zero crossing providing unity power factor. However, the current profile gets distorted and ripples are generated shown in *figure 6(b)*. The figure is a zoomed image of the obtained input current profile. The DC output under voltage ripple less than 5% is maintained. The quantitative analysis results are tabulated in *table 2*.

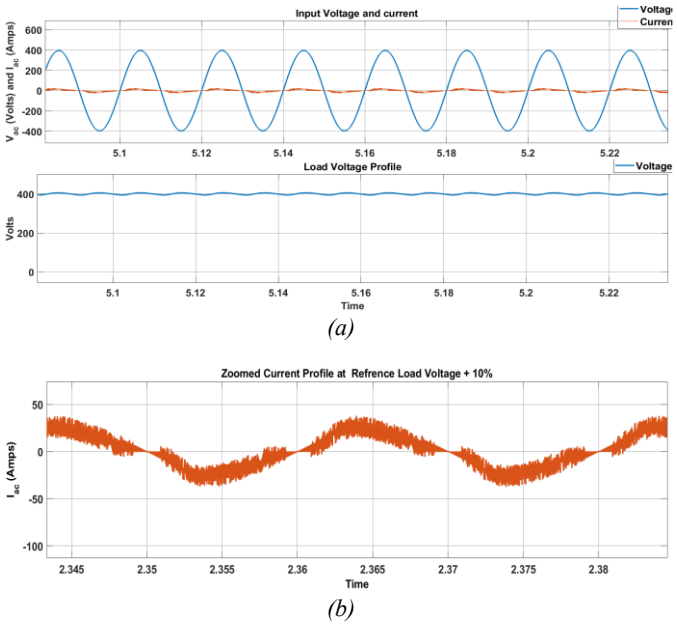

Figure 6. (a) Input Voltage (@400-volt peak), current and Load Voltage (b) Zoomed Image of current to watch ripples

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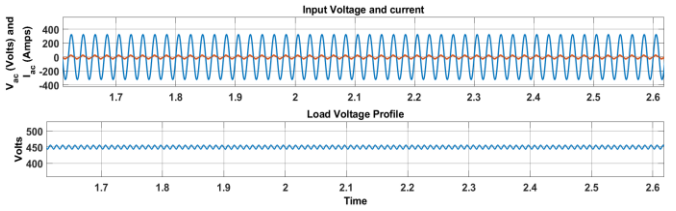
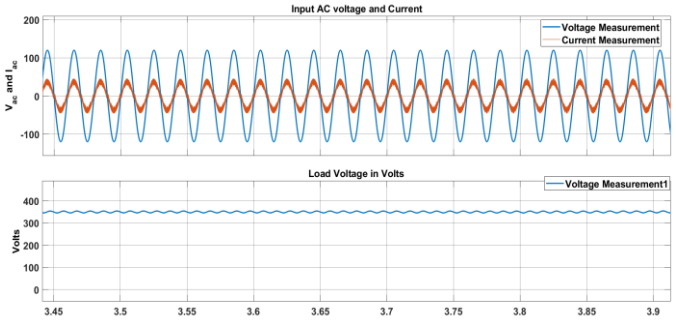
For obtaining a wide output voltage from the developed topology, the reference voltage is set for obtaining 450 volts and 350 volts DC output without changing any other parameter in the control and circuit. This change is approximately 12% up and down than the rated selected reference of 400 volts respectively. The obtained results demonstrate that unity power factor is obtained at rated input voltage for both set DC reference values. The obtained results are presented in *figure 7(a)* and *(b)* respectively.



(a)



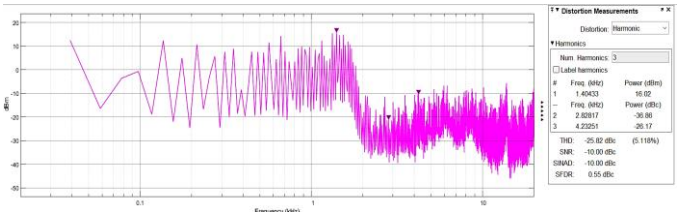
(b)

Figure 7. (a) Input Voltage (@ 325-volt peak), current and Load Voltage with reference 450-volt (b) Input Voltage (@ 325-volt peak), current and Load Voltage with reference 350 volt

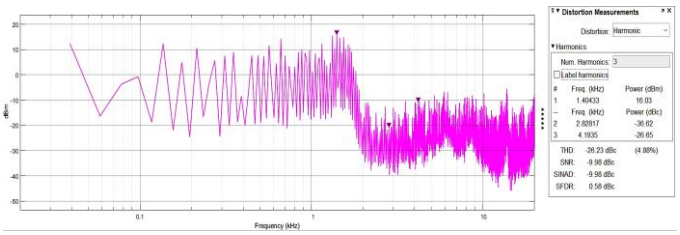
Table 2. Quantitative Simulation Results of Developed Topology

Input AC Voltage (V peak)	Input AC Current (A peak)	Unity Power Factor	DC Output Voltage (V)	DC Ripple (%)
120	2.5	0.93	400	4.2
325	6.8	0.96	400	3.7
400	8.5	0.94	400	4.8
325	6.8	0.95	450	4.1
325	6.8	0.95	350	3.9

To analyse the THD level in the input current, the current signal is passed through spectrum analyzer. For the rated input voltage and 400 volts DC reference output generation the results obtained through the DBR–Boost converter topology and Totem-Pole topology is presented in *figure 8(a)* and *(b)* respectively.



(a)



(b)

Figure 8. Input current Total Harmonic Distortion (THD) analysis for rated input voltage and 400 V DC output: (a) DBR–Boost converter, (b) Totem-Pole converter

The MATLAB Simulink simulation of the developed topology is computationally intensive, taking over 100 seconds for a 10-second simulation, highlighting the need for real-time validation before hardware implementation. Component behavior (inductors, capacitors, switches) at 40 kHz may vary in real conditions, so the topology was validated using the OPAL-RT 4510 real-time hardware-in-the-loop (HIL) platform. Figure 9 shows the setup comprising a Host PC, DSO, and OPAL-RT 4510, with a sampling time of 10 µs for continuous loop simulation. *Figure 10(a)* displays the input voltage (orange) and current (green) for a 325 V peak supply, showing in-phase alignment and unity power factor. The output DC voltage is shown in blue. Scaling factors were applied due to DSO limits: input voltage by 1/20, current by 1/5, and output voltage by 1/40, making one division equal to 400 V. *Figure 10* (b) shows current ripples at a 450 V peak input, still achieving zero-crossing with voltage.

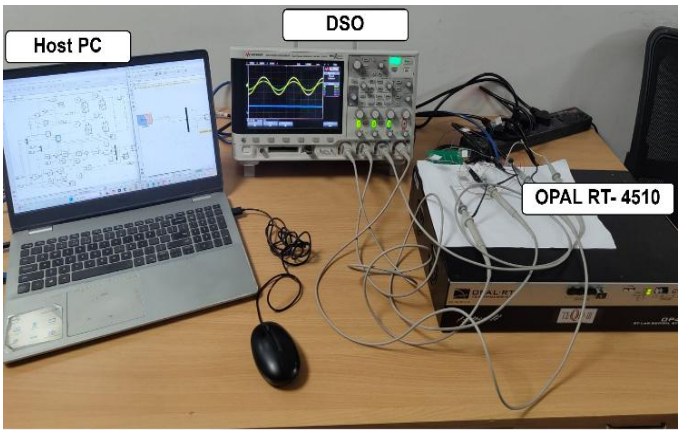


Figure 9. HIL Setup for validation of Topology

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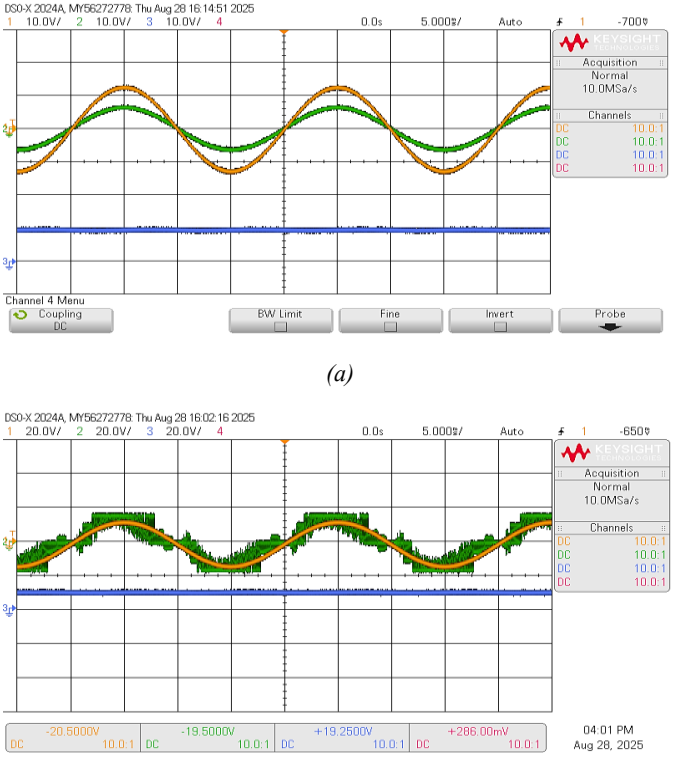


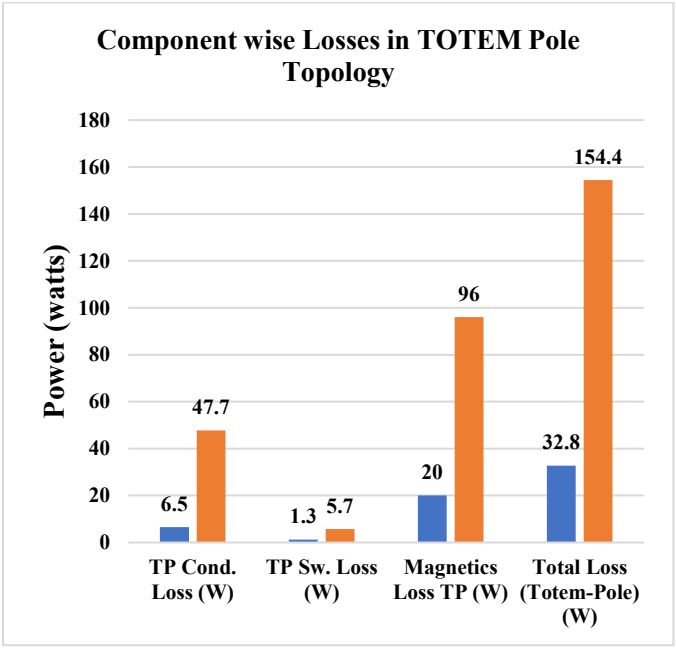
(a)

(b)

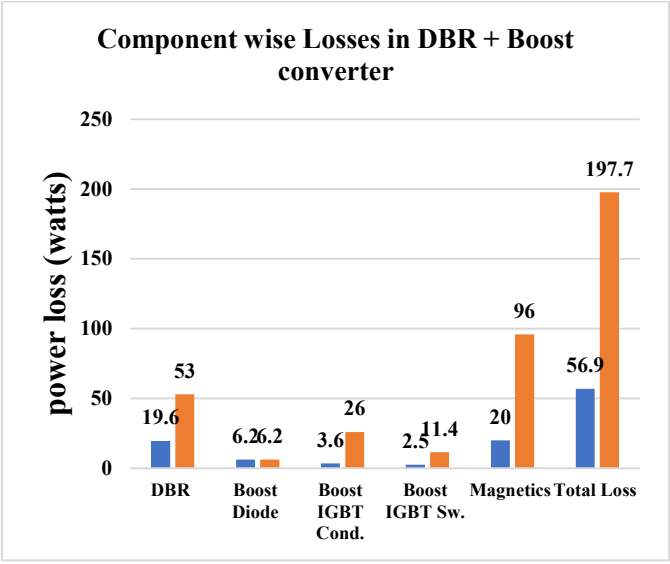
Figure 10. (a) Input AC voltage (@ 325-volt Peak), current and DC output (b) Input AC voltage (@ 450-volt Peak), current and DC output

5. POWER LOSS ANALYSIS

In this section the two topologies are compared on the criteria of efficiency, for doing these losses in every component is measured and efficiency is evaluated.



(a)



(b)

Figure 11. Losses in DBR and Boost converter

Figure 11 presents the component-wise losses for both topologies. *Figure 11(a)* shows the DBR + Boost converter, and *figure 11(b)* the Totem-Pole converter. Losses were calculated from voltage and current measurements, with switching losses as the product of voltage and current, and conduction losses as I^2R. For the DBR + Boost converter, lower input voltage (120 V peak) significantly increases losses compared to rated input (325 V peak). The diode bridge losses rise from 19.6 W to 53 W, boost IGBT conduction losses from 3.6 W to 26 W, and switching losses from 2.5 W to 11.4 W. Magnetic losses also jump from 20 W to 96 W, resulting in total losses of 197.7 W at 120 V versus 56.9 W at 325 V. Similarly, the Totem-Pole topology shows higher losses at lower input: conduction losses increase from 6.5 W to 47.7 W, switching losses from 1.3 W to 5.7 W, and magnetic losses from 20 W to 96 W, giving total losses of 154.4 W at 120 V compared to 32.8 W at 325 V.

Table 3 summarizes the quantitative comparison of the two topologies. The Totem-Pole achieves higher peak efficiency (+1.8%), improved power factor (+2%), slightly lower THD, and reduced total losses (−43.3 W at 325 V), confirming its superior performance under both low and rated input conditions.

Table 3. Comparative analysis of two discussed topologies for quantitative analysis

Parameter	DBR–Boost	Totem-Pole	Improvement
Peak Efficiency (%)	91.7	94.5	+2.8 %
Power Factor (PF)	0.93	0.95	+2%
THD (%)	5.118	4.88	0.238%
Total Loss (W @325V)	197.7	154.4	−43.3

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6. CONCLUSION

The comparative analysis between the conventional DBR–Boost converter and the Totem-Pole Bridgeless Boost converter demonstrate clear performance advantages of the proposed design. Quantitative evaluation reveals a 2.8% increase in efficiency, 2% increase in PF, and THD reduced by 0.238%. Both MATLAB/Simulink and OPAL-RT validations confirm high consistency, with less than ± 2.5% deviation between simulation and experimental data.

The presented stage-wise power loss method provides a practical benchmark for evaluating PFC converters, and the validated results establish the Totem-Pole topology as a superior choice for high-efficiency, low-distortion AC–DC conversion systems.

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